Static Noise Margin Evaluation Method Based on Direct Polynomial-Curve-Fitting with Universal SRAM Cell Inverter TEG Measurement

Kazuyuki Nakamura, Kazunori Noda, and Hiroki Koike*

Center for Microelectronic Systems, Kyushu Institute of Technology
* Fukuoka Industry, Science & Technology Foundation
680-4 Kawazu, Iizuka, Fukuoka 820-8502, Japan
Tel: +81-948-29-7584, Fax: +81-948-29-7586, Email: nakamura@cms.kyutech.ac.jp

ABSTRACT

A new method to evaluate the Static Noise Margin (SNM) for leading-edge CMOS SRAM development is proposed. This method includes: (1) direct measurement of the inverter DC transfer curves using a "Universal SRAM Cell Inverter TEG (USCIT)" with arbitrary transistor ratios, (2) curve-fitting of the measured data to polynomial functions in a 45-degree rotated space, and (3) a database of the polynomial coefficients to evaluate and optimize the SNM by a simple algebraic operation. The SNM values obtained using this method are in good agreement with the measured SRAM operations.

INTRODUCTION

In the development of SRAMs for the 45-nm technology generation and beyond, it is difficult to maintain a sufficient static noise margin (SNM) in the SRAM because of supply voltage scaling and device variability [1][2]. Historically SNM analysis using classical MOSFET Id-Vd expressions has been used, but it has been shown that this cannot fit the scaled CMOS technologies. A method that uses SPICE simulation is now more widely used; the procedure for this is depicted in Fig. 1 [3][4]. This method comprises the following steps: (i) measuring I-V characteristics for a single transistor TEG, (ii) extracting the SPICE model parameters, (iii) simulating DC transfer curves of the inverter in an SRAM cell, and (iv) drawing the butterfly curves by combining the two inverter characteristics and reading off the SNM value. This method is, however, inadequate in several aspects, such as fitting errors in the SPICE model parameter extraction and the accuracy limit of the SPICE simulation. This imposes considerable restrictions on the design of highly scaled CMOS SRAM.

NEW SNM EVALUATION METHOD

The proposed method, illustrated in Fig. 2, comprises the following steps: (1) direct measurement of inverter DC transfer curves using an USCIT that can realize arbitrary transistor ratios, (2) fitting of the measured data to polynomial functions in a 45-degree rotated space, and (3) storing the coefficients of the polynomial functions in a database to evaluate and optimize the SNM by a simple algebraic operation. Since this method is based on measured data and directly curve-fitted polynomials, neither SPICE model extraction nor other accuracy degradation steps are included. In addition, the SNM can be obtained simply by subtracting the coefficients of two polynomials which can be stored in a database based on the measured data. This method requires neither SPICE simulation nor drawing butterfly curves, therefore, it is suitable for statistically aware memory cell optimizations.

DESIGN OF UNIVERSAL SRAM CELL INVERTER TEG (USCIT)

A typical 6-transistor SRAM cell circuit is shown in Fig. 3. To calculate the SNM, the DC transfer characteristics of the inverter with three transistors, namely Load PMOS (PL), Driver NMOS (ND), and Transfer NMOS (NT), must be evaluated. We have developed the USCIT that can evaluate arbitrary transistor ratios for these three transistors with selectable binary-weighted transistor arrays as shown in Fig. 4. The gate width (W) can be set by 5-bit signals for PLi, NDj, and NTk (where i, j, k=0~4), respectively. We design the five gate widths for the weighted transistor array: 1/1.5/2/4/8 x Wmin, instead of a simple binary-weighted array using Wmin as the base. Wmin is the minimum transistor gate width determined by process technology. By combining these widths, we can successfully achieve any transistor size covering 1.0 ~ 15.5 times the value of Wmin with a minimum resolution of half the value of Wmin. As a result, about 30,000 design combinations can be examined with this USCIT. Fig. 5 shows the layout of an USCIT using 0.18-um technology. The macro size is 17 x 108 um^2. The measured DC transfer characteristics for the USCIT are shown in Fig. 6. By setting the level of the BL terminal to VDD or GND, we obtain the DC transfer curves (Fig.6 (a) and (b)) corresponding to the SRAM READ/WRITE operations, respectively.

POLYNOMIAL-CURVE-FITTING IN A 45-DEGREE ROTATED SPACE

A method that utilizes Butterworth filter function for DC transfer curve fitting was proposed [5]. However, we tried

to fit the DC transfer curves measured by the USCIT to simpler polynomial functions. Since parts of the curve are parallel to the X- or Y-axis as shown within the dotted area in Fig. 7(a), it would be difficult to fit the curve accurately even if the degree of the polynomial were increased. In order to solve this issue, we rotate the measured curve by 45 degrees in the X-Y coordinates before the polynomial curve fitting. Table 1 compares the accuracy of the curve fitting between the original and rotated curves. Rotating the curve improves the accuracy significantly. The error can be suppressed down below 1% by extending the polynomial to the degree of 4. The results of fitting a curve to a polynomial function of degree of 5 are shown in Fig. 7(b).

SNM Calculation with Polynomial Database

The SNM of an SRAM cell is calculated from the polynomial functions of the 2 inverters that compose the SRAM cell. Here we assume that the 2 characteristics are expressed by the following polynomial functions;

$$y_1(x) = (1/\sqrt{2}) \sum_{k=0}^{n} (a_{1k} \cdot x^k) \quad \ldots (1)$$

$$y_2(x) = (1/\sqrt{2}) \sum_{k=0}^{n} (a_{2k} \cdot x^k) \quad \ldots (2)$$

The SNM function, snm(x), is defined by subtracting $y_2(-x)$ from $y_1(x)$. Using Eqs. (1) and (2), we obtain

$$\begin{aligned} snm(x) &= y_1(x) - y_2(-x) \\ &= (1/\sqrt{2}) \sum_{k=0}^{n} [\{a_{1k} - (-1)^k \cdot a_{2k}\} \cdot x^k] \quad \ldots (3) \end{aligned}$$

An example of function snm(x) is plotted in Fig. 8. The SNM is the smaller of the absolute values of the 2 extrema (maximum and minimum values) in Eq. (3). Note that if the polynomial functions are fitted into 5-degrees or less, the algebraic solution can be used to find the extrema. As a result, the corresponding SNM value can be calculated instantly by a simple algebraic operation on the polynomial coefficients in the fitted-curve database.

Experimental Results

We have fabricated a 256-bit SRAM chip, in which the unit cell is composed of two USCITs as shown in Fig. 4. The chip layout is shown in Fig. 9. Figs. 10(a), (b), and (c) show correlations between the SNM values calculated from the conventional SPICE simulation method, SNM values obtained from the measurement results of the USCIT, and PASS/FAIL values of an entire 256-bit SRAM TEG chip operation, respectively. The horizontal and vertical axes denote the gate widths for Transfer NMOS (NT) and Load PMOS (PL), respectively. The Drive NMOS (ND) size is fixed in all cases. In Figs. 10(a) and (b) the smaller of the Write or Read SNM values [in mV] is written in each block, with Write SNM values appearing in a Italic font and Read SNM values in a solid font. Each black and hatched block denotes the region where SNM < 0 and 0 ≤ SNM < 60mV, respectively. In Fig. 10(c), 'P' and 'F' indicate Pass and Fail operations, respectively. According to these results, the measured operational margin of a 256 bit SRAM (Fig.10(c)) is in good agreement with the SNM evaluation from the USCIT measurement (Fig.10(b)), when taking into account the cell transistor mismatch (i.e., 60mV for this measurement).

Conclusion

We have developed a new SNM evaluation method based on the measurement results of an USCIT, polynomial curve fitting with a 45-degree rotation, and a polynomial coefficients database. This method has demonstrated greater accuracy than the conventional method that uses SPICE simulation, and is suitable for data processing covering the comprehensive conditions such as transistor-sizes, voltage, temperature, etc. The proposed method is, therefore, especially effective in establishing reliable guidelines for the early-stage development of highly scaled CMOS SRAM cells.

Acknowledgments

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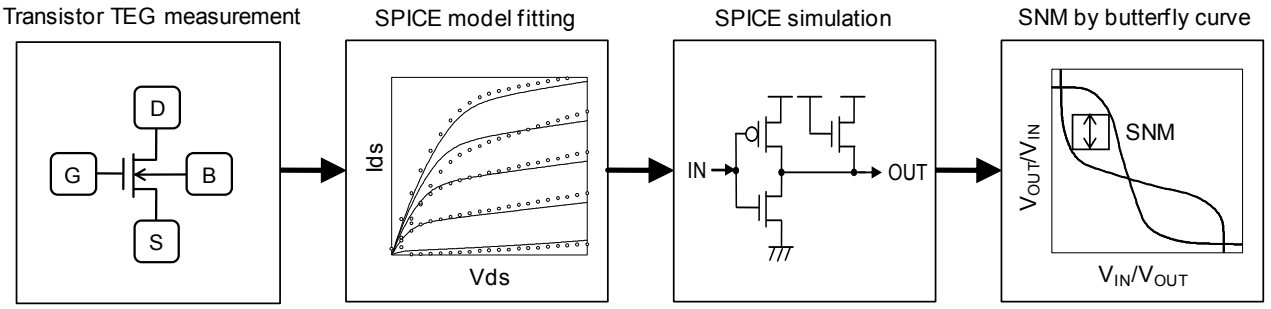


Fig. 1 Conventional method for calculating SNM values

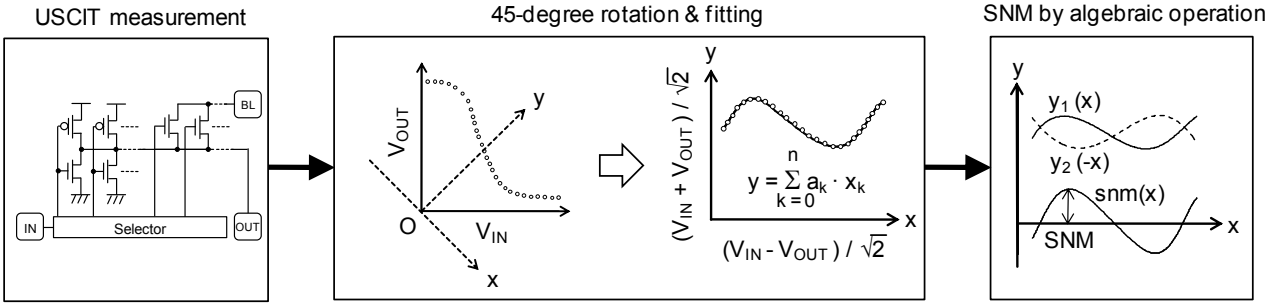


Fig. 2 The proposed method for calculating SNM values

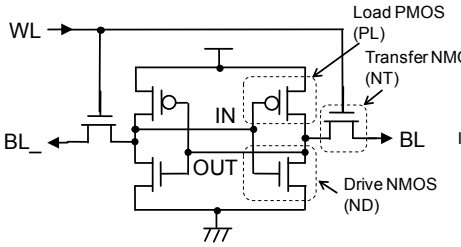


Fig. 3 6T-SRAM cell circuit

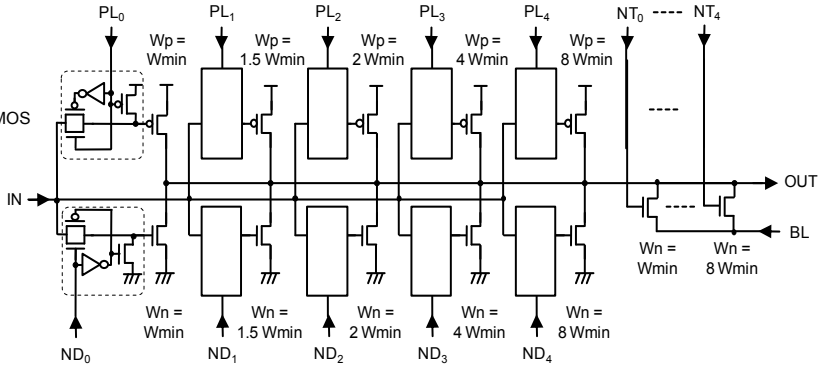


Fig. 4 USCIT circuit to measure inverter DC transfer characteristics

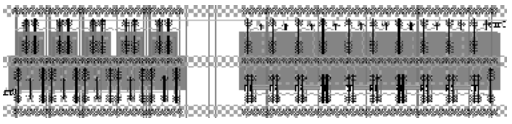
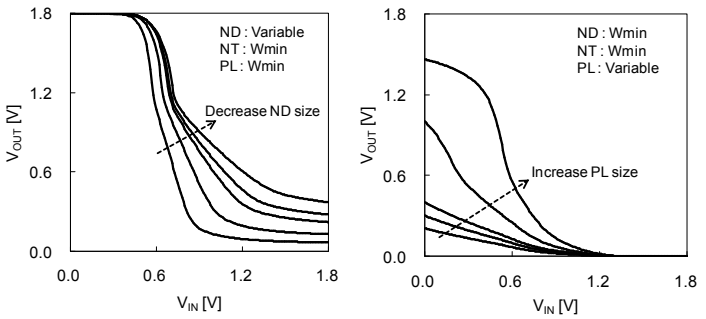


Fig. 5 Layout of the USCIT

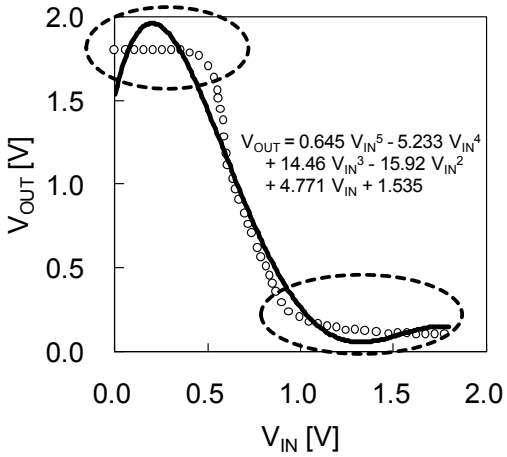
TABLE I
FITTING ERROR VERSUS THE DEGREE OF THE POLYNOMIAL USED FOR FITTING

Degree of polynomial	3	4	5	6	7	8	9
Original curve fitting [%]	10.4	5.7	5.6	4.0	2.8	2.8	2.1
45-degree rotated curve fitting [%]	2.0	0.7	0.7	0.6	0.6	0.2	0.2

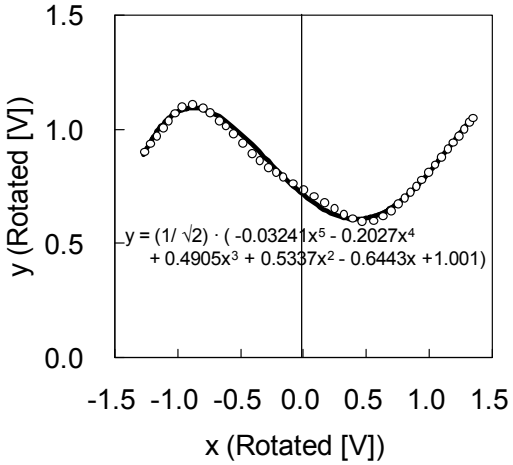


(a) BL=VDD (b) BL=GND

Fig. 6 Measured inverter DC transfer characteristics



(a) Original



(b) After 45-degree rotation

Fig. 7 Examples of DC curve fitting to a polynomial of degree of 5
(Circles indicate measured data, while the solid line is the fitted curve.)

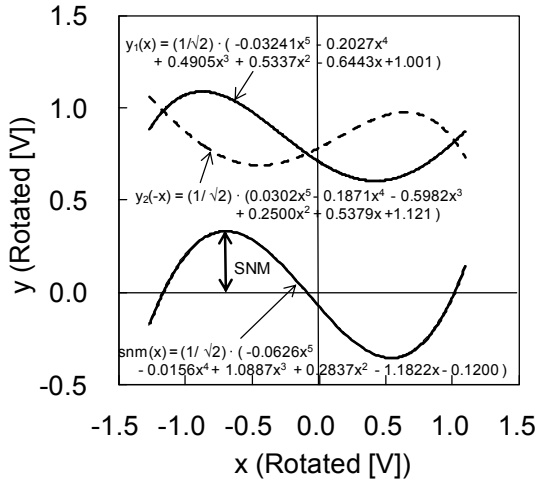


Fig. 8 An Example of SNM calculation

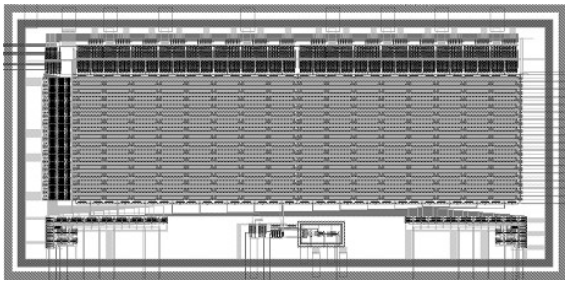


Fig. 9 256-bit SRAM TEG layout using 0.18-um technology

W of NT / W of PL

268	169	31	4	<0	<0	<0	<0	<0	<0	<0
287	190	54	28	<0	<0	<0	<0	<0	<0	<0
305	228	97	67	<0	<0	<0	<0	<0	<0	<0
316	224	93	71	<0	<0	<0	<0	<0	<0	<0
138	252	125	101	22	<0	<0	<0	<0	<0	<0
84	260	137	113	35	6	<0	<0	<0	<0	<0
<0	268	160	138	62	33	<0	<0	<0	<0	<0
<0	*224*	169	146	71	43	<0	<0	<0	<0	<0
<0	*145*	187	165	92	65	17	<0	<0	<0	<0
<0	*117*	194	172	101	73	26	5	<0	<0	<0

(a) SNM for Conventional method (using SPICE simulation)

W of NT / W of PL

320	231	114	101	28	1	<0	<0	<0	<0	<0
338	249	135	120	48	17	<0	<0	<0	<0	<0
283	283	170	157	86	57	12	<0	<0	<0	<0
269	279	166	153	82	53	8	<0	<0	<0	<0
123	304	194	180	111	82	39	20	<0	<0	<0
70	312	202	189	121	92	48	30	0	<0	<0
<0	*268*	221	210	142	114	70	52	23	4	<0
<0	*218*	230	218	151	123	80	59	33	19	<0
<0	*137*	245	233	167	140	97	79	50	38	16
<0	*109*	250	238	173	145	103	85	56	43	22

(b) SNM for Proposed method

W of NT / W of PL

P	P	P	P	F	F	F	F	F	F	F
P	P	P	P	F	F	F	F	F	F	F
P	P	P	P	P	F	F	F	F	F	F
P	P	P	P	P	F	F	F	F	F	F
P	P	P	P	P	P	F	F	F	F	F
P	P	P	P	P	P	F	F	F	F	F
F	P	P	P	P	P	P	F	F	F	F
F	P	P	P	P	P	P	F	F	F	F
F	P	P	P	P	P	P	P	F	F	F
F	P	P	P	P	P	P	P	F	F	F

(c) Measured PASS/FAIL with 256-bit SRAM Operation

Fig. 10. Experimental results