Real-time failure monitoring system for high power IGBT under acceleration test up to 500 A stress

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***Abstract*—Real-time failure monitoring system for IGBT module was demonstrated under 500 A power cycling test. The system successfully captured internal phenomena occurred in interface regions of the device under test. Moreover, we proposed real-time failure analysis method by combining the real-time monitoring and image processing techniques. This failure analysis method enables to distinguish the place where degradation occurs in DUT and also trace internal degradation process to failure.**

I. Failure Analysis Based on Real-Time Monitoring

Power devices have been required to have mass productivity according with the increase in the demands in energy saving application field, therefore, "Reliability" enhancement of power devices will become important technology for future power electronics. In many cases, post-defect or interim samples picking out under testing have been used for the failure analysis. With this way, it is often difficult to identify the real cause of failure because of incidental damages especially for high power density modules [1,2]. On the other hand, a real-time monitoring of internal phenomena of devices under test (DUT) is one solution for this difficulty of the failure analysis. Information about which kind of degradation is true cause of the failure and in which time domain the degradation propagates through the failure process is the most distinctive feature of real-time monitoring based failure analysis. Such kind of information was difficult to obtain by post-defect way and it is necessary not only for reliability assessment but also for failure prediction.

II. Real-Time Monitoring System for Internal Degradation of Power Devices

We have developed a real-time monitoring system for internal failure analysis system for power devices [3,4]. Main components of this system were (1) inside imaging by SAT, (2) high power stress control by DC power supply, (3) water cooling of DUT and (4) chip temperature monitoring (Fig. 1).

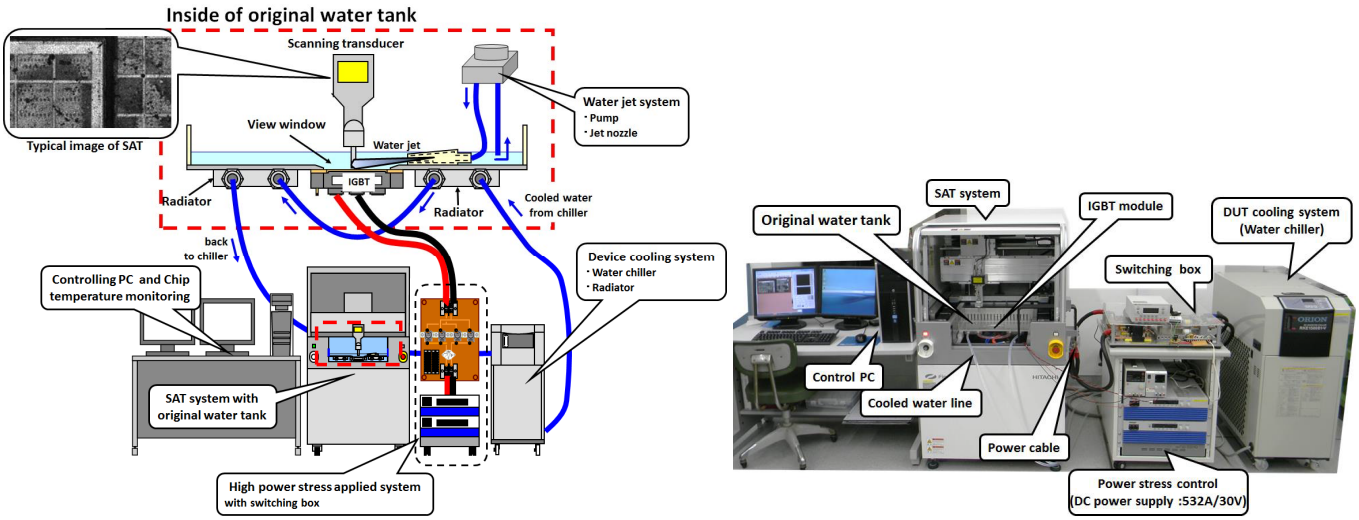
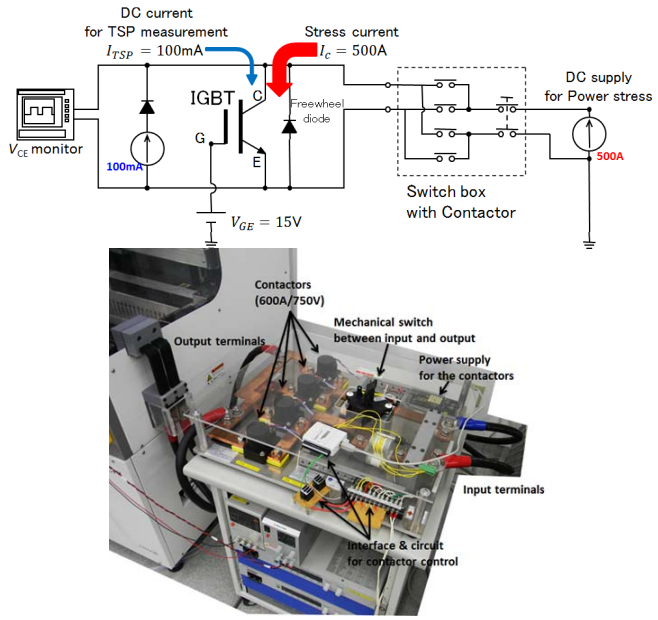


Figure 1. Real time failure monitoring system for high power IGBT modules



Fugure 2. Power cuircuit with switching box

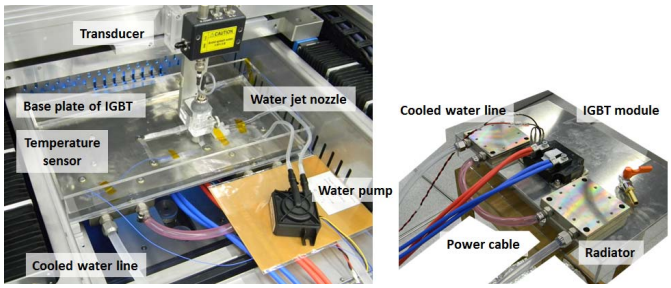


Figure 3. Experimental set-up with original design water tank

A. *Inside Imaging of Power Devices*

The scanning acoustic tomography (SAT) is often used for the post-defect failure analysis to inspect degradations such as delamination or clack propagation in the interface of power devices [5-10]. In recent years, SAT systems have achieved to fine resolution of less than few μm, and maximum scan speed up to 1000 mm/s [11] and they will be potentially improved. This property of SAT is preferable to high speed imaging like the real-time monitoring. As for our real-time monitoring system, SAT imaging monitor was captured as a movie during the power cycling test.

B. *High Power Stress Controll*

The power cycling was applied by PC controlled 16kW (I_c = 532 A) DC power supply. The power supply was connected to DUT by bus bars and bold wires via switching system constructed by DC contactors (Fig.2). The contactors were controlled by TTL signal form PC and enable to isolate DUT from the power supply mechanically and also enable to change a polarity of the bias applied to DUT. The power stress sequence was programed through an original GUI.

C. *Water Cooling of DUT*

The temperature of a base plate of DUT was controlled by couplant water for SAT imaging which was necessary for ultrasonic wave transmission. Only observed surface of DUT was immersed the couplant water cooled by radiators placed at the bottom of an original design water tank (Fig. 3). In addition, a water pump and a water jet nozzle were prepared to generate efficient water flow along DUT surface and to remove tiny bubble generation by self-heating of DUT [3,4].

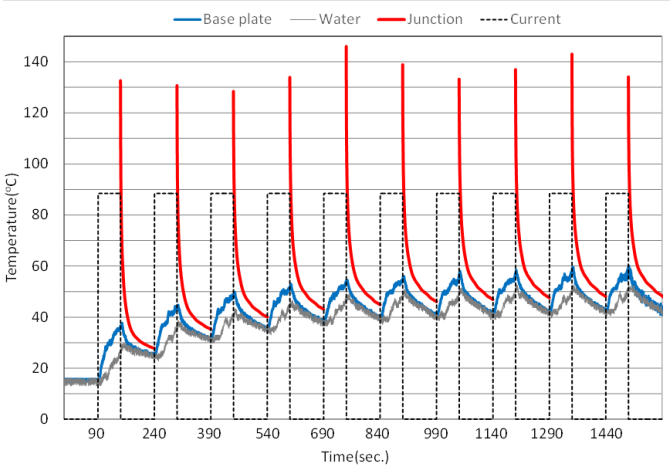


Figure 4. Temperature change with power stress

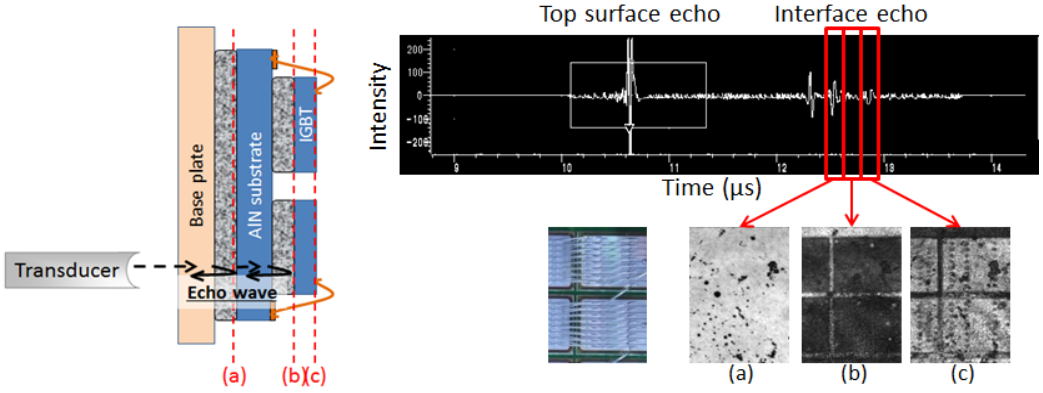


Figure 5. Procedure to obtain different interface SAT image

D. *Chip Temperature Monitoring*

The junction temperature T_j of DUT was estimated from temperature sensitive parameter of on-state voltage drop at low current (Fig. 2). The I_{TSP} =100 mA was applied and the corrector-emitter voltage V_{CE} of IGBT was monitored at all time of power cycling. When the power stress was turn-off, the DUT was immediately isolated from the high power supply by using the switching system. The T_j was estimated numerically from V_{CE} by a conversion formula experimentally obtained.

III. Demonstration with 500 A Power Cycling

The real-time failure monitoring system was demonstrated by an IGBT which maximum rating of collector current was I_C = 400 A DC. The power stress of 500 A was applied to the device with the gate-emitter voltage of 15 V. The power

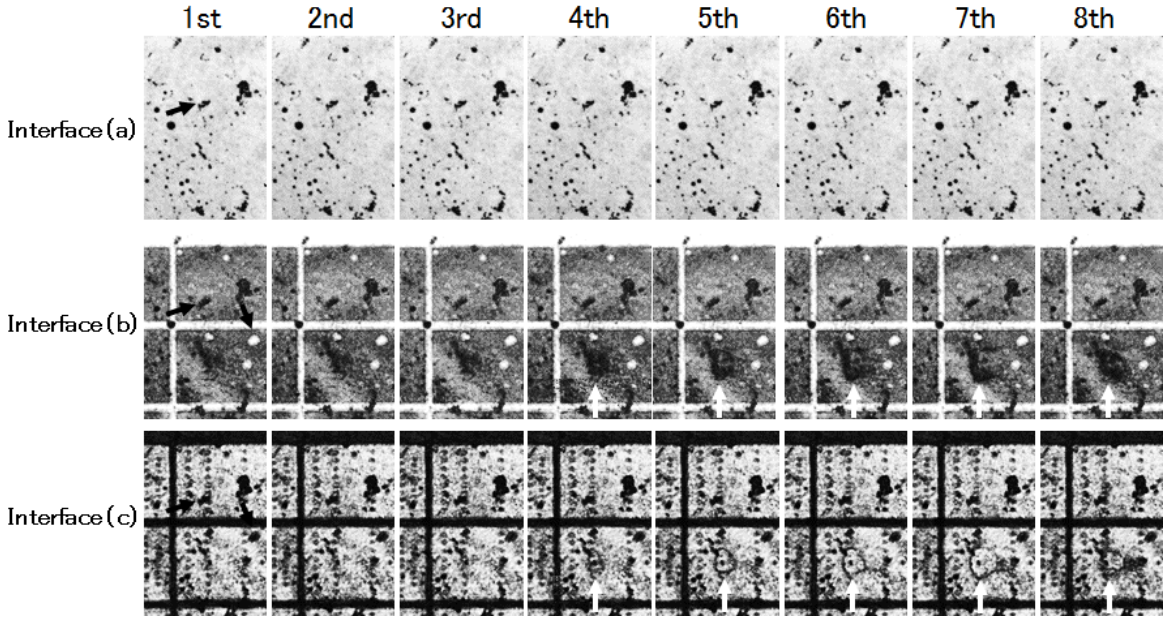


Figure 6. Inside images of IGBT obtained during power stress test

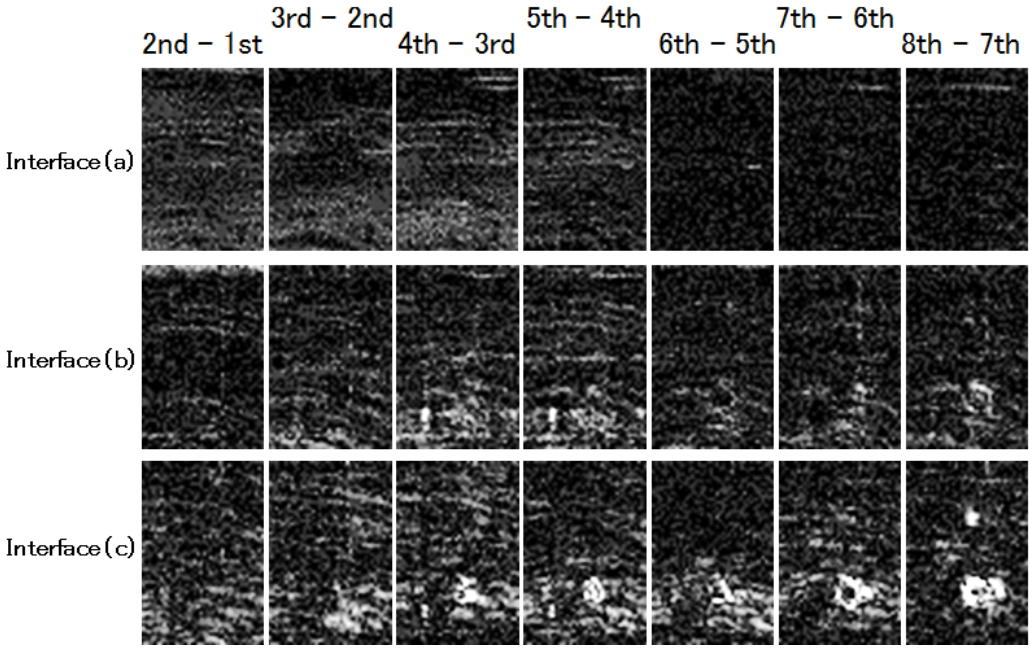


Figure 7. Subtract images obtained by each 10 power cycling

cycling sequence was 60 s turn-on and 90 s turn-off. Fig. 4 shows typical variation of temperatures at this demonstration. The temperature of surrounded water and the base plate was gradually elevated and it settled at around 45 °C after 10 times power cycle. The T_{high} and T_{low} also elevated with same tendency and these were settled around 135 °C and 50 °C, respectively, namely the ΔT_j was approximately 85 °C in this demonstration.

Three different interface regions were observed at the same time in this demonstration by using reflected echo in different time domain as shown in Fig. 5. Fig. 6 shows series of SAT images obtained by each 10 cycle in a certain time domain of the power cycling test. As shown in Fig. 5, interface labeled (a) to (c) was corresponded to base plate / solder, solder / chip and top region of the chip, respectively. The acquisition windows of reflected echo were configured from the base plate to the chip, therefore, if internal degradation occurs in the interface (a), other interface images (b) and (c) are affected by it. Such kinds of dark or bright spots in the image are pointed by black arrows in 1st image. A slight change of image was occurred at the chip center in the 4th image of interface (b) and (c), and it propagated to wide area. No image change was observed in this area in the interface (a), therefore, some internal change took place at the interface (b) or (c).

Fig. 7 shows subtract images obtained from each 10 power cycles, for example, the images leveled "2nd – 1st" was obtained by subtract the image "1st" from the image "2nd" in Fig. 6. The gray scale level was corresponded to the degree of brightness change in a pixel during the power cycle test. The brightness change in the interface (c) was obvious in comparison to the other interfaces and it started from the image "4th – 3rd". Judging from this result, it is considered that the some serious phenomena took place in the interface (c) and it affected to interface (b) in the power cycling after the image "3rd". In this way, by tracing the subtract images in the same interface, namely comparing the images in horizontal rows in Fig. 7, we can find out that internal changes had occurred in which time domain in the failure process. Moreover, by comparing the images in the same time domain, namely comparing the images in vertical rows, we can find that an internal change was occurred in which interface inside of DUT. Combining real-time monitoring under acceleration test and image processing techniques enables us new time domain failure analysis of power devices.

IV. CONCLUSION

We have developed a real-time failure monitoring system for IGBT and demonstrated this system under 500 A power cycling test. The system successfully captured a internal change in individual interface. Moreover, we propose a time domain failure analysis methods with image processing techniques.

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