New Measurement Base De-embedded CPU Load Model for Power Delivery Network Design

Motochika Okano[1,2], Koji Watanabe[3], Masamichi Naitoh[1], and Ichiro Omura[1]
[1] Kyushu Institute of Technology, Japan
[2] Toshiba Corporation, Japan
[3] Toshiba Digital Media Engineering Corporation, Japan

***Abstract*-- CPU load model including on-chip wiring and package interconnection has been required for printed circuit board (PCB) design of digital products according to the improvement in the speed of CPU operation in recent years. Especially, accurate power delivery network (PDN) information inside CPU is indispensable for PCB design according to requirement of low-impedance and the broadband (from DC to GHz) from the inside of CPU to DC-DC converter. While the detailed impedance information inside CPUs is not disclosed to PCB board designers with the complicated back-end and front-end production design for CPU chip and package. This paper aims to establish new methodology to extract CPU load model with combination of measurement and simulation. The method is simple yet powerful for high-end CPU board design.**

***Index Terms*-- CPU Load Model, De-embedded, Power delivery network, Target impedance**

I. Introduction

Severe voltage margin for the CPU power supply has been required according to the decrease of supply voltage for high performance CPU. In order to supply required power to the CPU under GHz operation, it is necessary to precisely design the power delivery network (PDN) from DC-DC converter to the digital circuit on CPU chip including wiring on the chip, in the package, and other interconnections as shown in Fig. 1.

Specially, mΩ level low-impedance characteristics along entire PDN is required in frequency range up to tens of GHz. This impedance is called "Target impedance" (Z_t). Power supply voltage, Current consumption, and Z_t of high-end CPU in recent years are shown in Fig. 2. Z_t is calculated by (1).

$$Z_t = \frac{V_s \cdot 10\%}{I_c} \tag{1}$$

Where V_s is the Power supply voltage and
I_c is the Current consumption.

Current consumption I_c has the frequency dependence, so that Z_t also has the frequency dependence as shown in (2).

$$Z_t(f) = \frac{V_s \cdot 10\%}{I_c(f)} \tag{2}$$

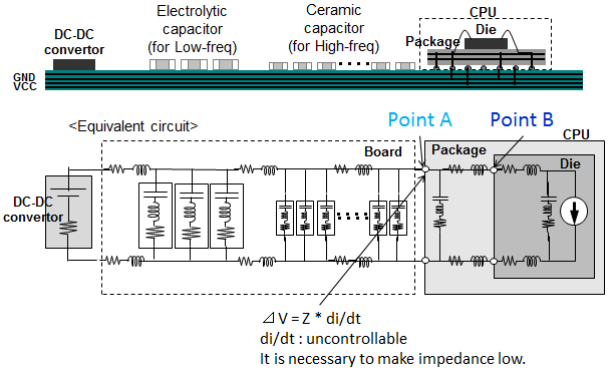


Fig. 1. PDN from DC-DC converter to the inside of CPU.

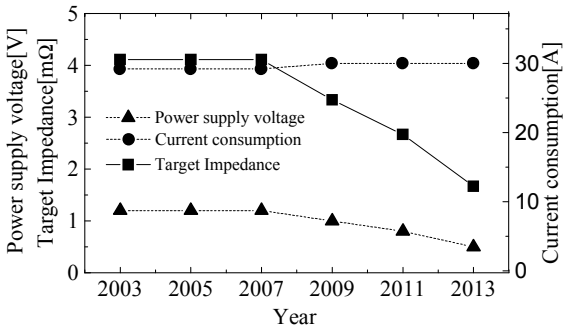
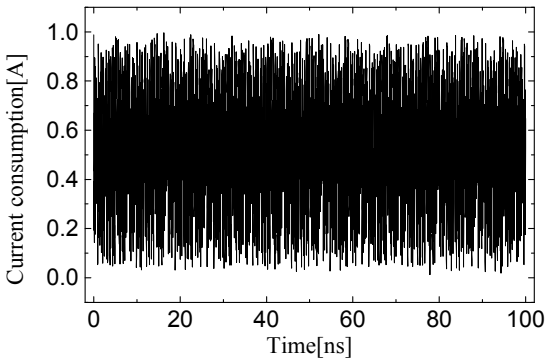


Fig.2 Trend of high-end CPU
Power supply voltage (V_s), Current consumption (I_c), and Target impedance (Z_t).

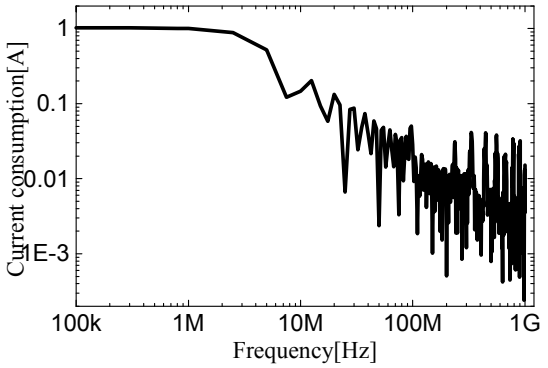
Current waveform (Time domain) of CPU and its frequency dependence (Frequency domain) by Fourier transform are illustrated in Fig. 3. Frequency domain target impedance Z_t can be directly obtained from Fig. 3 (b) as shown in fig. 4. The target impedance Z_t is defined as the lower side envelope of the impedance curve obtained.

As indicated in Fig. 4, although the frequency basis impedance increases as frequency, Z_t is required to maintain relatively low level even in high frequency range.

Since the CPU load models are not disclosed from CPU vendors to board designers, the amount of capacitors has been assembled on the PCB, based on designer's experience, to maintain low impedance up to the high frequency and no practical method exists to ensure the design validity.



(a) Time domain



(b) Frequency domain

Fig.3. Example of Current consumption waveform.

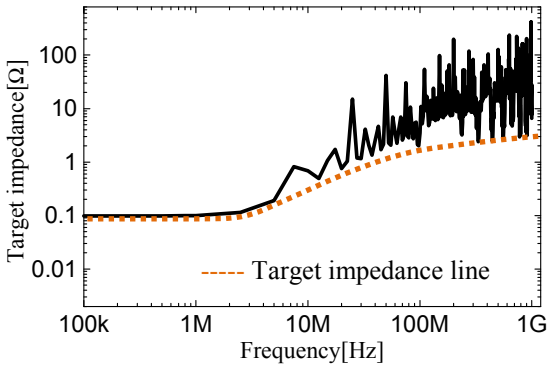


Fig.4. Example of Target impedance.

In order to realize PDN for required target low impedance and frequency, with minimum number of capacitors, it is necessary to design entire network including inside CPU package and on-chip wiring. The CPU impedance information is not disclosed from the CPU vendor, thus extraction method become important. Although there have been some papers on extraction method for impedance inside CPU [1-3], the low accuracy and the complication has been the problem. This paper aims to introduce novel method to extract CPU impedance inside package by the combination of measurement and simulation. The method is simple and accurate without special measurement tools. The method will contribute efficient design for CPU power delivery on PCB.

II. Necessity of CPU load model

The PDN impedance with and without CPU load model are shown in Fig. 5. The PDN impedance curves ("blue" and "aqua" colored lines in Fig. 5) are calculated with the exact CPU load model specially calculated from the chip and the package design detail in Toshiba Corp. for the particular CPU. The detailed PKG design data used for the exact load mode is shown in Fig. 6. The model includes the effect of vias and bonding wires inside CPU package. (The data and model is not provided for users).

The "blue" line is the impedance at CPU chip indicated by Point B in Fig. 1, and the "aqua" line is the impedance of at package BGA indicated by Point A in Fig. 1. It should be noted that detailed package wiring data is required to obtain the impedance at CPU chip shown by "blue" line in Fig. 5, thus the impedance at Point A is the practical index for the board design without detailed package and CPU wiring information.

Without CPU load model, the calculated PDN impedance is out of the target impedance at high frequency range as shown in "Black" line. Therefore, the number of required capacitors is always over estimated by the board designer, resulting higher board cost and larger board size. Further, mutual correlation effects, such as anti-resonance effect appeared at 20 MHz in Fig. 5 in "blue" and "aqua" line, are not considered without CPU load model.

The CPU load model is important for following three points according to above discussion.

(a) Provide CPU model to board designer to minimize on-board capacitors
(b) Ensure the board design validity to the target impedance of the PDN
(c) Co-design of PCB board – CPU package in terms of PDN quality

As described, most of the CPU vendors do not provide the CPU load model of their products nor detailed package and CPU wiring information. Therefor the accurate extraction method for the CPU load model is indispensable. In the next section, the new experiment – simulation combined CPU load model extraction method is proposed. The CPU load model is extracted from the difference between PDN impedances obtained by board level measurement with CPU on the board and by the board level simulation without CPU. This technique is the very powerful to minimize the size and cost in terms of PDN design, even if the CPU model is not provided from the CPU vendor.

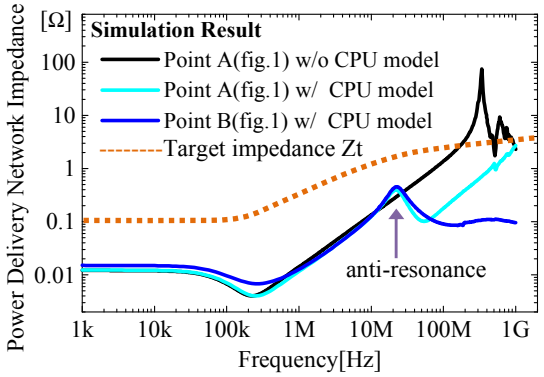
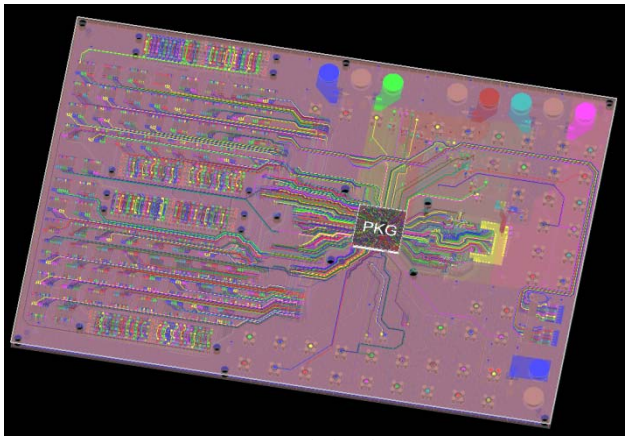
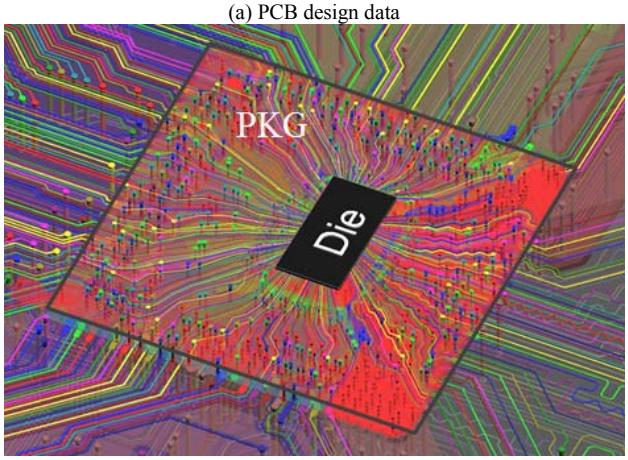


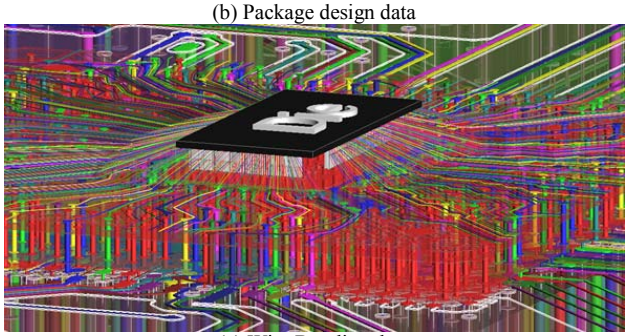
Fig. 5. PDN Impedance w/ and w/o CPU. CPU load model is precisely calculated from CPU design data.



(a) PCB design data



(b) Package design data



(c) Wire Bonding data

Fig. 6. PCB and Package design data mounted CPU inside Toshiba, which is not disclosed for users.

III. New Extraction Method

PCB in which CPU was mounted is prepared, and the Power-GND impedance is measured. Moreover, the Power-GND impedance is simulated in the state where all parts included CPU are not mounted, using PCB design data. The PDN information inside CPU is extracted by taking these both difference. The image is shown in Fig. 7.

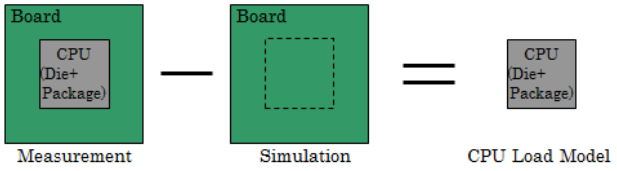


Fig. 7. CPU Load Model extraction concept.

A. Proposed Method

The relation of input and output can be realized by (3) (4) and (5), if F parameter [F_{PCB}] is defined as shown in Fig. 8.

[F_{PCB}] is converted from S parameter by (6) even in high frequency. This S parameter [S_{PCB}] is the impedance of the PCB without CPU, and it can calculate it in analysis from PCB design data.

Z_{IN} is the Power-GND impedance. S_{11} of S parameter between Power and GND of input side is measured using PCB with CPU by Shunt-Thru method. In Shunt-Thru method, the transmission characteristic (S_{11}) comes to hand as S_{21}. Z_{IN} can be transformed from S_{11} by (7).

$$\begin{bmatrix} I_{IN} * Z_{IN} \\ I_{IN} \end{bmatrix} = \begin{bmatrix} F_{PCB11} & F_{PCB12} \\ F_{PCB21} & F_{PCB22} \end{bmatrix} \begin{bmatrix} I_{CPU} * Z_{CPU} \\ I_{CPU} \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} \frac{I_{CPU}}{I_{IN}} * Z_{CPU} \\ \frac{I_{CPU}}{I_{IN}} \end{bmatrix} = \begin{bmatrix} F_{PCB11} & F_{PCB12} \\ F_{PCB21} & F_{PCB22} \end{bmatrix}^{-1} \begin{bmatrix} Z_{IN} \\ 1 \end{bmatrix} \tag{4}$$

$$\text{If} \frac{I_{CPU}}{I_{IN}} * Z_{CPU} = a\,,\ \frac{I_{CPU}}{I_{IN}} = b \ \text{ then } \ Z_{CPU} = \frac{a}{b} \tag{5}$$

$$\begin{bmatrix} F_{PCB11} & F_{PCB12} \\ F_{PCB21} & F_{PCB22} \end{bmatrix} = \frac{1}{2 \times S_{21}} \begin{bmatrix} (1+S_{11})(1-S_{22}) + S_{12}S_{21} & \left[(1+S_{11})(1+S_{22}) - S_{12}S_{21}\right] \cdot Z_{ref} \\ \frac{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}{Z_{ref}} & (1-S_{11})(1+S_{22}) + S_{12}S_{21} \end{bmatrix} \tag{6}$$

$$Z_{IN} = \frac{50 \times S_{11}}{2 \times (1-S_{11})} \tag{7}$$

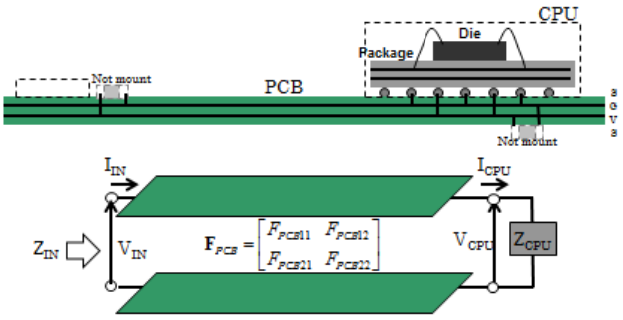


Fig. 8. CPU Load model extraction method.

B. *Work Flow to extract CPU load impedance*

These workflow are indicated in Fig9.

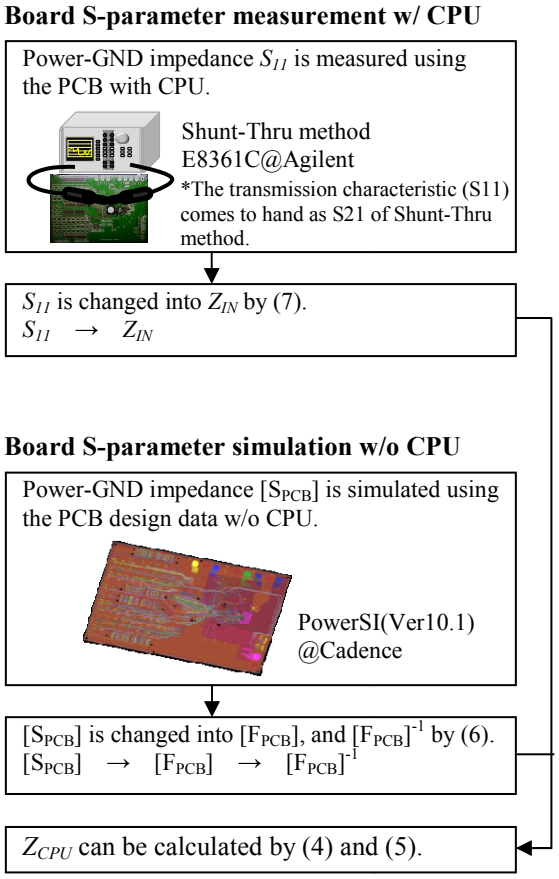


Fig. 9. Work flow for CPU load model with combination of simulation and measurement.

IV. Results and Discussion

A. *Calculation of Z_{IN}*

The PCB mounted CPU is shown in Fig. 10. Only CPU is mounted in this substrate. The measurement point is "Port1" near DC-DC converter. Measuring instruments is the network/impedance analyzer (product E8361C made by Agilent). The frequency range is 10[MHz]-1[GHz].

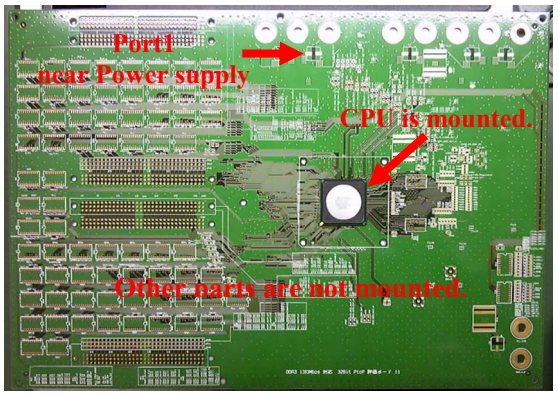


Fig. 10. PCB mounted only CPU for measurement.

S parameter(S_{21}) can be measured by the Shunt-Thru method. Z_{IN} calculated from this S_{21} of [$S_{Measure}$] is shown in Fig. 11-12. (S_{21} of the Shunt-Thru means the transmission characteristic (S_{11})).

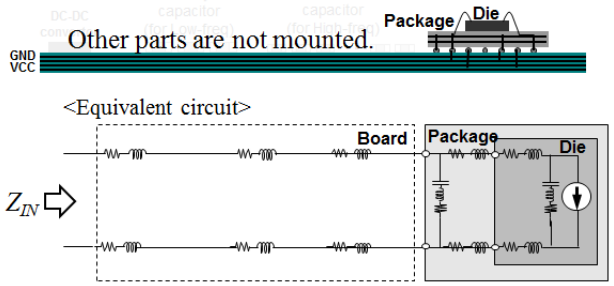


Fig. 11. Equivalent circuit of Z_{IN}

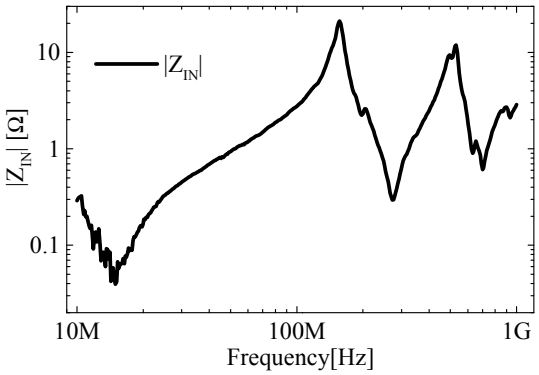


Fig. 12. Measurement result $|Z_{IN}|$

B. *Calculation of [F_{PCB}]*

[S_{PCB}] was calculated in the Power-GND impedance simulation using the PCB design data which does not mount any parts included CPU. The simulator is used PowerSI(Cadence) Ver10.1 (Fig. 13).

PCB is 4-layer through-hole. The layer structure is shown in TABLE 1.

Port1 is the same as the measurement point, and Port2 is set to the power and ground pads of CPU as far as possible from Port1 as shown in Fig. 14.

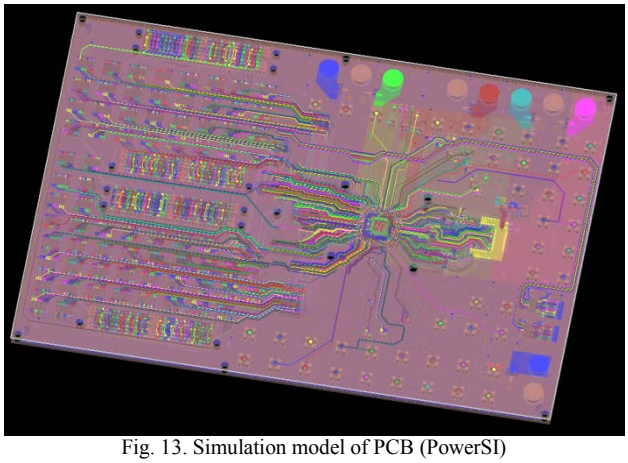


Fig. 13. Simulation model of PCB (PowerSI)

TABLE I
THE LAYER STRUCTURE OF THE PCB

L	S/V/G	Material	Thickness [mm]	Conductivity [S/m]	Dielectric Constant	Loss Tan
		Solder Resist	0.030		3.600	0.010
1	S	Copper +Plating	0.048	5.80E+07		
		P.P	0.110		4.600	0.016
2	G	Copper	0.035	5.80E+07		
		Core	1.130		4.600	0.016
3	V	Copper	0.035	5.80E+07		
		P.P	0.110		4.600	0.016
4	S	Copper +Plating	0.048	5.80E+07		
		Solder Resist	0.030		3.600	0.010

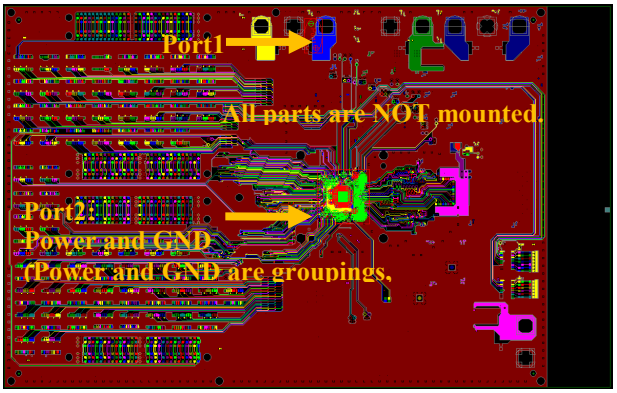


Fig. 14. Simulation Ports setting

Z_{PCB} calculated from S_{11} of $[S_{PCB}]$ is shown in Fig. 15-16, and it was changed into $[F_{PCB}]$ and $[F_{PCB}]^{-1}$ from this $[S_{PCB}]$ by (6).

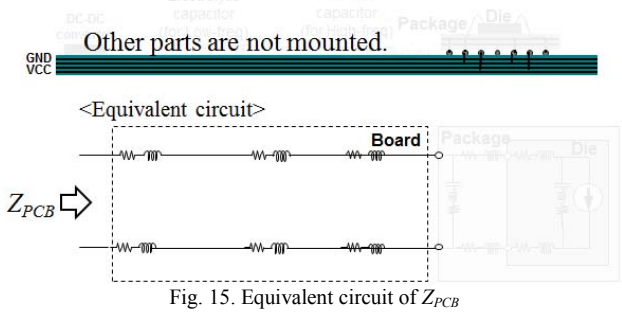


Fig. 15. Equivalent circuit of Z_{PCB}

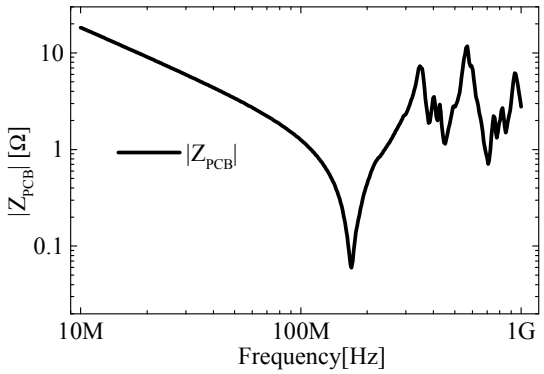


Fig. 16. Simulation result $|Z_{PCB}|$

C. *Calculation of Z_{CPU}*

The CPU load impedance (Z_{CPU}) is calculated using Z_{IN} of measurement and $[F_{PCB}]^{-1}$ of simulation by (4) and (5). This extracted result is shown in Fig. 17-18.

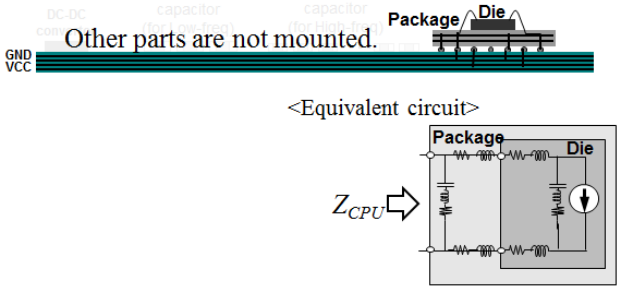


Fig. 17. Equivalent circuit of Z_{CPU}

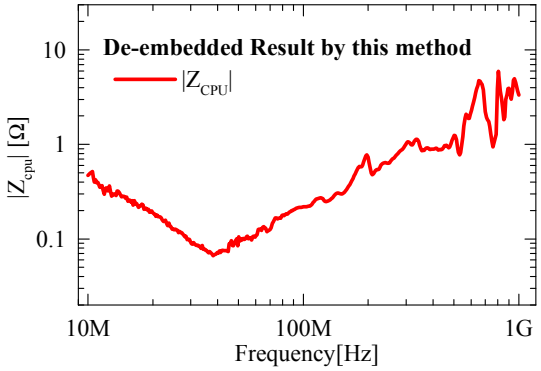


Fig. 18. Z_{CPU} obtained by this de-embedded method.

D. *Verification of extracted Z_{CPU}*

The extracted Z_{CPU} is applied to CPU part on Fig. 19 and the result Z_{IN} simulated is indicated on Fig. 20. To compare, Measurement result of Fig.12 is also shown on the same chart.

Z_{IN} using Z_{CPU} agrees very well with measurement result. This proves that it can be De-embedded CPU Load Model correctly by this method.

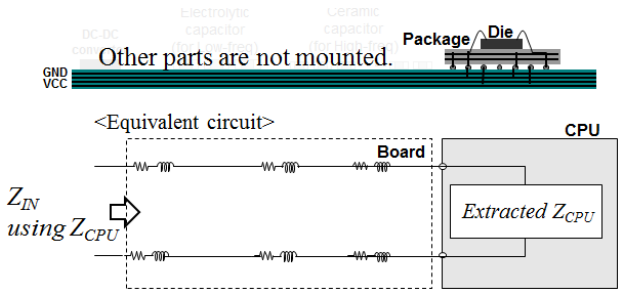


Fig. 19. Equivalent circuit of Z_{IN} using extracted Z_{CPU}.

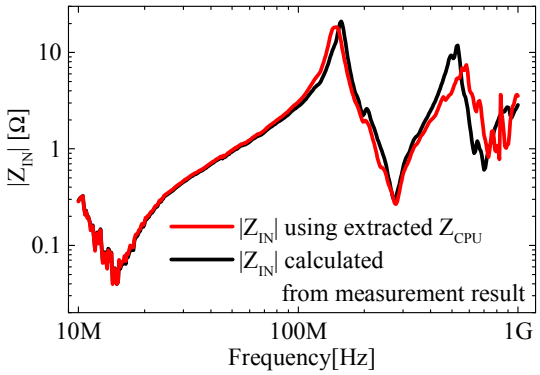


Fig. 20. Comparison of Z_{IN} using extracted Z_{CPU} ("Red") and Z_{IN} calculated from measurement result("Black").

E. *PDN Impedance using extracted Z_{CPU}*

The Power-GND impedance of Point A in Fig. 1 using PCB data and extracted Z_{CPU} is shown by the "green" line in Fig. 21. This impedance is equivalent to the "aqua" line using the CPU load model specially calculated from CPU design data. With the proposed method, CPU load model is successfully extracted with high accuracy.

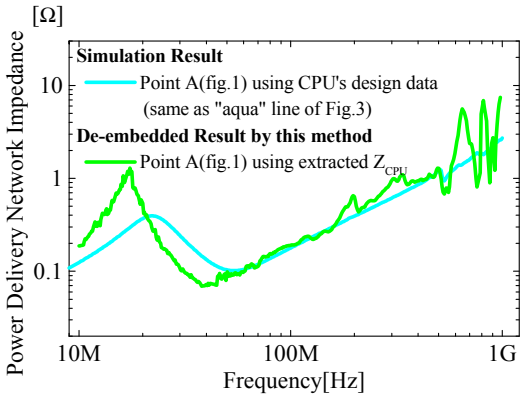


Fig. 21. PDN using extracted Z_{CPU}

As show in Fig. 18, the load model of CPU (Z_{CPU}) is rising by more than 40 MHz, and PDN is also rising in the same way by more than 40 MHz as shown in Fig. 21. This means that the inductance ingredient of CPU(especially Package in CPU) becomes dominant for more than 40 MHz of impedance.

In other words, there are no ways but CPU vender increases the capacity in CPU included Package to lower more than 40 MHz of impedance and it's ineffective that PCB designer arranges additional capacitors on PCB.

The conventional Power-GND impedance which has no CPU Load models and this Power-GND impedance using the CPU Load model extracted by this method are shown in Fig. 22. PCB designer didn't know even the frequency range to take a measure at the PCB design side, because there were no CPU Load models. With the proposed method, on the other hand, the CPU Load model was clearly defined. In case of this example, it's necessary that the PCB side to take the measure to lower PDN impedance in frequency range less than 40 MHz.

In particular, there is the sudden change impedance rise around 20MHz. This seems to depend on anti-resonance of PCB and CPU(especially Package). Therefore, PCB designer has to arrange some capacitors to lower impedance around 20MHz, avoid the signal line of around 20MHz from this PDN, and design the shape of Power and Ground plane without resonance 20MHz.

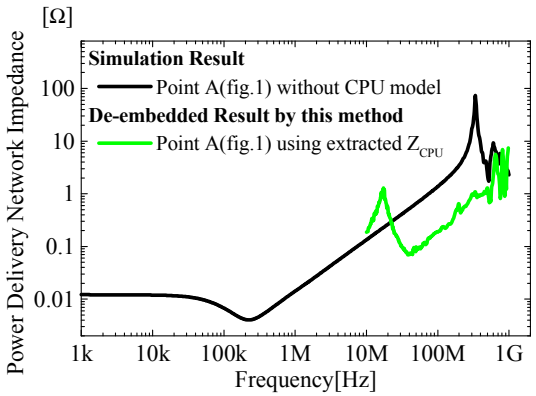


Fig. 22. PDN Impedance without CPU and with CPU load model extracted by this method.

V. Conclusions

A novel extraction method for CPU load impedance inside package including on-chip wiring has been successfully demonstrated. The method is simple yet accurate without special equipment. The method will contribute efficient design for CPU power delivery on PCB.

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