Self-Turn-on-Free 5V Gate Driving for 1200V Scaled IGBT

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***Abstract*—Negative biasing of the gate voltage in a scaled insulated gate bipolar transistor (IGBT) during the off-state was modeled and found to be effective against self-turn-on failures. The required self-turn-on-free criteria were verified experimentally.**

Keywords—scaled IGBT, self-turn-on, gate shielding layer

I. INTRODUCTION

This paper reports the modeling and demonstration of a self-turn-on-free 5V gate drive (V_{GE_th} = 1.7 V) for a 1200V scaled insulated gate bipolar transistor (IGBT), in which the MOS gate shielding layer prevents self-turn-on failures [1–3]. Since 2011, new IGBTs with a scaling (miniaturizing) factor of k = 3 have been proposed and fabricated [4–6]. The scaled IGBT features a high conduction current capability and a low gate drive voltage of 5V. A low gate drive voltage dramatically reduces the gate drive power in proportion to the square of the voltage swing; that is, by a factor of k^2. However, it has the disadvantage of self-turn-on failures due to switching noise, especially when driven at high dV_{CE}/dt [7, 8], because of the low gate threshold voltage. In this paper, we first analyze the gate shielding mechanism and propose gate voltage model for the planer gate IGBT. Then we demonstrate a shielding mechanism and present the criteria for a scaled trench gate IGBT that is free from self-turn-on failures.

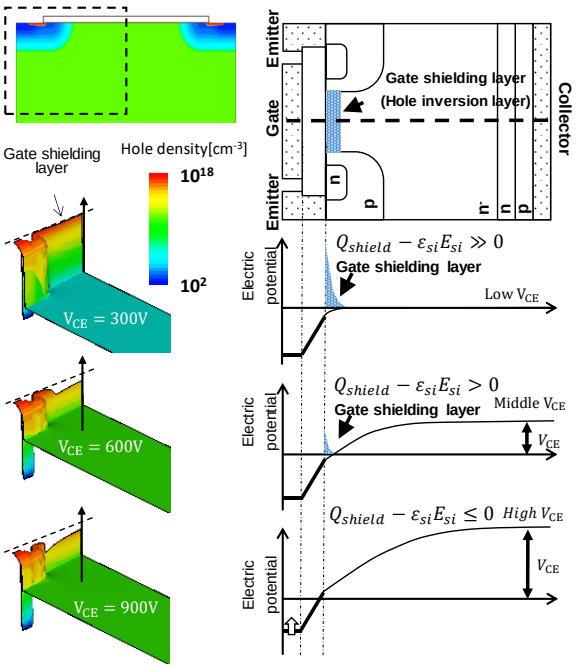


Fig. 1. TCAD simulation of a planar gate IGBT with a negative bias voltage and the electrostatic potential distribution in the device.

II. ANALYSIS OF THE MOS GATE SHIELDING MECHANISM

Off-state negative gate biasing has been employed for IGBT gate drives because it was believed that the negative voltage adds a margin to the gate threshold voltage, and thus

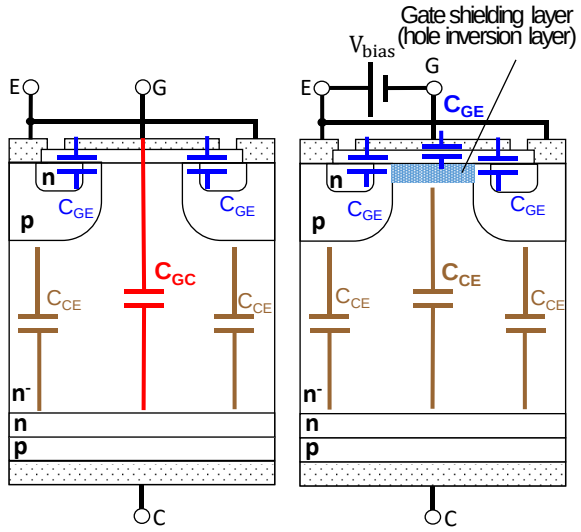


Fig. 2. Schematic view of parasitic capacitance in a planar IGBT with/without a gate shielding layer.

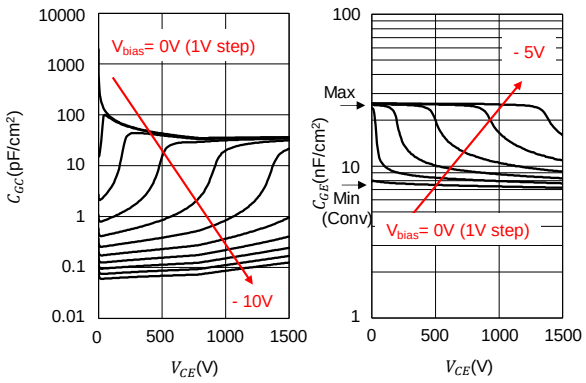


Fig. 3. TCAD simulation of C_{GC} and C_{GE} in a planar gate IGBT.

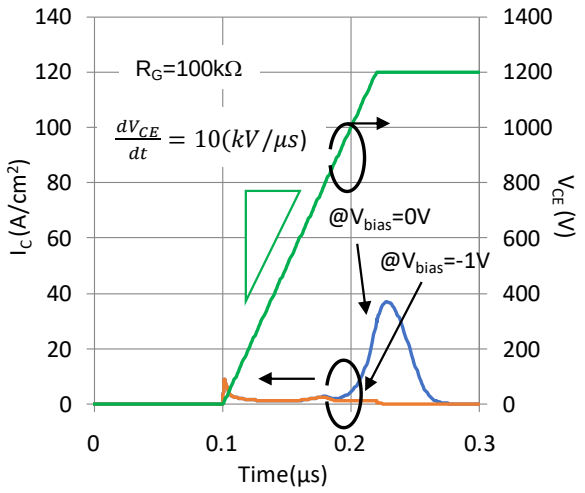


Fig. 4. TCAD simulation of the collector voltage and current waveforms during the off-state under high dV_{CE}/dt conditions for a planar gate IGBT.

reduces the self turn-on risk. Recently, it has been reported that a negative gate bias induces a shielding (hole inversion) layer beneath the MOS gate, so that the electric field when driven at high dV_{CE}/dt is completely terminated to the source/emitter voltage, and thus the MOS device is strongly protected from self-turn-on failures. However, the physics-based mechanism has not been explained or modeled.

A gate shielding layer appears with a negative gate bias at a low V_{CE}. This layer is removed at a high V_{CE} with the increase in the electric field in the N-base (N-drift) surface E_{Si}, and this was confirmed TCAD simulation (Fig. 1). The layer appears when the initial(V_{CE}=0V) shielding layer charge Q_{shield} is larger than the charge from V_{CE}. The shielding layer changes C_{GC}, C_{GE} and C_{CE}. C_{GC} changes in a part of C_{CE} and C_{GE} appears between the MOS gate and the N-base (N-drift) surface. As a result, C_{GC} becomes very small and C_{CE} and C_{GE} become large (Figs. 2 and 3). We used TCAD to simulate the waveforms at a very high dV_{CE}/dt for an IGBT driven at 10kV/us in the off-state (Fig. 4). Applying a negative gate bias of –1V dramatically reduced the self-turn-on current.

III. Gate Voltage Model in The Off-State

Gate voltage was modeled based on the shielding layer mechanism. When a shielding layer exists, V_{GE} can be expressed by the following equation, because C_{GE} is completely shielded by the shielding layer.

$$V_{GE}(Q_{shield} - \epsilon_{si}E_{si} > 0) = V_{bias} \quad (1)$$

where $Q_{shield} = \epsilon_{ox}E_{ox} = \epsilon_{ox}\frac{V_{bias}}{t_{ox}}$

When no shielding layer exists (Fig. 5), V_{GE} is expressed by the following equation, because C_{GC} and C_{GE} are connected in series between the collector and emitter terminals via the gate terminal.

$$\int_{V_{CE_th}}^{V_{CE}} C_{GC}dV_{CE} = \int_{V_{bias}}^{V_{GE}} C_{GE}dV_{GE}$$

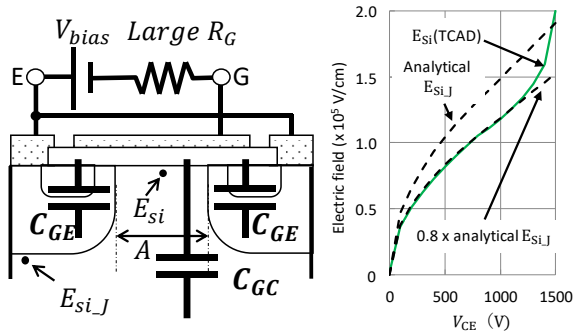


Fig. 5. Schematic of V_{GE} model of Eq. (2) and the electric field as a function of V_{CE} ($E_{si} = \alpha E_{si_J}$, $\alpha = 0.8$).

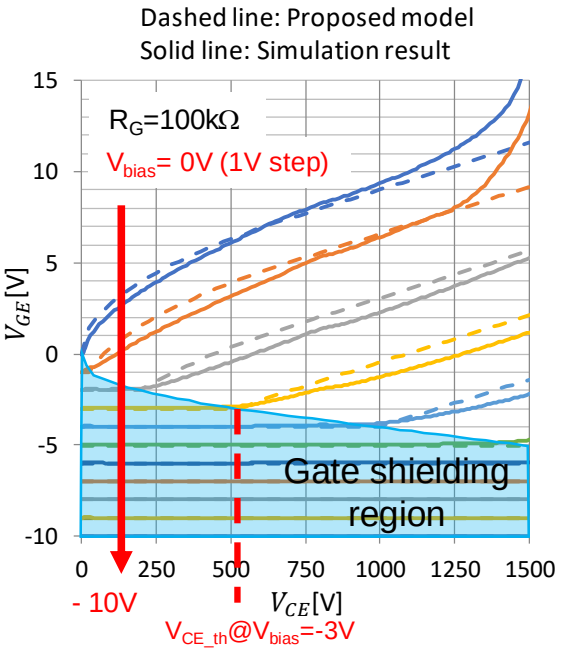


Fig. 6. Off-state V_{GE} calculated using the proposed model compared with the TCAD simulation results.

$$A(\epsilon_{si}E_{si} - Q_{shield}) = (V_{GE} - V_{bias})C_{GE}$$

$$V_{GE}(Q_{shield} - \epsilon_{si}E_{si} \le 0) = V_{bias} + \frac{A(\epsilon_{si}E_{si} - Q_{shield})}{C_{GE}} \quad (2)$$

where $E_{si} = \alpha E_{si_J} = \alpha\sqrt{\frac{2qN_BV_{CE}}{\epsilon_{si}}}$ or $\alpha\left(\frac{V_{CE}}{W_B} + \frac{qN_BW_B}{2\epsilon_{si}}\right)$

The V_{GE} calculated from the analytical model was compared with the V_{GE} from the TCAD simulation. The values for V_{GE} were in close agreement, confirming the accuracy of the analytical model (Fig. 6).

IV. Self-Turn-On-Free Criteria for The Scaled IGBT

The self-turn-on-free criteria for a scaled 1200V IGBT were confirmed experimentally. An IGBT with a gate drive voltage of 5V (k = 3) was used as the DUT because we assumed that a low V_{GE_th} of 1.7 V would facilitate self-turn-on failures (Fig. 7). Measurement of C_{GC} and C_{GE} confirmed the appearance and disappearance of the gate shielding layer (Fig. 8). C_{GC} decreased on applying a negative bias voltage

with a low V_{CE}. Conversely, C_{GE} increased on applying a negative bias voltage. The characteristics agreed with those from the TCAD simulation analysis (Fig. 3). The value of

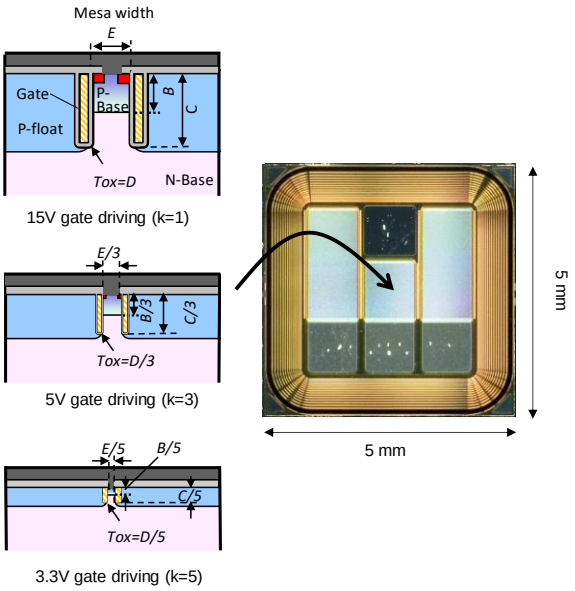


Fig. 7. Scaled IGBT and the fabricated 5V gate driving trench gate IGBT chip.

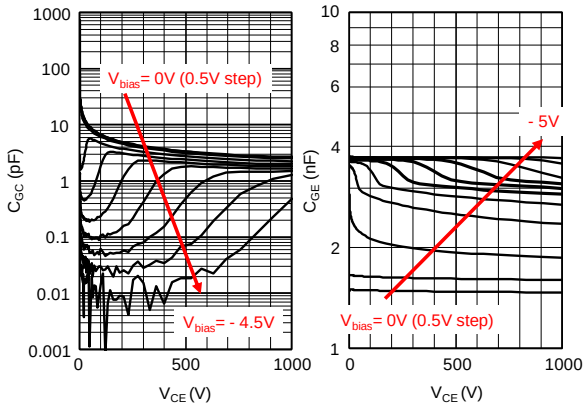


Fig. 8. Measured C_{GC} and C_{GE} for the 5V gate trench gate IGBT chip (C_{GC} was calibrated assuming that C_{GC} was 0F at V_{bias} = –5V).

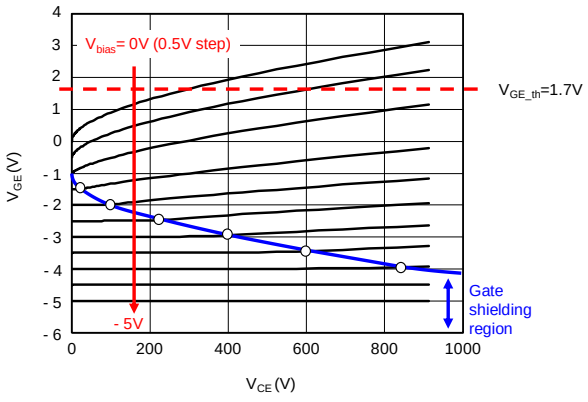


Fig. 9. Expected V_{GE} for the 5V gate driving IGBT chip from the measured C_{GC} and C_{GE} (Fig. 8).

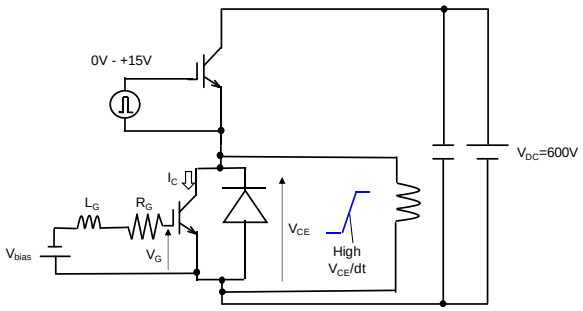


Fig. 10. Test circuit for self-turn-on-free driving (Inductive load and single pulse switching).

V_{GE} was obtained from C_{GC} and C_{GE} using the following equation.

$$V_{GE} = V_{bias} + \frac{\int_0^{V_{CE}} C_{GC} dV_{CE}}{C_{GE}} \quad (3)$$

The results of the TCAD simulation and the model generally agreed well (Figs. 6 and 9). The required V_{bias} of –1V was expected from Eq. 3.

We confirmed experimentally that the scaled IGBT operated free from self-turn-on-failures in a single pulse test. The gate resistance of the switching IGBT was 0Ω for a high dV_{CE}/dt of 25kV/μs (Fig. 10). Even under high impedance gate circuit conditions (L_G = 400nH and R_G up to 1kΩ), no self-turn-on failures occurred when applying a negative gate bias of –2V or below (Fig. 11). The difference from the expected value of V_{bias} is assumed to be due to the short expansion of the depression layer with the high dV_{CE}/dt.

We also tried self-turn-on-free driving with no V_{bias} to simplify the gate drive circuit. With L_G as low as 10nH, self-turn-on-free operation was established without a negative gate bias (Fig. 12). Thanks to the low impedance of the gate circuit, the charge on C_{GC} quickly discharged to the emitter terminal.

V. Conclusion

We found by modeling and by experiment that a negatively biased gate voltage was effective against self-turn-on failures. Simple yet accurate model equations were proposed and the results showed good agreement with the TCAD simulation. The model can be easily implemented in a SPICE device model (see Appendix), and the parameters can be easily extracted from measurement and the N-base structure. The self-turn-on-free criteria we obtained by experiment demonstrated that completely self-turn-on-free operation is possible with a negative V_{bias} even for a 1200V scaled IGBT with the gate driven at 5V. The practicality of a gate drive voltage at a CMOS logic level of 5 V shows the possibility of new functionality for gate drives using digital IoT/AI technology [9].

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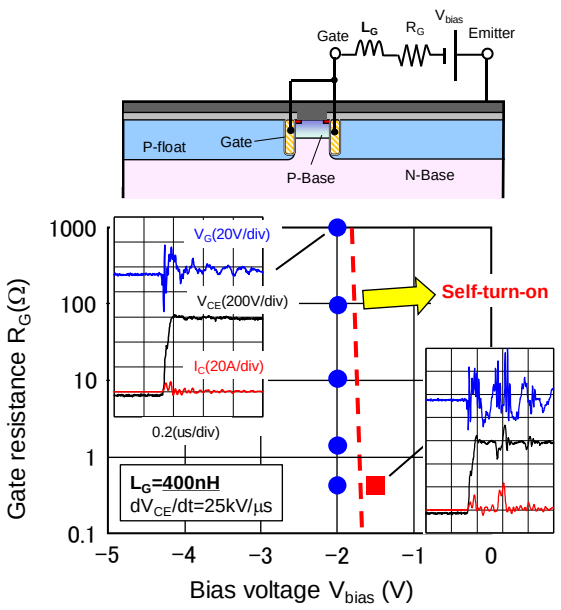


Fig. 11. Absolute criterion for self-turn-on-free driving for 1200V scaled trench gate IGBT and the waveforms.

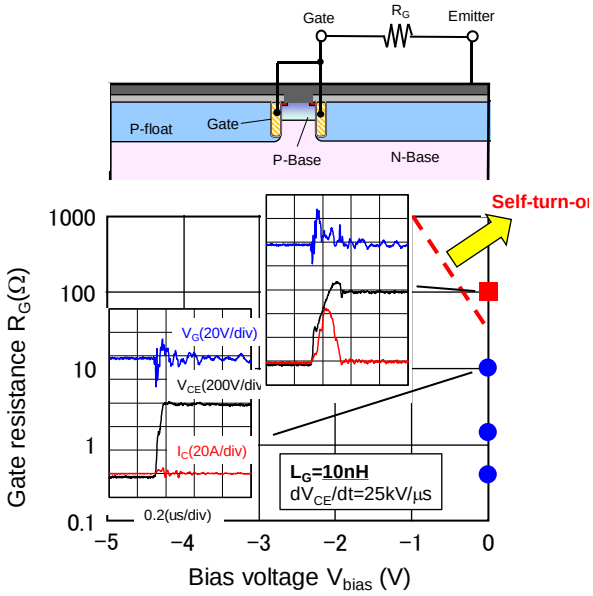


Fig. 12. Criteria for a low gate impedance for self-turn-on-free driving of a 1200V trench gate scaled IGBT and the waveforms.

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APPENDIX

We propose a configuration for the capacitances in the device for a SPICE device model (Fig. 13). The appearance and disappearance of the shielding layer is at the border of the capacitance value. The required V_{bias} is expressed by the following equation.

$$Required\ V_{bias} = \frac{\epsilon_{si} E_{si} t_{ox}}{\epsilon_{ox}} = \frac{\epsilon_{si} E_{si} A}{C_{GE_max} - C_{GE_conv}} \qquad (4)$$

This SPICE model is applicable to all MOS gate devices.

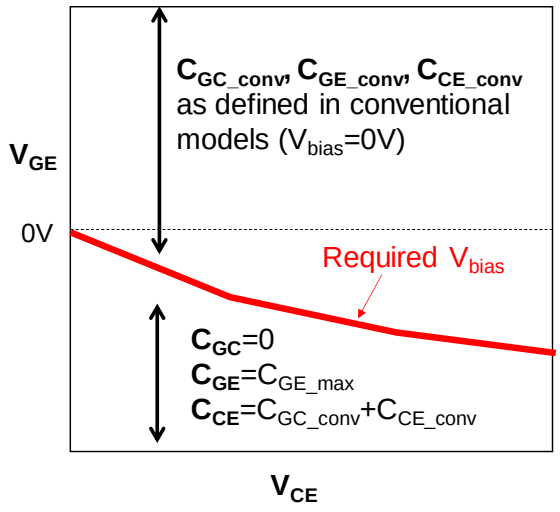


Fig. 13. Capacitance parameters for the SPICE device model from the gate shielding layer for MOS gate devices.