A Capture-Safety Checking Metric Based on Transition-Time-Relation for At-Speed Scan Testing*

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SUMMARY Test power has become a critical issue, especially for low-power devices with deeply optimized functional power profiles. Particularly, excessive capture power in at-speed scan testing may cause timing failures that result in test-induced yield loss. This has made capture-safety checking mandatory for test vectors. However, previous capture-safety checking metrics suffer from inadequate accuracy since they ignore the time relations among different transitions caused by a test vector in a circuit. This paper presents a novel metric called the Transition-Time-Relation-based (TTR) metric which takes transition time relations into consideration in capture-safety checking. Detailed analysis done on an industrial circuit has demonstrated the advantages of the TTR metric. Capture-safety checking with the TTR metric greatly improves the accuracy of test vector sign-off and low-capture-power test generation.
key words: at-speed testing, ATPG, IR-drop, test power reduction, low power test

1. Introduction

Power reduction, in addition to timing closure and area minimization, is now mandatory for LSI designs. Various techniques, such as clock gating, multi-threshold voltages, power domain portioning, dynamic voltage scaling, etc, have been proposed for reducing functional power. With these techniques, designers can achieve a low functional power level. However, low functional power does not mean low test power. In fact, test power can be several times higher than functional power [1] due to high fault/block parallelism and non-functional clocking used during testing for higher test efficiency. Excessive test power may cause severe problems, especially in at-speed scan testing.

Scan testing has two modes, namely shift and capture. Shift is for loading test stimuli and unloading test responses through scan chains, while capture is for capturing test responses from the circuit-under-test. At-speed scan testing is usually achieved by using the Launch-On-Capture (LOC) clocking scheme shown in Fig. 1, which is widely used in the industry due to its simple physical implementation.
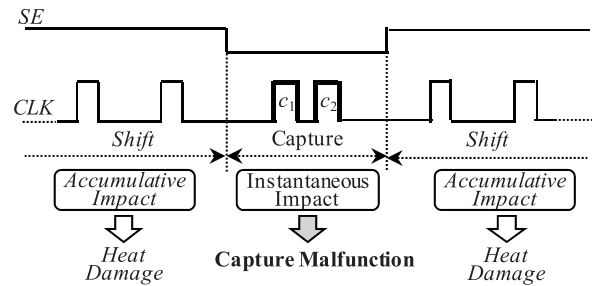
Fig. 1 Test power issues in at-speed scan testing.

Due to the large number of shift cycles, the accumulative impact of shift power may manifest itself as excessive heat, causing damage to packages or dies. Fortunately, several successful approaches, notably scan segmentation, have been proposed and applied in the industry for shift power reduction [2].

On the other hand, there are only two capture clock cycles in the LOC scheme, which means that the accumulative impact of capture power is negligible. However, the instantaneous impact of capture power may cause capture malfunction [3], [4], as described below:

In the LOC scheme illustrated in Fig. 1, there is a launch cycle (C_1) and a capture cycle (C_2). If excessive switching activity occurs in the launch cycle, C_1, excessive IR-drop may occur, leading to excessive path delay and ultimately timing failures in the capture cycle. That is, unexpected test responses may be captured in C_2, even though the circuit-under-test is defect-free and functionally operational. Particularly in the testing of high-speed devices, even a small increase in delay due to excessive IR-drop may cause capture malfunction, resulting in test-induced yield loss [7].

In order to tackle the problem of capture malfunction, it is critical to check whether or not a test vector may cause excessive switching activity in the launch cycle. In other words, capture-safety checking needs to be conducted, either in test vector sign-off or in test generation. Capture-unsafe test vectors need to be discarded or rescued by various low-capture-power techniques using DFT, ATPG, and test vector modification [5]–[11]. It is clear that the effectiveness and efficiency of test vector sign-off and low-capture-power test generation are determined by the accuracy of capture-safety checking.

Previous capture-safety checking metrics can be classified from spatial and temporal perspectives, as illus-
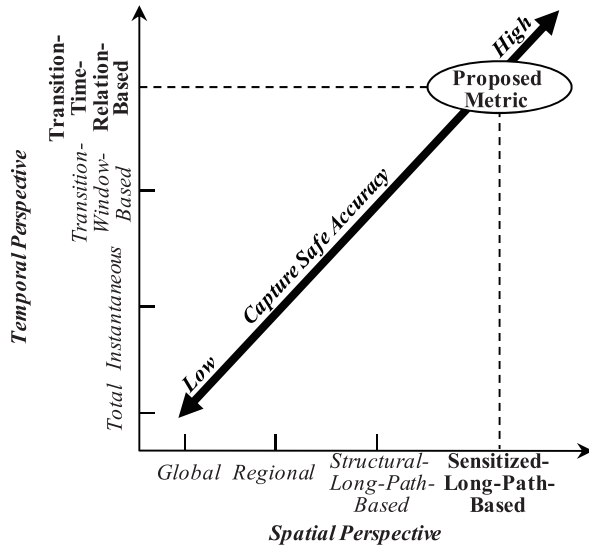
Fig. 2 Classification of capture-safety checking metrics.

trated in Fig. 2. From the spatial perspective, capture-safety checking metrics can be classified as (S1) *global* (the switching activity of the entire circuit is checked) [9]–[11], (S2) *regional* (the switching activity in specific regions is checked) [8], (S3) *structural-long-path-based* (the switching activity around structurally long paths is checked) [12], and (S4) *sensitized-long-path-based* (the switching activity around sensitized long paths is checked) [13]. From the temporal perspective, capture-safety checking metrics can be classified as (T1) *total* (the switching activity for the whole launch cycle is checked) [9]–[11], (T2) *instantaneous* (peak or instantaneous switching activity is checked) [8], and (T3) *transition-window-based* (switching activity in the transition window is checked) [14].

Generally, metrics that focus on the switching activity around sensitized long paths are more accurate than others. The reason is that sensitized long paths are very susceptible to IR-drop-induced delay increase. In other words, the delay of an on-path gate, G, increases when its supply voltage drops due to the transitions occurring at its neighboring gates. However, from the temporal perspective, if the transition at a neighboring gate occurs after the transition of G, it will not impact the supply voltage of G. That is, a late transition will not impact an early transition. Clearly, this transition time relation is important for the accuracy of capture-safety checking. However, none of the previous capture-safety checking metrics takes transition time relations into consideration.

In this paper, we propose a novel capture-safety checking metric based on *transition time relation* (*TTR*). The TTR metric focuses on long sensitized paths (i.e., paths whose lengths exceed a threshold) and evaluates the delay increase along each long sensitized path based on the transition time relation. As shown in Fig. 2, the proposed metric has higher determination accuracy compared to previous metrics.

In order to take transition time relations into consideration, the proposed metric first identifies sensitized long paths and their neighboring node (logic gate) set, where nodes in the set are located close together and share a power supply net. Then, it assesses the delay increase of each sensitized long path using the *TTR metric*, which is based on those transitions that occur earlier than any transition at each on-path node. Detailed evaluative experiments on an industrial circuit demonstrated the accuracy and scalability of the TTR metric for capture safety checking.

The rest of this paper is organized as follows. Section 2 describes the background; the proposed transition time relation based metric is described in Sect. 3. Experimental results are shown in Sect. 4, and conclusions are in Sect. 5.

2. Background

2.1 Importance of Capture-Safety Checking

Capture-safety checking is conducted in order to determine whether a test vector is capture-safe or capture-risky. Obviously, the accuracy of capture-safety checking is extremely important. If a test vector is optimistically classified as capture-safe and used in production test, a defect-free chip may be wrongly rejected, resulting in yield loss. On the other hand, if a test vector is conservatively classified as capture-risky and discarded, fault coverage and/or test vector count will be affected.

Generally, capture-risky test vectors identified by capture-safety checking can be discarded or rescued by DFT, ATPG, and test vector modification [5]–[11]. Figure 3 illustrates an example of the complete capture-safe test generation flow that consists of capture-safety checking, test vector modification, and low-power ATPG, as follows:
① *Capture-Safety Checking -I*: This is the first capture-safety check, which is conducted for given test vectors generated by a conventional detection-oriented ATPG.
② *Test Vector Modification*: This modifies test vectors so as to reduce as much capture power in the launch cycle as possible. Test vector modification targets only the capture-risky test vectors identified by the first capture-safety check.
③ *Capture-Safety Checking -II*: This is the second capture-safety check, which is conducted on the test vectors modified by the previous step.
④ *Low-Power ATPG*: This dedicated ATPG generates test vectors that achieve both fault detection and low-capture power. Many commercial low-power ATPG tools are available. Since low-power ATPG has constraints for low-power in addition to fault detection, the computation time is always expensive. If capture-safety checking is included in ATPG implementation in order to always generate capture-safe vectors, the computation time becomes more expensive. Therefore, low-power ATPG must be conducted for only few number of faults undetected by capture-safe vectors previously checked.

Note that the test vector modification step consists of X-identification [15] and X-filling [16], [17]. In the flow
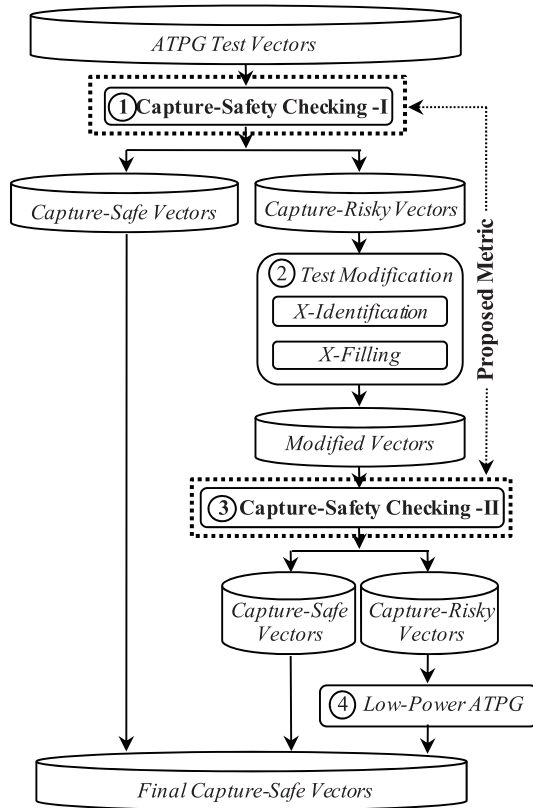
Fig. 3 Example of capture-safety test generation flow.

shown in Fig. 3, these techniques are applied to only capture-risky test vectors. This improves the effectiveness of capture power reduction, since more *X*-bits can be made available for capture-risky vectors. On the other hand, while low-capture-power ATPG [7] is helpful for reducing capture power, its run time is long and the test vector count is large if it must be performed for a large number of faults. Fortunately, in the flow of Fig. 3, the low-capture-power ATPG only targets faults undetected by capture-safe vectors identified by capture-safety checking. Therefore, there is no significant increase in run time or test vector count. From this test generation flow, it is apparent that capture-safety checking indeed plays an important role.

2.2 Previous Metrics

Previous capture-safety checking metrics can be classified from spatial and temporal perspectives. In the following paragraphs, we review previous metrics and highlight their problems.

Spatial-Perspective-Based Classification: There are four types of metrics for capture-safety checking from the spatial perspective, as described below:

(S1) *Global*: The switching activity of the entire circuit is checked to determine capture safety [8]–[11]. Since capture malfunction is a local phenomenon that usually occurs at the endpoint of a sensitized long path, the global metric may not be able to provide an accurate determination [8].

(S2) *Regional*: The switching activity in some specific regions is checked to determine capture safety [8]. Although more accurate than the global metric, the regional metric only checks switching activity throughout the entire region instead of focusing on those paths that are most susceptible to the effects of IR-drop.

(S3) *Structural-Long-Path-Based*: The switching activity around structural long paths is checked to determine capture safety [12]. While this metric is more accurate than the global or regional metrics, if a path is not sensitized, there is no need to consider the path [8]. Note that structural long paths are not always sensitized.

(S4) *Sensitized-Long-Path-Based*: The switching activity around each sensitized long path is checked to determine capture safety [13]. From the spatial perspective, this is the most accurate approach since it directly addresses the real cause of capture malfunction, i.e. excessive switching activity around long sensitized paths. The proposed metric in this paper is also a sensitized-long-path-based metric.

Temporal-Perspective-Based Classification: There are four types of metrics for capture-safety checking from the temporal perspective, as described below:

(T1) *Total*: The total switching activity for the whole launch cycle (C_1 in Fig. 1) is used to determine capture safety [8]–[11]. For example, the total number of transitions (toggle rate) or weighted transitions (WSA: weighted switching activity) can be calculated for this purpose.

(T2) *Instantaneous*: The peak switching activity in the launch cycle is used to determine capture safety [8]. For example, the maximum number of transitions (toggle rate) or weighted transitions (WSA) at a certain point in time can be used.

(T3) *Transition-Window-Based*: The switching activity in the transition window is used to determine capture safety. The transition window is the period in which all transitions occur in the launch cycle. For example, switching cycle average power (SCAP) has been proposed [14]. Although more accurate than a total or instantaneous metric, the transition-window-based metric is usually time-consuming, since timing-based simulation is needed to determine the transition window.

2.3 Drawbacks of Previous Metrics

From the spatial perspective, switching activity around sensitized long paths is the most important consideration; from the temporal perspective, however, the two following problems exist:

(1) *Ignorance of Transition Time Relations*: None of the previous capture-safety checking metrics takes transition time relations into consideration. The SCAP metric [14] considers the time window in which all transitions occur, but time relations among the transitions in the window are not considered. As shown in Fig. 4, transition time relations are indispensable for more accurately assessing the impact of IR-drop-induced delay increase. For example, $g_4 \rightarrow g_5 \rightarrow g_6$ is a sensitized long path in Fig. 4. Now
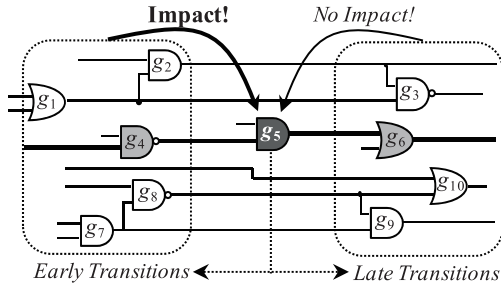
Fig. 4 Impact of transition time relations.

consider the on-path node g_5, and suppose that $g_1 \sim g_4$ and $g_6 \sim g_{10}$ are located close together in the layout and share the same power supply net with g_5. Previous metrics consider transitions at all of these nodes when assessing the delay increase at g_5 [8]–[11]. However, transitions at g_1, g_2, g_4, g_7, and g_8 occur earlier, while transitions at g_3, g_6, g_9, and g_{10} occur later than any transition at g_5. Obviously, only the transitions at g_1, g_2, g_4, g_7, and g_8 may potentially delay at g_5. In short, transition time relations need to be factored in to achieve higher accuracy in capture-safety checking.

(2) *Low Scalability*: Although IR-drop-analysis-based capture-safety checking is accurate, it is computationally expensive, making it hard to apply to large circuits or a large number of test vectors. Similarly, while the transition-window based SCAP metric is relatively accurate, it still requires timing-accurate simulation.

2.4 Contributions

This paper proposes a novel capture-safety checking metric, called the ***Transition-Time-Relation-based*** (***TTR***) metric. The advantages of the TTR metric are as follows:

• **High Accuracy**: The TTR metric checks the switching activity around sensitized long paths, which is more advantageous than previous metrics from the spatial perspective. The TTR metric also takes transition time relations into consideration when assessing the impact of neighboring switching activity on the delay increase of a sensitized long path, which is more advantageous than other metrics from the temporal perspective. As a result, the TTR metric can achieve higher accuracy in capture-safety checking.

• **High Scalability**: The TTR metric is based on logic simulation. Therefore, it is more scalable than IR-drop analysis-based metrics as well as metrics requiring timing accurate simulation results [14].

3. TTR-Based Capture-Safety Checking

3.1 Overview of Proposed Capture-Safety Checking

In order to obtain accurate capture-safety checking results from both the spatial and temporal perspectives, the proposed capture-safety checking consists of four techniques (depicted in Fig. 5). As illustrated in Fig. 5, capture-safety checking requires the layout data, netlist, and test vectors.
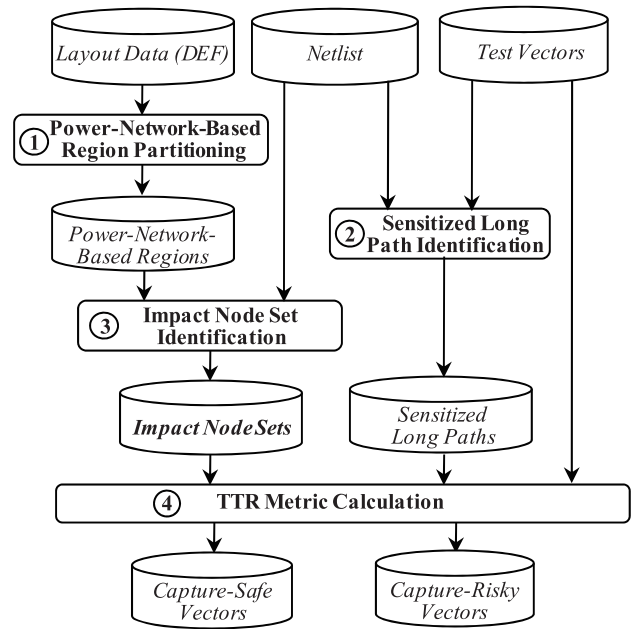

Fig. 5 Flow of TTR-based capture-safety checking.

Finally, the test vectors are classified as capture-safe and capture-risky vectors. Each technique in Fig. 5 is summarized below.

① **Power-Network-Based Region Partitioning**: This is a pre-processing step where a circuit is partitioned into small regions based on power supply network design and layout information (DEF). Each region consists of nodes that are located close together and share a power supply net.

② **Sensitized Long Path Identification**: All paths that are sensitized and longer than a threshold are identified. From the spatial perspective, such sensitized long paths are the most susceptible to excessive IR-drop.

③ **Impact Node Set Identification**: The set of impact nodes that significantly affect the IR-drop of a sensitized long path's on-path node is identified for each on-path node. These impact nodes are identified from related power-network-based regions in order to improve accuracy from the spatial perspective.

④ **TTR Metric Calculation**: A ***TTR value*** is calculated for a test vector based on the impact node set for each on-path node of every sensitized long path. This *TTR* value is used to determine the capture-safety of the test vector. Since transition time relations are considered when assessing the switching activity around each sensitized long path, TTR-based capture-safety checking can achieve higher accuracy than previous metrics.

3.2 Power-Network-Based Region Partitioning

In order to assess IR-drop on a node for capture-safety checking, it is necessary to identify all other nodes that have significant impact on that node. Generally, if two nodes are located close together and share a power supply net, the transition at one node (the *aggressor*) will significantly affect the
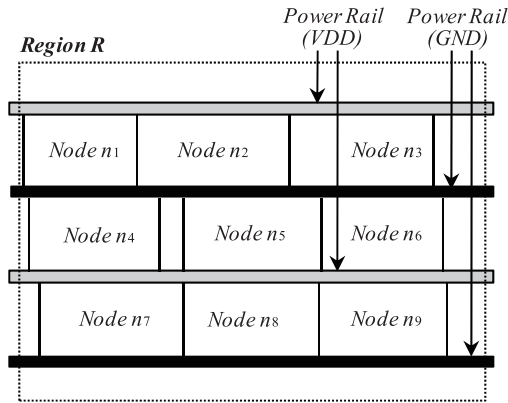
Fig. 6 Power-network-based region.

Sensitized Long Paths: P_1, P_2, P_3
Power-Network-Based Regions: $R_1 \sim R_6$
Primary Regions: $PR_1 \sim PR_4$
On-Path Node: ○
Off-Path-Primary Node: ●
Off-Path-Non-Primary Node: ⬚

Fig. 7 Primary regions and various types of nodes.

other node (the *victim*) in terms of IR-drop.

Therefore, we partitioned a circuit into small regions, called ***power-network-based regions***, where each consisting of nodes that are located close together and share a power supply net. Ideally, the region size must be determined by circuit level simulation such as SPICE. However, it is too expensive to conduct SPICE simulation for all gates in a large industrial circuit.

In our experiments, we partition a circuit so that each region consists of approximately 10 nodes, because each gate is surrounded by about 10 gates in a general layout design. Therefore, each node shares the same nearby power rail and each gate directly affect each other in terms of IR-drop. Note that this partitioning only needs to be conducted once as pre-processing.

Figure 6 shows an example of a power-network-based region, R, which consists of nine nodes. It is clear that if, for example, the IR-drop impact at n_5 needs to be assessed, it is only necessary to take the transitions occurring at n_1, n_2, n_3, n_4, n_6, n_7, n_8, and n_9 into consideration.

3.3 Sensitized Long Path Identification

In the TTR metric, we identify the sensitized long paths of a test vector as target paths for capture-safety checking. That is, we check the switching activity around such target paths to determine the capture-safety of the test vector. This is because unsensitized or short paths are unlikely to cause capture malfunction even if there is excessive switching activity around those paths. Whether or not a path is long is determined by a designer-specified threshold. In our experiments, we used the efficient path extraction technique in [18], which allowed us to obtain sensitized paths in descending order of path length in a relatively short amount of time. In addition, we used 55% of the length of structurally longest path as the threshold.

3.4 Impact Node Set Identification

As described in Sect. 2.2, the transitions occurring in close physical proximity to a particular node do not necessarily
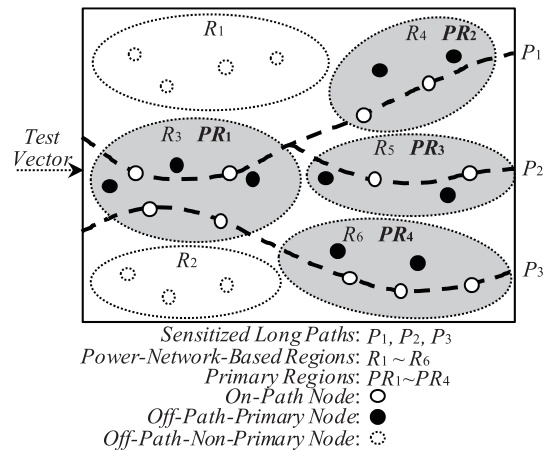
have a significant impact on the delay increase of the node. In other words, spatial accuracy alone is not enough to guarantee accurate capture-safety checking; temporal accuracy is also required. For this reason, we obtained the ***TTR impact node set***, which takes transition time relations into consideration.

First, ***primary regions*** are identified from power-network-based regions. A primary region is a region that passes through at least one sensitized long path. In addition, an ***off-path-primary node*** is an off-path (*with respect to a sensitized long path*) node that exists in a primary region. An example is shown in Fig. 7, where $P_1 \sim P_3$ are sensitized long paths and $PR_1 \sim PR_4$ are primary regions among power-network-based regions $R_1 \sim R_6$.

Next, in order to take transition time relations into consideration, the ***impact node set*** for an on-path node, v (denoted as $INS(v)$), is defined as the set of all nodes whose transitions occur earlier than the transition on the on-path node. There are two approaches to determining transition time relations: a static approach that compares distances from flip-flops (sources) to nodes (destinations), and a dynamic approach that uses timing-accurate logic simulation. Generally, the static approach yields accurate enough results within a reasonable computation time.

An example is shown in Fig. 8, where the target on-path node is n_2. If the lengths of nodes n_1, p_1, p_2, p_3, and p_4 from flip-flops are shorter than that of n_2, $INS(n_2)$ is $\{n_1, p_1, p_2, p_3, p_4\}$. By considering only those nodes whose transitions have impacts on n_2 while excluding those nodes whose transitions have no impact on n_2, higher accuracy can be expected in assessing the delay increase at n_2.

3.5 TTR Metric Calculation

The proposed metric calculates the TTR value for each test vector. For this purpose, three types of impact factors (namely *node impact factor* (*IFnode*), *primary-region impact factor* (*IFprimary_region*), and *path impact factor* (*IFpath*)) need to be calculated first, as follows:

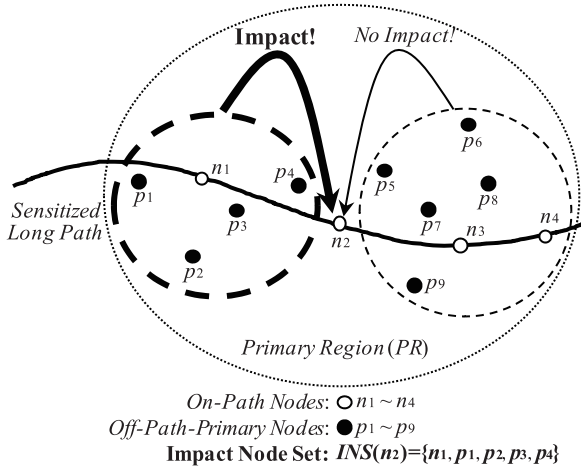• **Node Impact Factor**: In order to assess the impact of the

On-Path Nodes: $\bigcirc n_1 \sim n_4$
Off-Path-Primary Nodes: $\bullet\, p_1 \sim p_9$
Impact Node Set: $INS(n_2) = \{n_1, p_1, p_2, p_3, p_4\}$

Fig. 8 Impact node set.

nodes in a primary region (PR_j) on an on-path node, (n_i), the node impact factor for node n_i in primary region PR_j (denoted as $IF_{node}(n_i, PR_j)$) is defined as follows:

$$IF_{node}(n_i, PR_j)$$

$$= \frac{\sum_{1}^{k_i} (\#Fout + 1) \text{ for switching nodes in } INS(n_i)}{\sum_{1}^{m} (\#Fout + 1) \text{ for all nodes in } PR_j}$$

where #*Fout* is the fanout count of a node, k_i is the number of nodes in $INS(n_i)$, and m is the number of nodes in PR_j. Clearly, $IF_{node}(n_i, PR_j)$ is the weighted switching activity of the nodes in $INS(n_i)$ divided by the total weight (fanout count + 1) for all nodes including switching and non-switching ones in PR_j. As a result, transition time relations are taken into consideration.

• **Primary-Region Impact Factor**: Node impact factor values for all nodes in a primary region can be summed up for each sensitized long path in order to assess the primary region's impact on the sensitized long path. The primary-region impact factor for primary region PR_j and the sensitized long path P_k (denoted as $IF_{primary\_region}(PR_j, P_k)$) is defined as follows:

$$IF_{primary\_region}(PR_j, P_k) = \sum_{i=1}^{m} IF_{node}(n_i, PR_j)$$

where m is the number of on-path nodes for each sensitized long path in primary region PR_j.

• **Path Impact Factor**: The sum of the primary-region impact factor values of every primary region for a sensitized long path is divided by the length of the path for the purpose of normalization. The path impact factor for sensitized long path P_k (denoted as $IF_{path}(P_k)$) is defined as follows:

$$IF_{path}(P_k) = \frac{\sum_{j=1}^{q} IF_{primary\_region}(PR_j, P_k)}{Length(P_k)}$$

where q is the number of primary regions that the target sensitized long path P_k passes through, and $Length(P_k)$ is the length of P_k (the number of its on-path nodes).

An example for calculating these impact factors is shown in Fig. 8. Suppose that the fanout count of every node is 2, impact node sets for n_1, n_2, n_3, n_4 are $INS(n_1) = \{p_1\}$, $INS(n_2) = \{n_1, p_1, p_2, p_3, p_4\}$, $INS(n_3) = \{n_1, n_2, p_1, p_2, p_3, p_4, p_5, p_7, p_9\}$, and $INS(n_4) = \{n_1, n_2, n_3, p_1, p_2, p_3, p_4, p_5, p_6, p_7, p_8, p_9\}$. Also suppose that transitions occur at n_1, n_2, n_3, n_4, p_1, p_3, p_5, p_7, p_9, and that there is only one primary region. Based on the above definitions, $IF_{node}(n_1, PR) = 3/39$, $IF_{node}(n_2, PR) = 9/39$, $IF_{node}(n_3, PR) = 21/39$, and $IF_{node}(n_4, PR) = 24/39$. Furthermore, $IF_{primary\_region}(PR, P) = 57/39$, and $IF_{path}(P) = 57/156$.

• **TTR Value**: Although a test vector may sensitize more than one long path, the sensitized long path with the largest IF_{path} determines the capture-safety of the test vector. Therefore, in order to check capture-safety for a test vector, v, the *TTR* value (denoted as $TTR(v)$) is defined as follows:

$$TTR(v) = \text{Max}\{IF_{path}(P_1), \ldots, IF_{path}(P_r)\}$$

where $P_1, P_2, \ldots,$ and P_r are sensitized long paths under test vector v.

In capture-safety checking, the TTR value of a test vector is calculated and compared with a threshold to determine whether or not the test vector is capture-safe. The threshold can be set based on an arbitrary value. If transitions simultaneously occur at all nodes of a sensitized long path, its TTR value is 1. For example, the threshold can be set as 10% of the worst value. This is similar to the general threshold of power budget and delay slacks in the design phase. The time complexity of calculating the TTR value of a test vector is $O(m)$, where m is the number of long paths sensitized by the test vector.

4. Experimental Results

We implemented the proposed TTR metric using the C programming language, and conducted detailed analysis experiments on one industrial circuit. This circuit was synthesized using Design Compiler®, and was placed and routed using IC-Compiler® with the SAED_EDK90 nm library. We synthesized it with and without an 8X compression environment. We evaluated the proposed method in the two different environments (without compression: 809,310 gates/99,867 FFs; with compression: 812,354 gates/99,815 FFs). We used a workstation (Dual-Core AMD Opteron™: 2.8 GHz/16 GB) for experiments.

In order to obtain the golden result against which the proposed TTR metric was to be evaluated, we first conducted IR-drop analysis with PrimeRail® and obtained the exact delay for each sensitized long path by using PrimeTime®. Test vectors were then sorted based on path delay increases and path lengths, and the worst N test vectors were treated as capture-risky test vectors ($N = 5$, 10,

Table 1   Results of correct determinations (without compression).

	# Correct Risky Det.				Correct Det. Ratio			
	TTR	WSA			TTR	WSA		
		60%	65%	70%~		60%	65%	70%~
Worst 5	5	1	1	0	100%	20%	20%	0%
Worst10	10	1	1	0	100%	10%	10%	0%
Worst20	19	4	2	0	95%	20%	10%	0%

Table 2   Pessimistic and optimistic ratio (without compression).

	Pessimistic Ratio				Optimistic Ratio			
	TTR	WSA			TTR	WSA		
		60%	65%	70%~		60%	65%	70%~
Worst 5	87%	99%	97%	100%	0%	80%	80%	100%
Worst10	74%	99%	97%	100%	0%	90%	90%	100%
Worst20	51%	96%	95%	100%	5%	80%	90%	100%

Table 3   Correct risky determinations (with compression).

	# Correct Risky Determinations				
	TTR	WSA			
		60%	70%	80%	90%
Worst 5	4	5	3	1	1
Worst10	9	10	8	2	1
Worst20	18	20	18	3	2

Table 4   Ratio of correct determinations (with compression).

	Correct Determination Ratio				
	TTR	WSA			
		60%	70%	80%	90%
Worst 5	80%	100%	60%	20%	20%
Worst10	90%	100%	80%	20%	10%
Worst20	90%	100%	90%	15%	10%

Table 5   Pessimistic ratio (with compression).

	Pessimistic Ratio				
	TTR	WSA			
		60%	70%	80%	90%
Worst 5	94%	99%	99%	99%	96%
Worst10	86%	99%	99%	98%	96%
Worst20	72%	99%	99%	97%	93%

Table 6   Optimistic ratio (with compression).

	Optimistic Ratio				
	TTR	WSA			
		60%	70%	80%	90%
Worst 5	20%	0%	40%	80%	80%
Worst10	10%	0%	20%	80%	90%
Worst20	10%	0%	10%	85%	90%

20; called "Worst 5", "Worst 10", and "Worst 20" in Tables 1 and 2). These capture-safety checking results were used as the golden result to assess the accuracy of the proposed TTR metric and the widely-adopted WSA metric. The WSA metric checks capture safety by calculating the value of weighted transitions for the entire circuit in the launch cycle and comparing it with a threshold, which is a percentage of the maximum WSA. In our experiments, we used 60%, 70%, 80% and 90% as threshold percentages.

Table 1 shows the number of correct capture-risky determinations and the ratios of correct determinations by the TTR and WSA metrics. 2,231 transition fault test vectors with 98.5% fault coverage were generated using TetraMAX®. All sensitized paths whose lengths were greater than 55% of the longest structural path were identified [12] as sensitized long paths. The total number of such paths was 28,645. Note that the threshold of the TTR metric is set to 15% of the worst TTR value. From Table 1, it is apparent that the proposed TTR metric achieved much higher accuracy than the WSA metric with various thresholds. Particularly, the five capture-risky test vectors in the golden results for the "Worst 5" cases are more likely to be actual capture-risky test vectors than those of the "Worst 10" and "Worst 20" cases. It is clear that five of these capture-risky test vectors were also correctly identified by the TTR metric.

Table 2 shows both pessimistic and optimistic ratios. The pessimistic ratio is the percentage of test vectors incorrectly identified as capture-risky. For example, when TTR metric determines 39 vectors as capture-risky and only 5 vectors are actually capture-risky, 34 vectors are pessimistically identified as capture-risky. The percentage of the pessimistic ratio is obtained as 0.87 (34/39) which is corresponding to Worst 5 for TTR in Table 2. For the experiments without compression, TTR identified 39 vectors, WSA (60%) identified 111 vectors, WSA (65%) identified 38 vectors, and WSA (70%~) identified 19 vectors as capture-risky.

The optimistic ratio is the percentage of test vectors incorrectly identified as capture-safe. For example, when

one vector in 20 actual capture-risky vectors (Worst 20) is identified as capture-safe by TTR, the one vector is optimistically identified as capture-safe. The ratio is obtained as 0.05 (1/20) which is corresponding to Worst 20 for TTR in Table 2.

Obviously, pessimistic determinations cause over-test-induced yield loss, while optimistic determinations cause under-test-induced test quality degradation. From Table 2, we see that the TTR metric is more accurate since it has lower pessimistic and optimistic ratios than the other WSA-based metrics.

On average, the CPU time for checking the capture-safety of one test vector with the TTR metric was 6658.1 seconds, while IR-drop-analysis checking using EDA tools took 37798.8 seconds.

Tables 3, 4, 5, and 6 show the results for the circuit within an 8X compression environment. 2,246 transition fault test vectors with 98.5% fault coverage were generated using TetraMAX®. The total number of sensitized long paths was 83,312. From Tables 3 and 4, the proposed metric was able to identify risky test vectors with a high ratio of correct determinations.

Although Tables 3 and 4 demonstrate that the WSA metric with a 60% threshold could also achieve a high ratio
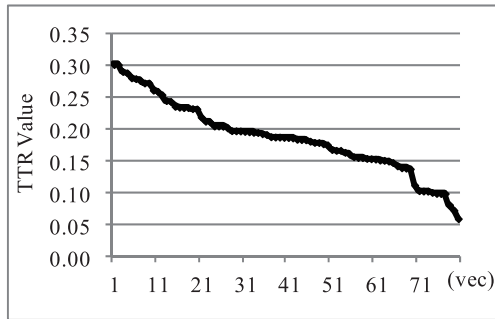
Fig. 9 TTR value distribution.

of correct determinations, the WSA metric is significantly pessimistic, as shown in Table 5. For this case, TTR identified 64 vectors, WSA (60%) identified 2223 vectors, WSA (70%) identified 1356 vectors, WSA (80%) identified 97 vectors, and WSA (90%) identified 27 vectors as capture-risky. The value "99%" in Table 5 means that almost all of the test vectors were identified as risky. This pessimistic determination is directly related to severe yield loss. The proposed metric can achieve lower pessimism than the WSA metric. As shown in Table 6, the proposed metric was able to achieve a relatively low optimistic ratio.

On average, the CPU time for checking the capture-safety of one test vector with the TTR metric was 8217.8 seconds, while IR-drop-analysis checking using EDA tools took 31838.1 seconds.

It should be noted that SPICE simulation or simulation using SPICE results require significantly more CPU time, which is unrealistic for large industrial circuits [19]. In addition, the proposed method conducts TTR metric for only vectors which sensitize paths obtained by sensitized long path identification in Sect. 3.3. In the experiments, all selected paths are sensitized by 50 vectors without compression and 80 vectors with compression.

As for the threshold, it is always important for capture-safety checking. For TTR metric, the threshold of TTR must be determined by the maximum TTR values in functional operation, because capture malfunction is caused by excessive switching activity in test operation while such excessive switching does not occur in functional operation. However, we could not obtain functional vectors for the circuits used. We assume 15% is the maximum TTR values in functional operation. Note that 100% is the case all gates have switching while few gates have switching in functional operation. Figure 9 shows the distribution of TTR values for 80 vectors selected by TTR metric. It is obvious that risky vectors are changed depending on the threshold. We address setting the optimal threshold determined by functional operation as our future work.

5. Conclusions

In this paper, we proposed the TTR metric, a novel metric that can more accurately identify capture-risky test vectors for at-speed scan testing. The TTR metric takes tran-sition time relations into consideration when assessing the switching activity in areas surrounding each sensitized long path. The advantages of the TTR metric for capture-safety checking were demonstrated by detailed analysis on an industrial circuit. Compared to WSA metrics, the proposed metric was able to achieve more accurate results that were obtained three times faster than with EDA tools. Future work includes implementing the TTR metric in a complete capture-safe test generation flow.

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