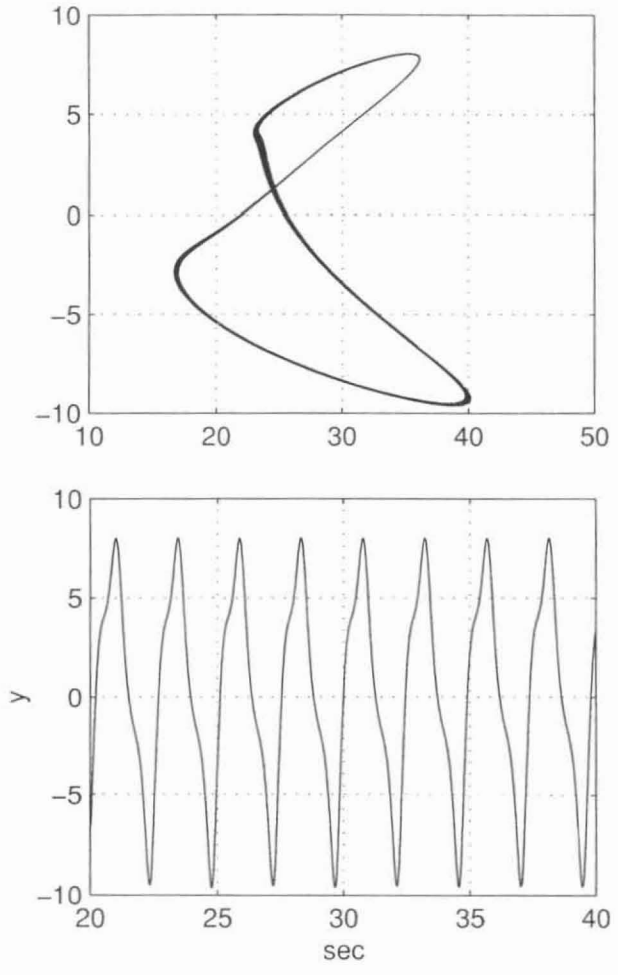

Fig. 4. Dynamics of the controlled period-2 orbit of the Lorentz system. (a) Phase portrait (b) Output (x_2)

Though general validity and sufficiency conditions for the effectiveness of the above algorithm is difficult to prove, it appears that stabilization in the above method is achieved through additional degrees of freedom introduced into the system by the filter in the feedback loop. The filter does not change much the projection of the system dynamics into the original low dimensional state space, but change only the Lyapunov exponent of the UPO. As compared to the delayed feedback method suggested by Pyragas [3], where the system dimension increases to infinity, a finite increase in system dimension occurs here, i.e., the finite dimensional LTI filter (a second-order transfer function for a single filter) approximates the delay element (having a transfer function e^{-Ts}) up to some frequency.

III. Conclusion

The above algorithm offers in a naive form a paradigm in which the problem of control of chaotic systems can also be viewed as that of synchronization of two back to back, mutually coupled system, of which one may be a chaotic system with numerous embedded UPO's and the other may be a LTI or a simpler nonlinear system whose natural dynamics is periodic. There is scope for future studies in using higher order filters and nonlinear systems in the feedback path.

In conclusion, a method of stabilizing chaotic systems approximately to a UPO, by small continuous-time perturbations, is presented. The main advantage of the above method lies in its easy applicability to a wide variety of systems. No complex calculations are involved and the algorithm can be implemented using low-order LTI filters only.

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CMOS Circuits Generating Arbitrary Chaos by Using Pulsewidth Modulation Techniques

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***Abstract*—This paper describes CMOS circuits generating arbitrary chaotic signals. The proposed circuits implement discrete-time continuous-state dynamics by means of analog processing in a time domain. Arbitrary nonlinear transformation functions can be generated by using the conversion from an analog voltage to a pulsewidth modulation (PWM) signal; for the transformation, time-domain nonlinear voltage waveforms having the same shape as the inverse function of the desired transformation function are used. The circuit simultaneously outputs both voltage and PWM signals following the desired dynamics. If the nonlinear voltage waveforms are generated by digital circuits and D/A converters with low-pass filters, high flexibility and controllability are obtained. Moreover, the nonlinear dynamics can be changed in realtime. Common waveform generators can be shared by many independent chaos generator circuits. Because the proposed circuits mainly consist of capacitors, switches, and CMOS logic gates, they are suitable for scaled VLSI implementation. CMOS circuits generating arbitrary chaos with up to third-order nonlinearity and two variables have been designed and fabricated using a 0.4 μm CMOS process. Chaos has been successfully generated by using tent, logistic, and Hénon maps, and a chaotic neuron model.**

***Index Terms*—Chaos, CMOS analog integrated circuits, nonlinear circuits, nonlinear functions, pulse width modulation.**

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I. Introduction

Many recent studies have revealed the important role of nonlinear analog dynamics from the viewpoint of information processing. Chaotic neural networks [1] and nonlinear oscillator networks [2] are typical examples. However, conventional VLSI neural hardware cannot sufficiently implement such nonlinear dynamics.

Circuit architectures in conventional neural VLSI chips are usually classified as digital or analog. Digital approaches essentially cannot implement analog dynamics, although they offer high precision and controllability. Analog approaches are obviously suitable for realizing analog dynamical systems but make it difficult to achieve arbitrary nonlinear, nonmonotone transformation because the transformation functions achieved by the analog approach strongly depend on the characteristics of devices and/or circuits used [3], [4].

We previously proposed a new circuit technique generating arbitrary nonlinear functions by using conversion from an analog voltage to a pulsewidth modulation (PWM) signal [5], [6]. A chaotic system using pulse timing and a nonlinear waveform [7] or one in which a capacitor is charged up by a constant current source [8] were proposed. Although our circuits are partly similar to such work, our approach targets on large-scale integrated nonlinear dynamical systems by sharing the common waveform generators.

In this paper, we present PWM CMOS circuits for arbitrary nonlinear dynamical systems, and demonstrate our experimental results for chaos generation using these circuits.

II. PWM Approach Suitable for VLSI Nonlinear Dynamical Systems

The PWM method is one approach toward achieving time-domain information processing by using pulse signals which have digital values in the voltage domain and analog values in the time domain. The PWM approach is suitable for large-scale integration of analog processing circuits because it matches the scaling trend in the Si CMOS technology, and it allows low voltage operation. Furthermore, its operation achieves lower power consumption than that of traditional digital or pulse-density modulation (PDM) circuits [9] because one data is represented by only one state transition.

In principle, the circuits proposed can implement the following nonlinear discrete-time continuous-state dynamical systems represented by N variables, x_n, $(n = 1, 2, 3, \cdots, N)$:

$$x_n(t+1) = \sum_{i=1}^{N} f_{ni}\left(x_i(t)\right) \tag{1}$$

where f_{ni} are arbitrary nonlinear transformation functions of one variable. Summations are achieved by switching current sources by means of PWM signals and by integrating charges into a capacitor [10]. A weight for summation is represented by a current value for each switched current source. Let us assume that PWM input signals have pulsewidth T_i, $(i = 1, 2, 3, \cdots, N)$, and currents I_i flow to capacitor C during period T_i. The number of charges stored in the capacitor, Q_{out} and the terminal voltage of the capacitor V_{out} are expressed as follows:

$$V_{\text{out}} = Q_{\text{out}}/C = \sum_{i=1}^{N} I_i T_i / C. \tag{2}$$

Thus, the weighted summation is achieved in PWM-voltage conversion.

Nonlinear transformations f_{ni} are performed in voltage-PWM conversion as follows. The PWM output signal is made by comparing V_{out} with a ramped reference value. A nonlinear transformation can be performed in this process of comparison by preparing a nonlinear reference waveform. If the reference signal voltage V_{ref} nonlinearly varies in the time domain, i.e., $V_{\text{ref}} = F(t)$ where F is a nonlinear function, the pulsewidth of output signal T_{out} expressed as a function of input voltage V_{out} is given by $T_{\text{out}} = F^{-1}(V_{\text{out}})$, where F^{-1} is the inverse function of F. The function F is, however, limited to a monotonic function in this scheme. Nonmonotonic functions can be gener-

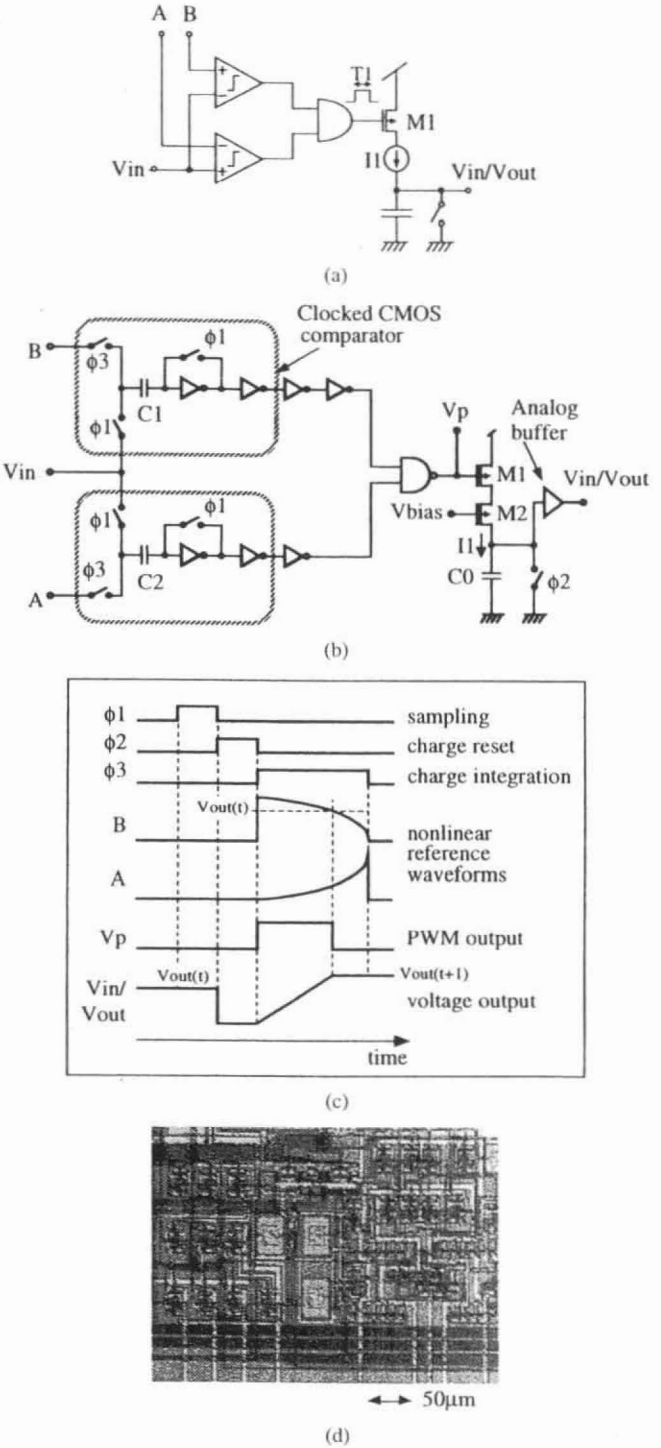

Fig. 1. Arbitrary chaos generator circuit with second-order nonlinearity designed using clocked CMOS comparators: (a) circuit configuration, (b) detail circuit, (c) timing diagram for performing logistic map, and (d) micro-photograph of the circuit in the fabricated chip (without a buffer).

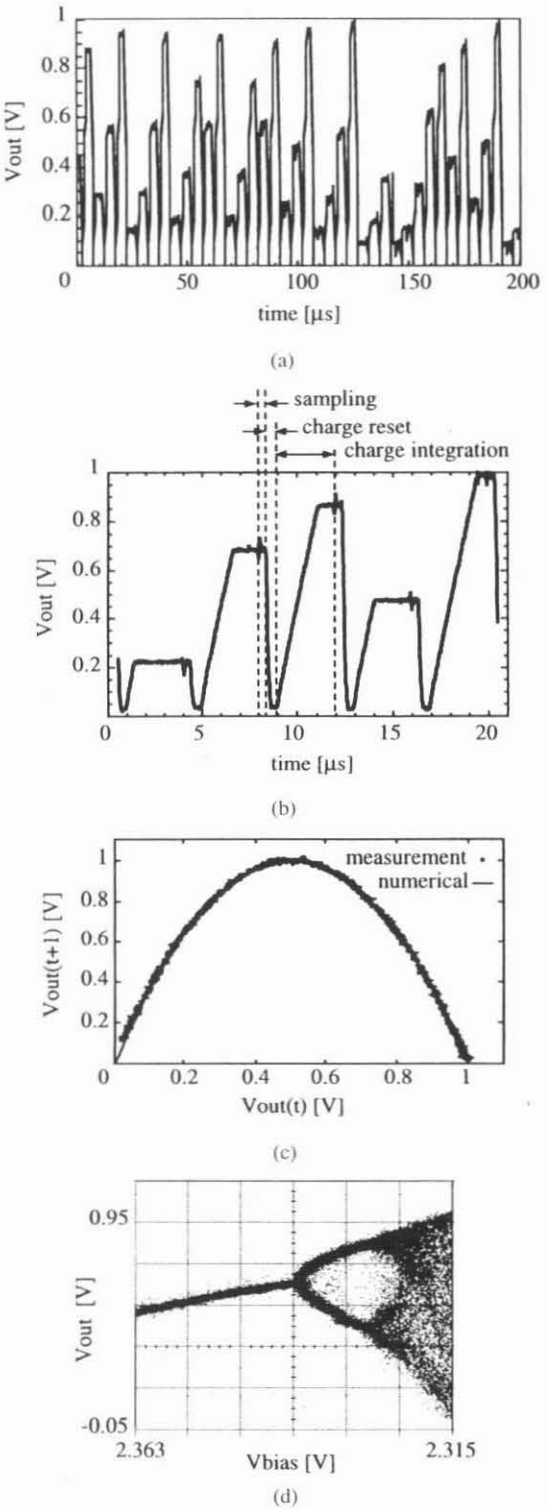

Fig. 2. Chaos observation for logistic map: (a) waveform on the oscilloscope screen, (b) magnified waveform where operation periods are indicated, (c) return map obtained by observed waveforms, and (d) bifurcation diagram obtained on the oscilloscope screen.

ated by combining the outputs of plural comparators, as shown in the following sections.

The reason this approach is useful is that it allows us to easily generate nonlinear waveforms $F(t)$ by using various oscillator circuits or a combination of digital approaches (look-up tables or function generation) and D/A converters. In the latter case, basic waveform data are arbitrarily generated by digital circuits; in addition, the waveforms can be changed in realtime with high controllability. This means that the nonlinear dynamics can be changed arbitrarily and in realtime. If the waveforms are smoothed by an additional low-pass filters, chaos can be generated even if the digital circuit has fairly low bit precision. Since a D/A converter operating at more than 100 MHz can be fabricated using a sub-micron CMOS technology [11], our chaos circuits can operate at more than 1 MHz with more than 6-bit precision. Because common waveform generators can be shared by many independent chaos circuits, the proposed approach is especially suitable for applications which require many chaotic units such as chaotic neural networks.

III. CMOS Circuits for Arbitrary Chaos Generation

A circuit for making second-order nonlinear functions of one variable and generating chaos is shown in Fig. 1. A clocked CMOS comparator that consists of CMOS inverters, a capacitor, and switches is effectively used. This comparator does not contain analog components, thus it can be shrunk with a scaling trend in CMOS fabrication technology. It also has a simpler configuration, consumes less power, and is more suitable for low-voltage operation than comparators using a differential-pair. Clocked operation is suitable for generating PWM signals because it is a discrete-time operation.

The circuit operation is as follows: During the ϕ_1 period, capacitors C_1 and C_2 hold the difference between the input voltage $V_{\rm in}$ and the threshold voltage of the inverters. This operation compensates for fluctuation of the threshold voltages in the inverters. During the ϕ_2 period, charges stored in C_0 are reset. Then, during the ϕ_3 period, monotonically nonlinear ramped reference voltages are supplied to nodes A and B. When the voltage of node A or node B reaches $V_{\rm in}$, the corresponding inverter inverts its output. Thus, an output pulse having the width $T_{\rm out}$ is generated. This PWM pulse turns on the current source, and voltage $V_{\rm out}$ is updated.

Since the clocked CMOS comparator operates as a sample and hold circuit, iterated operation can be achieved by simply feeding the output back to the input through an analog buffer. Thus, this circuit implements the following dynamics:

$$\begin{aligned} x(t+1) &= f(x(t)) \\ T_{\rm out}(t+1) &= f(T_{\rm out}(t)) \end{aligned} \tag{3}$$

where f is a second-order nonlinear function defined by the voltage waveforms supplied at nodes A and B. It is noted that one can simultaneously obtain both voltage and PWM signals following the given dynamics. This is a unique feature of our analog–digital merged architecture.

On the basis of the above circuit concept, we designed and fabricated a chaos generator chip using a 0.4 μm CMOS process that can implement arbitrary nonlinear dynamical systems with up to third-order nonlinearity and two variables by controlling pass gate switches. The capacitances are $C_0 = 5$ pF, and $C_1 = C_2 = 1$ pF. As an analog buffer, both a voltage follower of an on-chip op-amp and a CMOS source follower were used. The former gives high accuracy but occupies a large chip area. The latter makes the whole circuit compact, but the input–output relationship is not completely linear. However, this nonlinearity can be compensated for by modifying the reference waveforms. For simplicity, the following results are obtained by using the voltage follower. A micro-photograph of the arbitrary chaos generator circuit without the buffer part, which corresponds to the circuit shown in Fig. 1(a), is shown in Fig. 1(d).

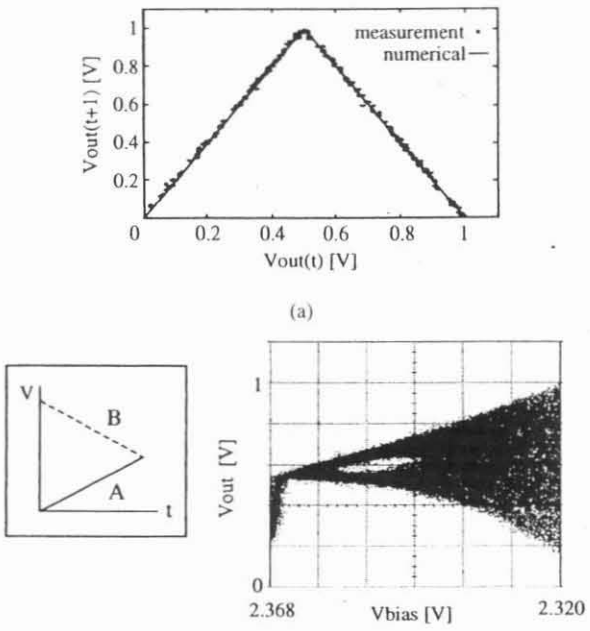

Fig. 3. Chaos observation for tent map: (a) return map obtained by observed waveforms and (b) bifurcation diagram obtained on the oscilloscope screen.

IV. Measurement Results of a CMOS Chip

In the following measurement, the power supply voltage was 3.3 V, and the clock period was 4 μs. The reference voltage waveforms were given by the external arbitrary waveform generator equipment.

First, we observed logistic map chaos. A logistic map is given by

$$x(t+1) = 4ax(t)(1 - x(t)) \tag{4}$$

where a is a parameter ranging from 0 to 1. Because the logistic map uses a second-order nonlinearity, the circuit shown in Fig. 1 can be used. The parameter a was modified by changing V_{bias}. The nMOSFET M_2 operates in the saturation region as a constant current source, whose current I_1 is proportional to $(V_{\text{bias}} - V_{\text{th}})^2$, where V_{th} is the threshold voltage of M_2. The current I_1 is proportional to parameter a in (4). Therefore, a is proportional to $(V_{\text{bias}} - V_{\text{th}})^2$, and when the change in V_{bias} is small enough, a change in a is approximately proportional to that in V_{bias}.

Fig. 2(a) and (b) show a chaotic behavior in the time series of the output voltage V_{out}. The disturbances due to clock control are observed at the start points of the *sampling* periods. Fig. 2(c) shows a return map obtained by the observed waveforms, where $a \approx 1$. We obtained about 6-bit precision. The precision is mainly determined by the comparators and the current source shown in Fig. 1. If the operation frequency is lowered, the precision at the comparators improves, but that at the current source degrades because the current value I_1 must be reduced for the fixed capacitance value C_0. If the capacitance value is increased, the precision improves, but the circuit area increases. Therefore, in order to improve the overall precision, the circuit has to be designed taking the operation frequency and the circuit area into account.

By supplying a linearly ramped signal to V_{bias} of approximately 20 Hz, and by sampling and holding V_{out}, a bifurcation diagram can be observed on the oscilloscope screen at the X-Y and *point* plot mode. An observed bifurcation diagram is shown in Fig. 2(d). Relatively large noise occurs partially because the oscilloscope samples transient states, and partially because a disturbance is caused by the ϕ_1 clock. However, this bifurcation diagram is only an on-screen demonstration of generating chaos. Many practical applications should use PWM chaotic sig-nals at V_p synchronizing with clock ϕ_3 as shown in Fig. 1(b) and (c); these PWM signals are free from such sampling noise.

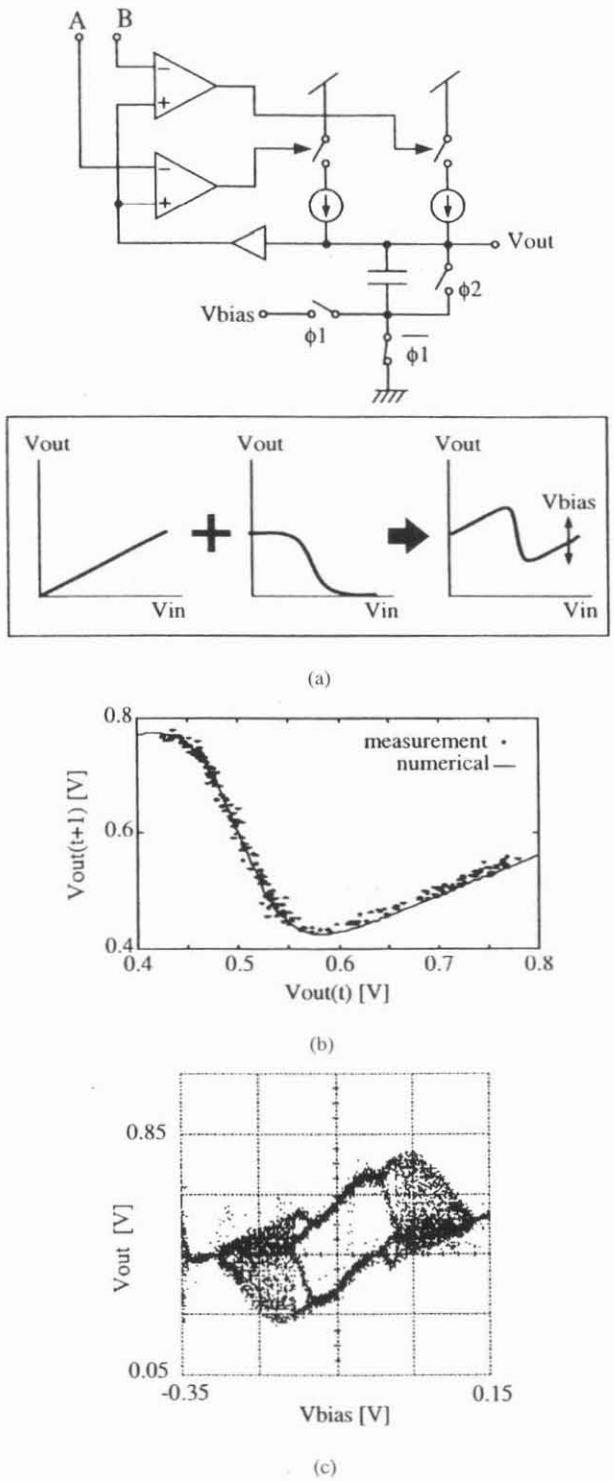

Fig. 4. Chaos observation for chaotic neuron model: (a) circuit configuration, (b) return map obtained by observed waveforms, and (c) bifurcation diagram obtained on the oscilloscope screen.

Fig. 3 shows the results of a tent map. A tent map is given by

$$x(t+1) = \begin{cases} 2ax(t), & \text{for } 0 \le x(t) < 1/2 \\ 2a(1 - x(t)), & \text{for } 1/2 \le x(t) \le 1 \end{cases} \tag{5}$$

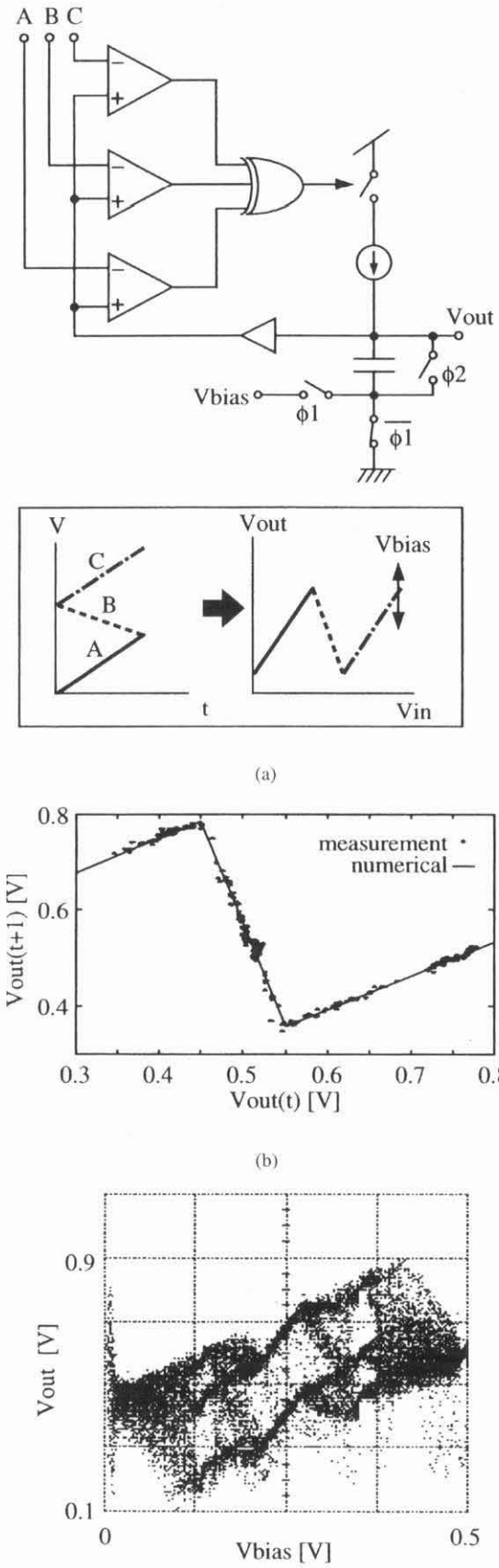

Fig. 5. Chaos observation for piecewise linear chaotic neuron model: (a) circuit configuration, (b) return map obtained by observed waveforms, and (c) bifurcation diagram obtained on the oscilloscope screen.

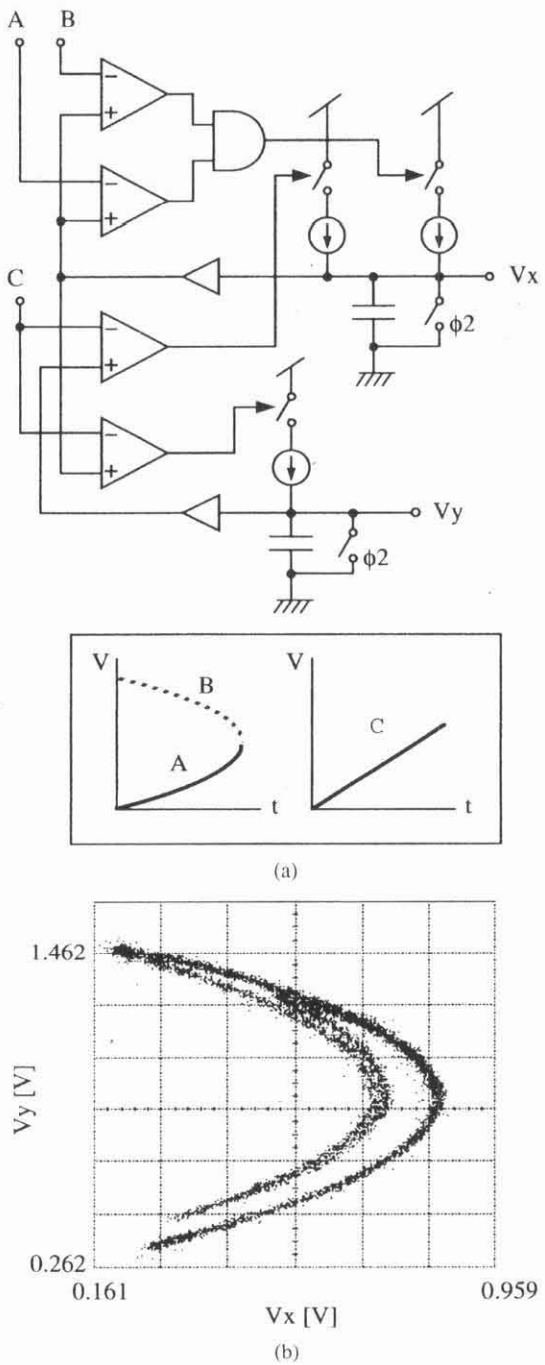

Fig. 6. Chaos observation for Hénon map: (a) circuit configuration and (b) return map obtained on the oscilloscope screen.

where a is a parameter ranging from 0 to 1. Because the tent map also uses a second-order nonlinearity, the same circuit configuration as that for the logistic map is used. The obtained return map and observed bifurcation diagram are nearly identical to those obtained by numerical simulations.

The next system is a chaotic neuron model [1]. Its dynamics are given by

$$y(t+1) = ky(t) - \alpha u(y(t)) + a \tag{6}$$

where $y(t)$ is the internal state of the neuron; k, α, and a are constants and $u(\cdot)$ is an activation function. This model is implemented by a circuit shown in Fig. 4(a), where $y(t)$ is expressed by V_{out}. The first two terms in (6) are expressed by the two current sources, which

is an example using weighted summation by switched current sources. The parameter a is modified by changing V_{bias}. For $u(\cdot)$ as a logistic function, the return map and bifurcation diagram obtained by the measurement results are shown in Fig. 4(b) and (c), respectively, which are nearly identical to those obtained by numerical simulation.

Fig. 5 shows the results of another chaotic neuron model, where $u(\cdot)$ is piecewise linear. Since (6) is considered to be a third-order nonlinear model, a circuit shown in Fig. 5(a) is used. The obtained return map and bifurcation diagram are nearly identical to those obtained by numerical simulation.

The last is an Hénon map, which is an example of two-variable nonlinear systems

$$\begin{aligned} x(t+1) &= y(t) + 1 - ax(t)^2 \\ y(t+1) &= bx(t) \end{aligned} \tag{7}$$

where a and b are constants. A circuit configuration and a return map are shown in Fig. 6. The two variables are expressed by the terminal voltages of two capacitors.

V. Conclusion

We presented a new circuit principle that implements arbitrary nonlinear dynamical systems using PWM signals. We designed and fabricated an arbitrary chaos generator chip by using a 0.4 μm CMOS process, and various chaos was successfully generated using the chip. Although the measurement results for bifurcation diagrams include relatively large noise because of experimental setups, in applications that directly use PWM signals, calculation precision as high as 6 bits can be achieved.

The nonlinear transformation described herein is arbitrary and analog. This cannot be realized by the ordinary analog or digital approach. Our approach allows nonlinear dynamics to be changed in realtime with high controllability. Thus, the proposed approach makes it possible to implement large-scale flexible nonlinear dynamical systems.

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