Full Digital Short Circuit Protection for Advanced IGBTs

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***Abstract*— A full digital short circuit protection method for advanced IGBTs has been proposed and experimentally demonstrated for the first time. The method employs combination of digital circuit, the gate charge sense instead of the conventional sense IGBT and analog circuit configuration. Digital protection scheme has significant advantages in the protection speed and flexibility.**

I. Introduction

As the increase in power density of IGBT with the reduction in chip thickness [1], the required time to protection becomes short, so that conventional protection method with sense IGBT ([2], [3]) will come to the limit of the speed. The required time to protection against short circuit for advanced IGBTs is expected to be less than 1 micro second (Fig. 1), which is much shorter than the protection speed with conventional sense IGBT method. To break the speed limit, the new approach has been introduced. The approach utilizes the gate charge as the indicator of the short circuit condition as explained in Fig. 2([4], [5]). This method is expected to improve the detection speed for the advanced IGBT.

In this paper, the new protection method is demonstrated on full digital configuration aiming to install automatic detection function of protection threshold and self–adjustment function for the deviation of device characteristics with temperature etc.. With these functions, the method can be applied to any type of IGBT without any change in the gate circuit and protection circuit. The new approach was experimentally demonstrated with a Field Programmable Gate Array (FPGA).

II. Protection Method with Digital Circuit

A. Comparison with Proposed method and Conventional method

Conventional short circuit protection method employs sense IGBT configuration with a gate drive circuit, a sense resistor R_s and the sense IGBT in the chip, as shown in Fig. 3(a). A sense IGBT is a small IGBT imbedded in the chip with a tiny emitter with common gate and collector with main IGBT. The high current under short circuit condition is detected with the voltage drop V_{sense} across R_S, which is proportional to the collector current. This method, however, has a drawback in the detection speed because of the noise from the high current through the main emitter under the short circuit condition.

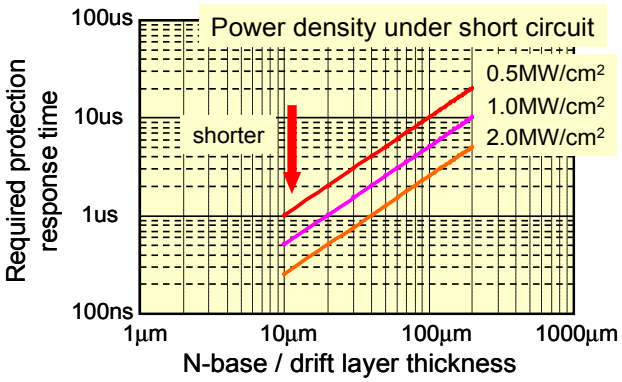


Figure. 1. Relationship between N-base thickness and the short circuit

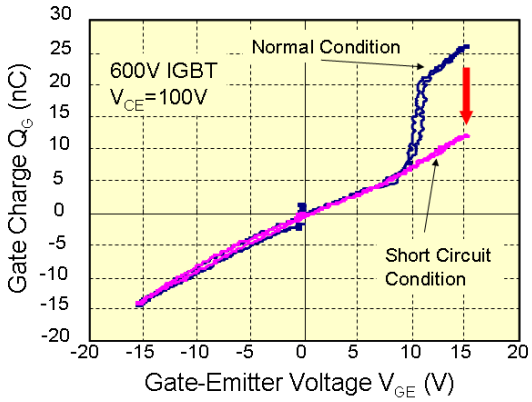
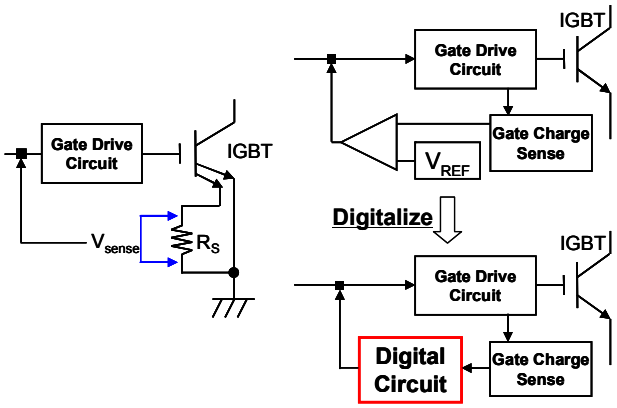


Figure 2. Difference of gate charge to the gate voltage under normal condition and short circuit condition.

To solve this problem, we propose a new method for the protection with gate charge as an indicator of the short circuit condition. Figure 2 shows the gate charge under short circuit condition in comparison with normal condition. Under short

circuit condition, the gate charge is substantially reduced from the value of the normal condition. In the new method, the decrease of the gate charge is detected with the gate circuit and feeds back the protection signal. A schematic illustration of the new protection circuit is shown in Fig. 3(b). The circuit consists of a gate driver, a gate charge sense, a reference voltage generator and a comparator. Once the voltage from the charge sense dropped to the predetermined reference voltage, the comparator output changed to the negative state which immediately pulled down the input voltage to the gate driver to protect the IGBT.



(a) Conventional Method (b) Proposed Method

Figure 3. Conventional method and proposed method

Applying the new method to practical IGBT protection, there are a couple of problems to be solved. In the method, the reference voltage is to be determined prior to install in the gate driver in the analog circuit for a particular IGBT to be protected and, more over, the reference voltage may changed with IGBT junction temperature, which means that the reference voltage generation must be temperature sensitive.

B. Advantage of digital protection over analog circuit

We employ digital circuit instead of analog configuration. The proposed method includes digital circuit with AD / DA converters. All the required functions such as reference voltage generation and comparator are implemented into the digital logic circuit. Major advantage of the digital logic over analog for the IGBT protection is the automatic reference voltage generation by self capturing the gate charge under normal condition. This function eliminates the procedure to determine the pre-setup of parameters, such as reference voltage, prior to implement the protection circuit into the IGBT inverters and makes it possible to adjust the reference voltage to the change in IGBT characteristics with temperature even under operation.

C. Gate charge sense circuit

The charge sense circuit is integrated into the gate driver as shown in Fig. 4. The gate driver is connected to bus voltage via two current mirror circuits. The equivalent current I_G^* to the gate current I_G flow into a capacitance C_M and the voltage V_{QG} across the capacitance indicates the gate charge of the IGBT driven by the gate circuit, i.e. the gate charge can be measured by the voltage V_{QG}.

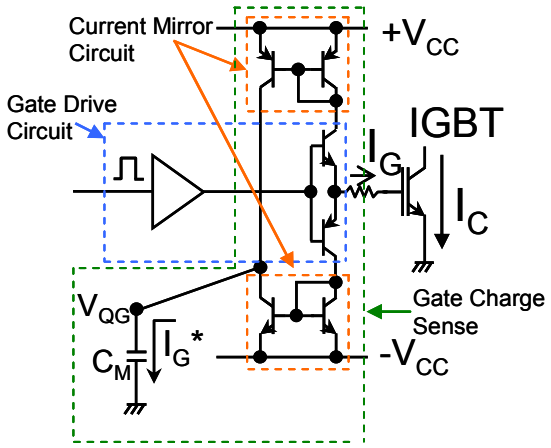


Figure 4. Configuration of gate charge sense

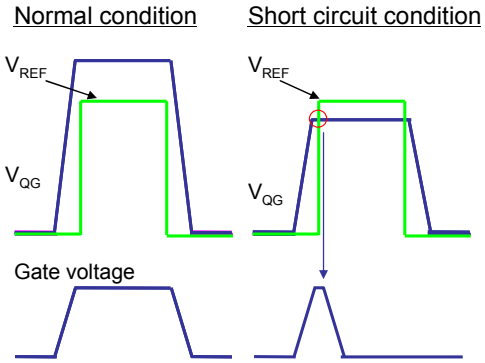


Figure 5. Schematic waveforms for reference voltage, gate charge voltage and gate voltage under normal condition and short circuit condition.

D. Protection scheme

The IGBT protection threshold is determined by the reference voltage V_{REF}, as shown in Fig. 5, and once the gate charge voltage V_{QG} drops below V_{REF}, the digital comparator outputs the protection signal.

III. Experiment and Result

The digital protection with the gate charge sense circuit was demonstrated using a FPGA. All the function explained below are implemented into the FPGA (32MHz) using Hardware Description Language (VHDL). A 60MHz A/D converter and a 125MHz D/A converter are used for analog interface.

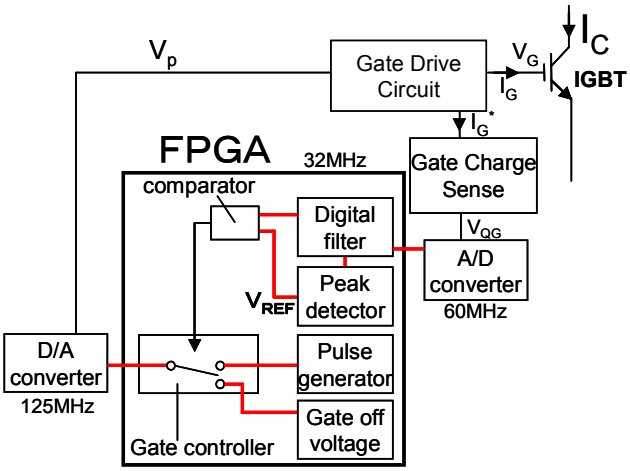
Digital filter: The voltage V_{QG} waveform is digitally filtered against the error with circuit noise. A FIR (Finite duration impulse response) filter is installed in the FPGA. The sampling frequency of about 30 MHz and the order of the filter is designed to be 4 for minimum time delay.

Peak detector: The reference voltage V_{REF} is generated in this block. V_{REF} is determined between V_{QG} values under the normal condition and short circuit condition with appropriate margin to prevent possible error caused by noise on V_{QG} waveform.

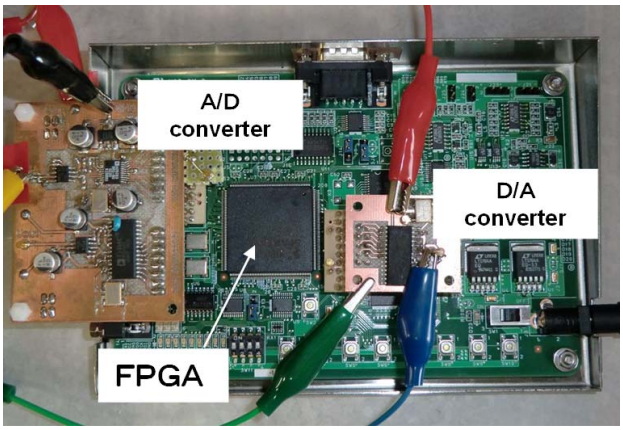
Pulse generator: Gate drive pulse for the experiment is generated in this block.

Digital Comparator: The gate charge voltage V_{QG} is digitally compared with the reference voltage V_{REF} to trigger the IGBT protection when V_{QG} decreases below V_{REF}.

Gate controller: The signal from the pulse generator is interrupted and switched to the off gate voltage when the protection scheme is triggered by the digital comparator so that the IGBT is immediately turned off.



(a)

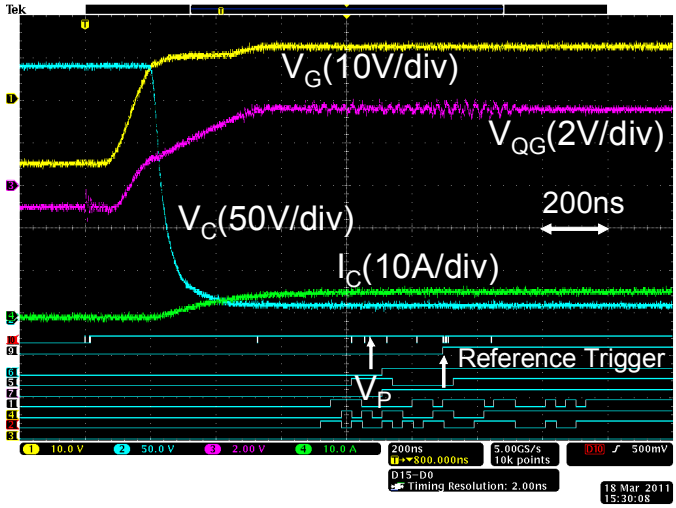


(b)

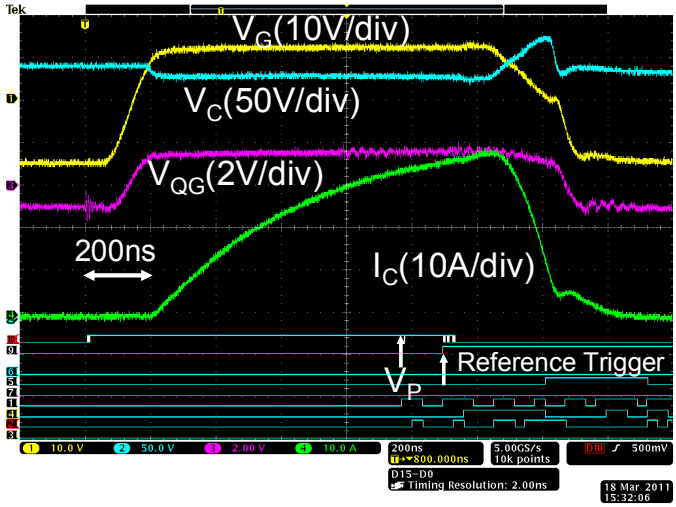
Figure 6. Block diagram for the demonstrated digital protection circuit(a) and the photograph of the FPGA board used in the experiment(b).

The short circuit protection with the digital circuit is demonstrated with the FPGA as shown in Fig 6. In this experiment, an IGBT with rated current of 10 A and the gate resistor of 27Ω. The main circuit voltage was 300 V.

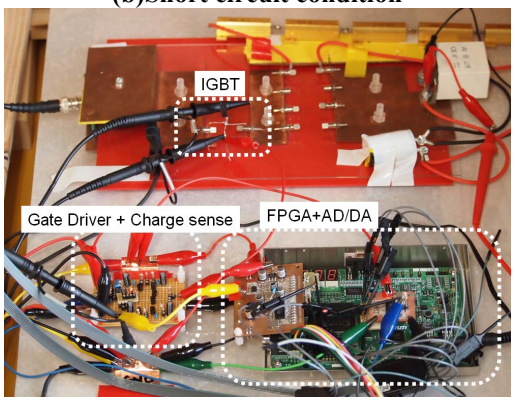
(1) Under normal condition, the peak detector obtains the data V_{PEAK} and generates the V_{REF} automatically. (2) Under short circuit condition, collector current I_C was shut down successfully by detecting the V_{QG} reduction.



(a)Normal condition



(b)Short circuit condition



(c)Experimental setup

Figure 7. Protection waveform under normal condition (a) the short circuit condition (b) with an IGBT GT10J303 and photograph for experimental setup(c).

The high speed protection was successfully demonstrated and the required time to protect the IGBT with this setup was about 1.5 μs. The most clock consuming process was the digital filtering. The overall protection time will be reduced to less than 1μs with the increase of clock frequency.

The detail of the experiment system is listed in Table 1.

IV. SUMMARY

We demonstrated the short circuit protection method for advance IGBT. The new method features the potential protection speed less than 1μs with the automatic capturing of the protection threshold and adjustment without pre-setting of parameters prior to setup the protection circuit into IGBT inverters. This function is enabled by the digital real time processing. The concept was experimentally demonstrated with a FPGA at 32MHz with high speed AD / DA converters as analog interfaces.

Table 1. Protection system detail

FPGA board		
	Device	XILINX Spartan XC3S400-4
	Clock	32 MHz
	Number of Gate	400kgates Max
AD Converter (8-Bit)		
	Device	Analog Devices AD9283
	Clock	60MHz
DA Converter(8bit out of 10-bit)		
	Device	Analog Devcies AD9760
	Clock	125MHz
Gate drive and gate charge sense		
	Op-amp	National Semiconductor LM7171
	NPN Bip Tr	Toshiba 2SC1815 x 3
	PNP Bip Tr	Toshiba 2SA1015 x 3
IGBT		Toshiba GT10J303
		Rg=27Ω

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