Sub-micron Junction Termination for 1200V Class Devices toward CMOS Process Compatibility

著者	Seto Kota, Takaishi Junpei, Imaki Hironori, Tanaka Masahiro, Tsukuda Masanori, Omura Ichiro
journal or publication title	2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD)
number	1943-653X
page range	281-284
year	2013-05
URL	http://hdl.handle.net/10228/5756

doi: info:doi/10.1109/ISPSD.2013.6694441

Sub-micron Junction Termination for 1200V Class Devices toward CMOS Process Compatibility

Kota Seto[1], Junpei Takaishi[1], Hironori Imaki[1], Masahiro Tanaka[1], Masanori Tsukuda[1,2] and Ichiro Omura[1]

[1]Kyushu Institute of Technology

1-1 Sensui-cho, Tobata-ku, Kitakyushu 804-8550, Japan

k349518k@tobata.isc.kyutech.ac.jp, omura@ele.kyutech.ac.jp

[2]Electrics Research Group for Sustainability, ICSEAD

***Abstract*— This study shows, for the first time, possibility of very shallow junction termination in submicron scale. The 2D-TCAD simulations unveil even 0.2µm junction depth structures are capable of blocking 1200V and usability for power devices with more than two hundreds of guard rings. Very shallow structure has robustness against diffusion depth deviation by special guard ring arrangement.**

I. INTRODUCTION

IGBTs have been required to have higher performance and mass productivity according with the increase in the demands in energy saving application field. It has been reported that shallow junction IGBTs with the new scaling rule exhibit feature of high current conduction, reduced losses and simplified fabrication process with the back-side-first wafer handling. The new concept of design method [1, 2] shows the direction to the future IGBTs with sub-micron fabrication process. Figure 1 shows the proposed design method with scaling factor k applying to trench MOS gate structure and while the cell width is maintained. According to the scaling, the V-I characteristics is improved to be 1.4V voltage drop for 1000A/cm^2 current conduction.

The edge termination design will become a bottleneck in production of the “sub-micron” IGBTs. The deep trench termination method can be a solution for this problem utilizing the advanced Micro Electro Mechanical System (MEMS) technology without long thermal process for fabrication [3, 4, 5]. In terms of process difficulty, the deep trench termination has disadvantage to planar technology.

Planar termination structure, on the other hand, sub-micron level shallow junction can cause breakdown voltage reduction with junction curvature increase ([6]).

The purpose of this study is to propose the very shallow junction termination design for high voltage power devices. In the following sections, a special method of guard rings arrangement with sufficient robustness to process condition deviation are shown for junction depth down to 0.2 um and breakdown voltage up to 2kV.

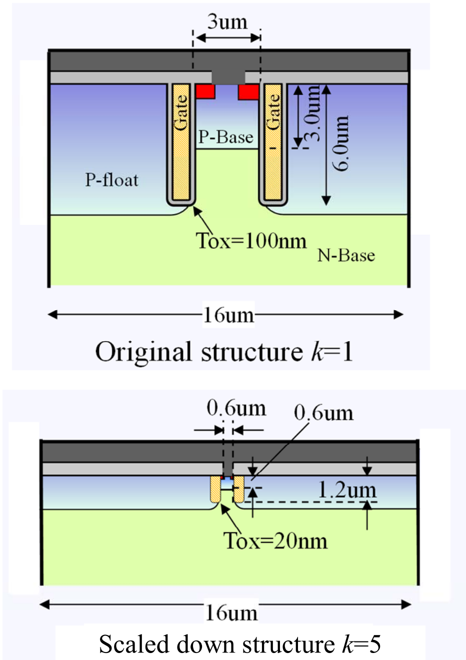

Fig.1 Scaled down IGBTwith the new scaling rule ([1,2]). Emitter side structures for k=1 and k-5 is shown.

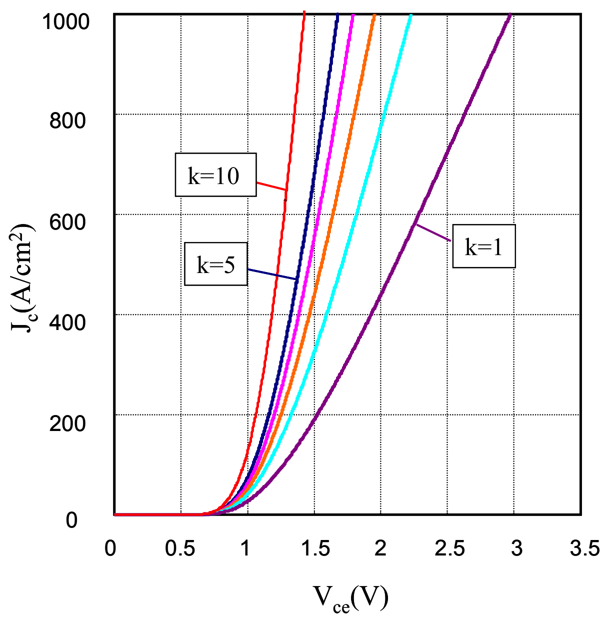

Fig.2 I-V characteristics of scaled down IGBTs ([1,2]) with shallower junction. In k=10 case, trench gate depth is only 0.6um and 1000A/cm^2 with Vce(sat) of 1.4V

II. SHALLOW GUARD RING ARRANGEMENT METHOD

A. Very shallow junction termination structure

Arrangement of P-rings is critical for very shallow guard ring structure design because breakdown voltage decreases with junction depth reduction ([6]), so design in very shallow guard rings needed special method of guard rings arrangement.

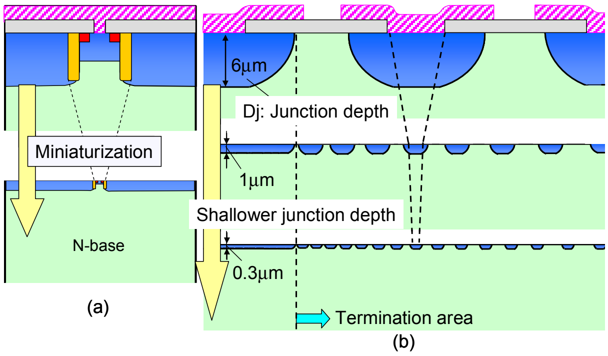

Fig. 3 scaled down IGBT (a) and concept of sub-micron junction termination (b).

In this design, termination area divided into three parts and interval of guard rings is determined by linear function respectively. The interval is gradually enlarged in inner area. In next area, only moderate increase of guard ring interval is applied to expand the depletion layer. In outer area, the interval of guard rings increases again to relax electric field near the N-layer. (Fig.3)

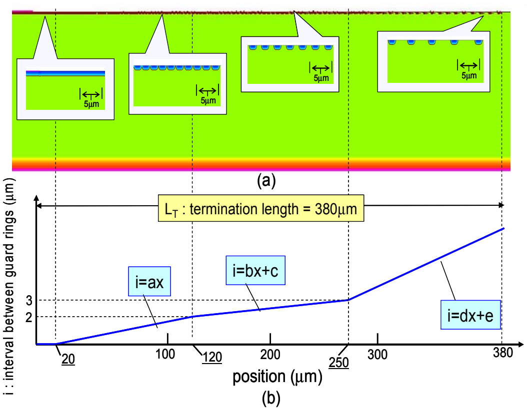

Fig.3 Method of shallow guard rings arrange

The anode P-layer concentration and cathode N-layer concentration, i-layer concentration for PiN structure were $3x10^{17}$ cm^{-3} and $1x10^{18}$ cm^{-3}, $7x10^{13}$ cm^{-3} respectively and i-layer thickness was 110 µm. Breakdown characteristics of shallow guard ring structures are shown in Fig.4. Very shallow structures have breakdown voltage efficiency equal to conventional structure and even 0.2µm junction depth structures are capable of blocking 1400V apply to 1200V class devices.

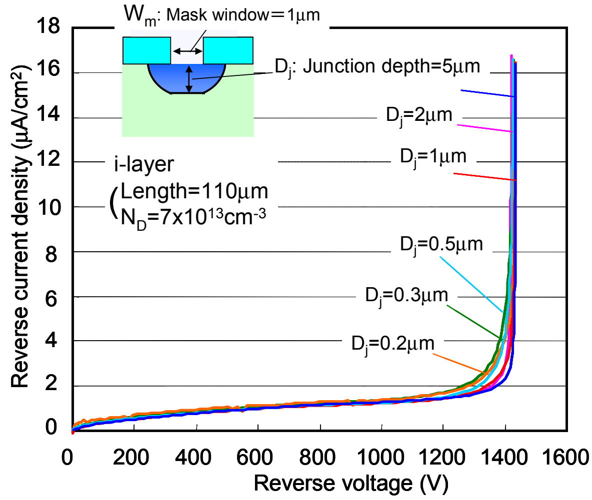

Fig.4 Breakdown characteristics of shallow guard

B. Robustness against diffusion depth deviation

In very shallow junction termination structure, sufficient robustness against diffusion depth deviation is required. Potential and electric field distribution of the shallow guard ring structure (D_j=W_m=1µm) are shown in Fig.5. By the special design method, electric field distribution has inverse U shape without extreme peak.

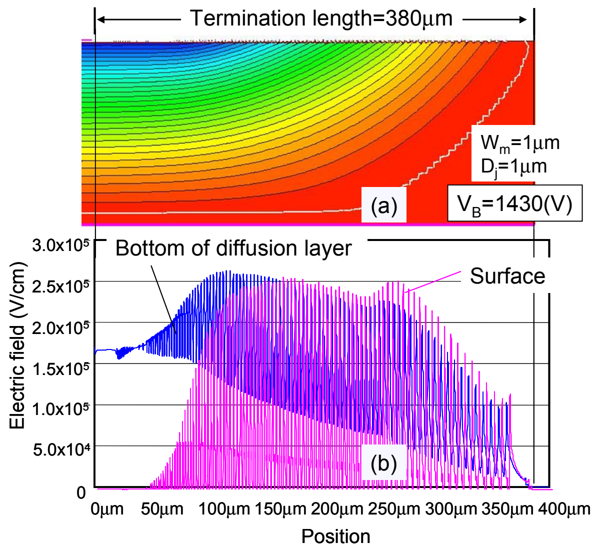

Fig.5 Potential distribution (a) electric field distribution (b)

Thanks to the inverse U shape electric field, peak of the field gradually shifts rather laterally and no significant field peak appears with junction depth deviation of 20% as shown in Fig. 6.

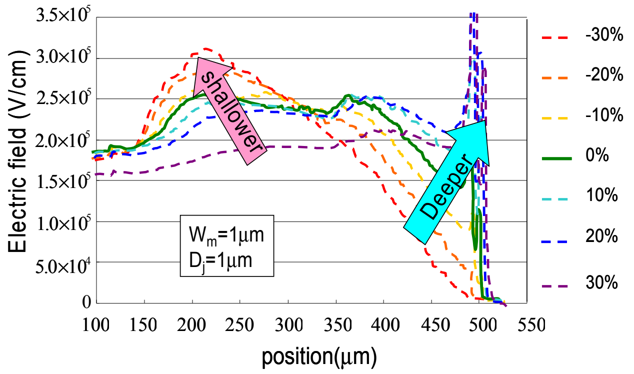

Fig.6 Diffusion depth deviation effects to electric field.

Robustness against diffusion depth deviation is shown in Fig.7. Proposed structure can maintain the breakdown voltage by peak shift for the diffusion depth deviation by inverse U shape electric field.

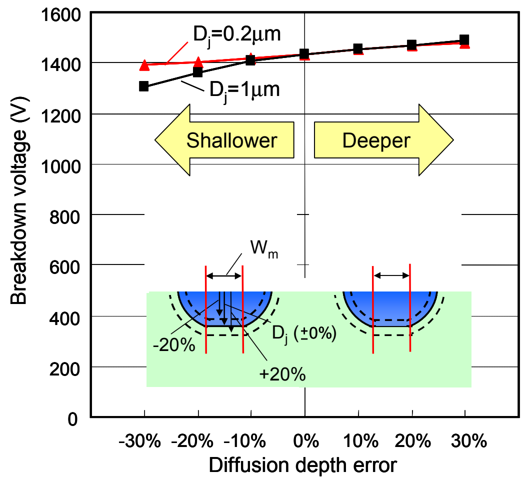

Fig.7 Robustness against diffusion depth deviation

III. Design Rule for Guard Ring Structure

A. *Design rule for shallow junction termiantion*

The number of the distributed guard rings over the termination area are, for example, 109 for D_j=1μm, 189 for 0.5μm, 225 for 0.3μm, 262 for 0.2μm, which is summarized in Fig. 8.

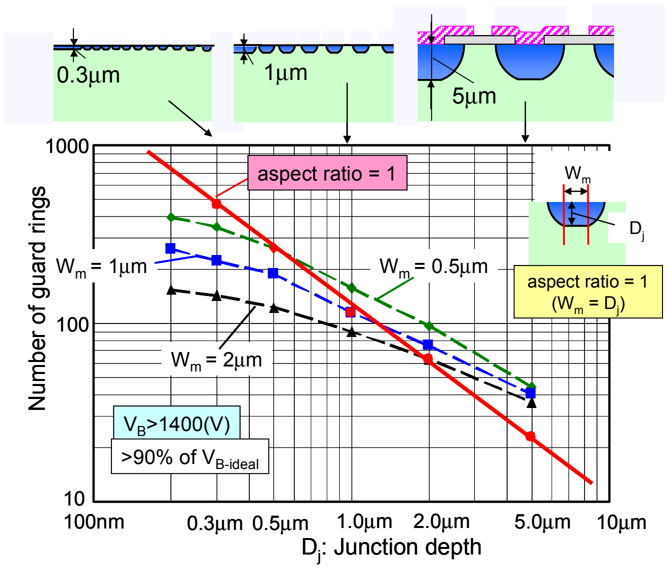

Fig.8 Relationship between junction depth and required number of guard rings.

The number of guard rings increase with junction depth shallower. The required number of guard rings is inverse proportional to junction depth for constant aspect ratio (ex. aspect ration of 1 (D_j=W_m) is shown in Fig.8)

Regardless the number of guard rings becomes tremendously large for the sub-micron junction termination, required termination length is equal to the conventional deep guard ring structure. ([7], [8], [9]) This result shows that shallow junction termination structure can be applied to sub-micron IGBT without increase in termination area.

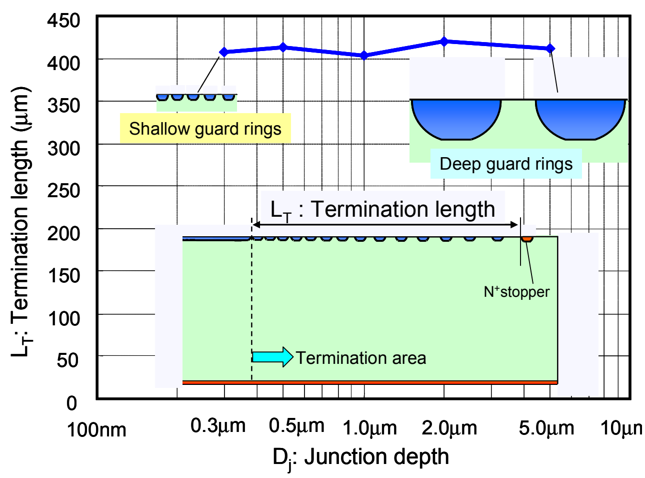

Fig.9 Relationship between junction depth and required termination length.

In shallow junction termination design, layout of guard rings is important and different layout method for each junction depths. It should be noted that, for various junction depths, a design is determined by the normalized ring-to-ring interval and the curves show universality as shown in Fig.10.

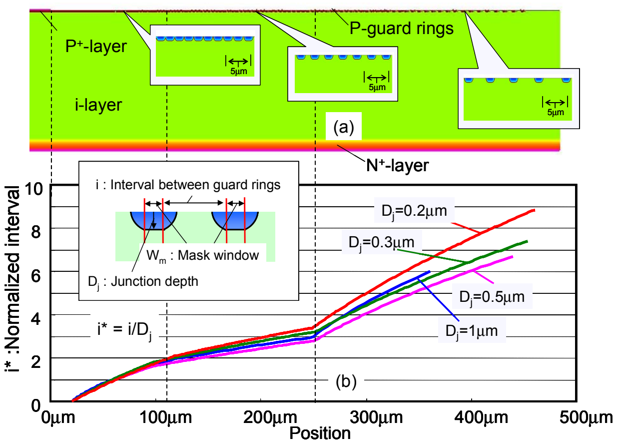

Fig.10 Universality of P-ring arrangement.

B. *Scaling rule for junction termination structure*

In this study, simulation results of different breakdown voltage devices unveil the scaling rule for guard ring structure design. Required number of guard rings is proportional to junction depth. (Fig.11)

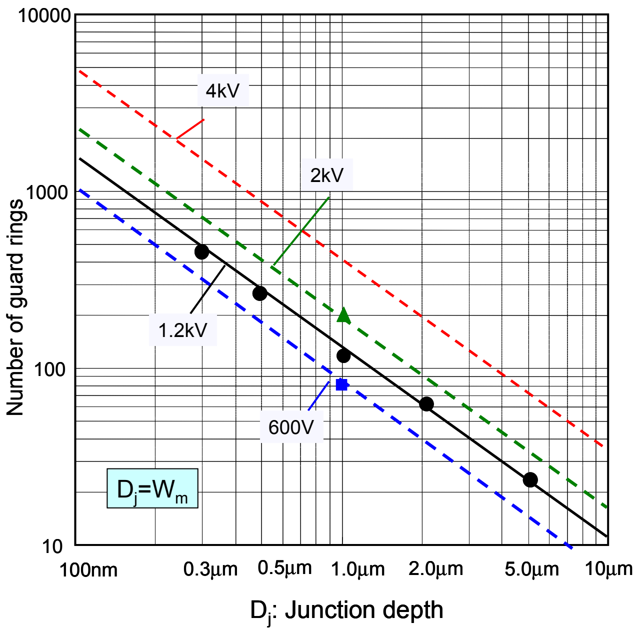

Fig.11 Design guideline of number of guard rings for junction depth down to deep sub-micron (D_j=W_m case).

The results shown in Fig. 11 simply summarized in the following formula.

$$\frac{V_{BV}}{D_j \cdot N_{GR}} = E_T \text{ [V/cm]}$$

Where, V_{BV}, N_{GR} and E_T are target blocking voltage, number of guard rings and a design constant with electric field dimension which is 0.5-1.1x10^5 V/cm in case of D_j=W_m.

IV. CONCLUSION

This study shows, for the first time, possibility of very shallow junction termination for the sub-micron IGBT. The 2D-TCAD simulations show that even 0.2µm junction depth structure can realize blocking voltage of 1200V with more than two hundreds of guard rings. Very shallow structure maintains robustness against junction depth deviation thanks to the proposed inverse U shape electric field distribution design. The required termination length is equal to the conventional deep junction termination even for the very shallow sub-micron guard ring structure. Scaling rule for guard ring structure design is proposed.

REFERENCES

[1] M. Tanaka et al. “Scaling Rule for Very Shallow Trench IGBT toward to CMOS process Compatibility,” Proc. of ISPSD 2012, pp. 177-180, 2012

[2] M. Tnaka et al. ”IGBT scaling principle toward CMOS compatible wafer processes,” Solid-State Electronics 80, pp.118-123, 2013.

[3] R. Kamibaba et al “Design of Trench Termination for High Voltage Devices” Proc. of ISPSD2010,pp. 107-110,2010

[4] K.Seto “Universal Trench Edge Termination Design” Proc. of ISPSD 2012,pp161-164,2012

[5] W. Hsu et al. “Innovative Designs Enable 300-V TMBS with Ultra-low On-state Voltage and Fast Switching Speed” Proc. of ISPSD 2011, pp80-83, 2011.

[6] M.Adler et al. “Theory and Breakdown Voltage for Planar Devices with a Single Field Limiting Ring” IEEE Transactions on Electron Devices, Vol.24, No.2, pp.107-113, Feb. 1977.

[7] S. Yasuda et al. “High-voltage planar junction with a field limiting ring” Solid-State Electronics, Vol.25, Issue5, pp. 423-427 May 1982.

[8] K.R. Whight et al. “Numerical analysis of multiple field limiting ring systems” Solid-State Electronics, Vol.27, Issue11, pp. 1021-1027 Nov 1984.

[9] T.Drabe et al. “Theoretical Investigation of Planer Junction Termination,” Solid-State Electronics, Vol.39, No. 3, pp. 323-328, Mar. 1996.