Numerical study on very high speed silicon PiN diode possibility for power ICs in comparison with SiC-SBD

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Abstract—**600V PiN diodes reverse recovery speed have been a bottle neck in reduction of system losses. In some applications such as PFC (Power Factor Control) SiC-SBDs have been replacing PiN diodes in recent years. The high speed reverse recovery characteristics of SiC-SBDs have contributed to the PFC downsizing and the efficiency improvement, only limited number of the diodes has been installed due to the high cost and the difficulty in implementation into power integrated circuits (Power ICs).**
In this work we have tried to find out possibilities to improve the PiN diodes capabilities in high speed applications based on analytical model, 1D and 2D-device simulation as our research tools. It is found that the reverse recovery can be improved by injection efficiency control with shallow P-/N-emitter. Simulated SOI structure shows the possibility to attain high speed characteristics comparable to SiC-SBDs.

I. INTRODUCTION

In power supply systems for information and telecommunications, higher power density is required with increase of consumed power of CPU. To attain high power density, increase in switching frequency is required to reduce the volume of inductor and capacitor because they occupy a considerable volume of power supply systems. Hence, fast recovery characteristics of power diodes are crucial to attain the high power density in power supply systems.

In power factor control (PFC) circuits, which are used in many of power supply systems, SiC Schottky barrier diodes (SBDs) have been introduced as fast recovery diodes, recently. SBDs show significant impact to downsizing the circuit with the increased switching frequency thanks to the very fast recovery characteristics [1].

If smaller power application is considered, however, SiC-SBD may have difficulty in realizing a small current chip and PFC function integration into single chip power ICs for small lighting equipment (LED, CFL) and so on.

In these circumstances, lateral fast recovery PiN diodes on silicon with 600V blocking voltage range will be very attractive for the single chip PFC if the reverse recovery speed of the silicon PiN diodes becomes comparable to SiC-SBDs.

In this paper, we propose a new lateral fast recovery diode structure on silicon. In following sections, we will introduce an analytical model to estimate silicon PiN diode theoretical speed limit in comparison with state-of-the-art SiC-SBDs, explain the approach to improve the speed of lateral silicon diode by the combination of shallow P-/N-emitter ([2], [3]) and SOI structure, show the simulation result and compare the recovery characteristics of the SiC-SBDs and the lateral silicon PiN diodes.

II. DESIGN CONCEPT FOR LATERAL VERY FAST RECOVERY DIODE

Flat carrier profile of stored carrier distribution in i-layer of PiN diodes has been recognized as a design method to attain high reverse recovery performance [2], [3]. Figure 1 schematically illustrates the flat carrier profile. In the profile, stored carrier rather has a flat shape than the well know U shape carrier profile. This profile realize the minimum amount of stored carrier for current conduction with reduced excess carrier in both side of i-layer (N⁻-layer).

For estimation of the theoretical possibility of silicon PiN diode, an analytical model is introduced ([4]) with equation (1),

$$\frac{Q_{RR}}{I_F} = \frac{V_B^2}{(\mu_n + \mu_p)(V_F - V_{built})E_{crit}^2} \tag{1}$$

where V_B, μ_n, μ_p, V_F, V_{build} and E_{crit} are breakdown voltage, electron mobility, hole mobility, forward voltage, built-in potential and critical electric field respectively. In the model, the i-layer length is assumed to be minimum value, i.e. very low doping concentration with the punch-through structure. Only drift currents contribute the conduction due to the constant carrier distribution.

Figure 2 shows the calculation results with the analytical model (Eq. (1)) as the theoretical limit of silicon PiN diode reverse recovery characteristics. This result is also confirmed by 1-dimensional TCAD simulation. In the figure, state-of-the-art characteristics and theoretical limit of SiC-SBD reverse recovery characteristics are shown as well. (The recovery charge is due to the junction capacitance discharge.) If we compare the theoretical limits of silicon PiN diode and SiC-SBD, the recovery speed limit of the SiC-SBD is much superior to silicon PiNs. Comparing with state-of-the-art SiC-SBD, it is found that silicon PiN diodes still have a large room of improvement and the performance can be comparable to state-of-the-art SiC-SBD.

To establish the flat carrier profile of stored carrier in the i-layer of PiN diodes, shallow P/N emitter and long carrier lifetime are needed to be introduced in the device design. The shallow emitter is effective to reduce stored carrier density at the emitter and the i-layer interface. The long carrier lifetime realize long ambipolar carrier diffusion length which enables the linear profile.

Carrier density distribution near emitter is shown Fig. 3. In emitter layer, most of the minority current is diffusion current. Equation (2) shows the diffusion current for normal emitter and the shallow emitter for P-emitter case.

$$J_n = qD_n \frac{n_0^2}{lN_A} \qquad (2)$$

where q, D_n, l, n_0 and N_A are electronic charge, diffusion constant, emitter thickness, electron density and hole density at the interface of the emitter and the i-layer, and impurity concentration of the emitter respectively. From equation (2), the minority carrier current is increased by thinning the emitter layer and as the result majority carrier injection efficiency decrease, i.e. the level of carrier storage near the both end of the i-layer can be reduced.

The SOI structure has advantage over junction insulation structure by restricting the area where holes and electrons are stored and thus can eliminate the tail current in reverse recovery waveform with no diffused carriers into substrate [5]. The SOI structure has an issue of the surface recombination. The surface recombination velocity in silicon-buried oxide interface is found to be a key parameter to control the characteristics of diode. The surface recombination velocity causes the reduction of effective carrier lifetime ([6] and hence lateral diffusion length of stored carrier in i-layer. The SOI layer thickness should be chosen according to the required ambipolar diffusion length with the surface recombination velocity. A relationship between effective carrier life time and surface recombination velocity is shown in equation (3).

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{(s_U + s_B)}{t_{SOI}} . \qquad (3)$$

where τ_{eff}, τ_{bulk}, S and t_{SOI} are effective carrier life time in SOI layer, carrier lifetime of bulk silicon in SOI layer, surface recombination velocity (s_U is at the upper surface and s_B is at the bottom surface) and SOI layer thickness respectively.

Figure 4 shows a relationship between SOI layer thickness and effective carrier life time and the effective ambipolar carrier diffusion length based on the analytical model and 2-dimensional simulation result. Here, the carrier life time is assumed to be 10 us for bulk silicon layer. In this work, we select SOI layer thickness of 10 um and surface recombination velocity of 1000 cm/sec. The effective ambipolar carrier diffusion length is approximately 50um.
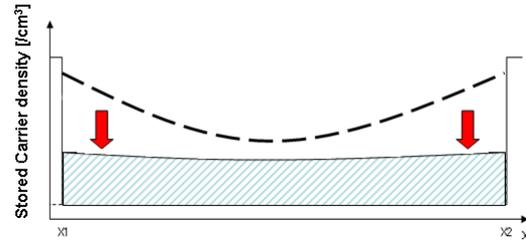

Figure 1. Optimization of stored carrier in PiN diodes[2] to improve $V_F - Q_{RR}$ tradeoff.
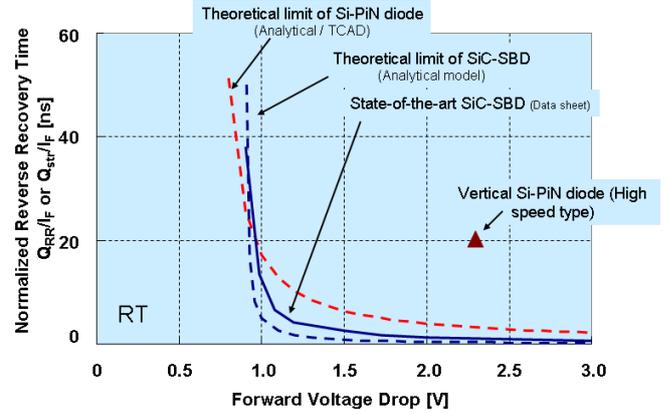

Figure 2. Theoretical level reverse recovery times for silicon PiN and SiC-SBD and vertical Si-PiN diode (high speed type).
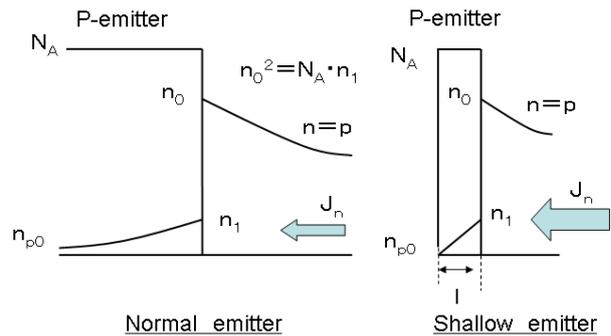

Figure 3. Carrier density distribution at N-emitter. The difference between normal emitter and shallow emitter is diffusion length. Electron current is increased at shallow emitter by shortening diffusion length.
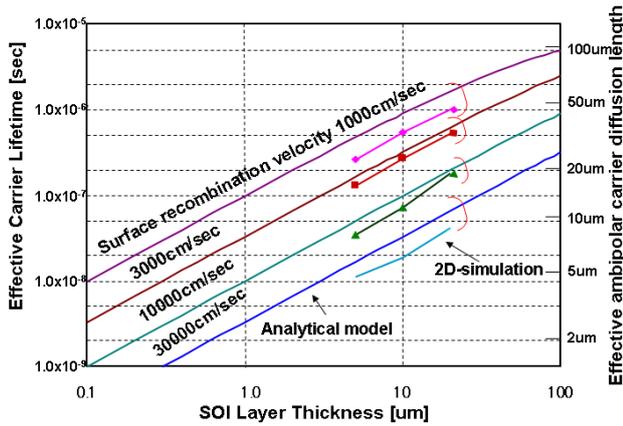
Figure 4. Surface recombination affect to effective carrier lifetime and hence diffusion length of stored carrier in SOI layer. The SOI layer thickness should be chosen according to the required ambipolar diffusion length and the surface recombination velocity.

III. SIMULATION

III-1 Device Design for 600 V Blocking Voltage

We simulate reverse bias characteristics of conventional structure and the proposed structure with the shallow P-/N-emitters. The structures are shown in Fig.5 and the reverse bias characteristics of the two structures are shown in Fig.6. The proposed structure with the shallow P-/N-emitters shows about 600 V blocking voltage with 5 um buried oxide. The reverse bias characteristics of two structures are in the same range.
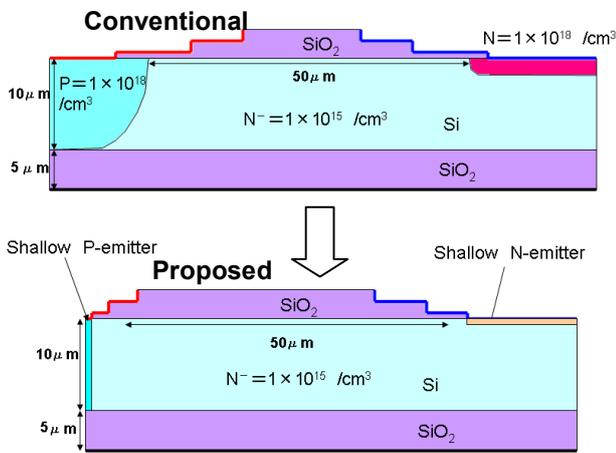

Figure 5. SOI power IC platform realization structure of the high speed PiN diode. SOI is chosen to minimize the stored carrier for conduction by maintaining the carrier inside restricted area. Shallow emitter concept [3] is adopted.
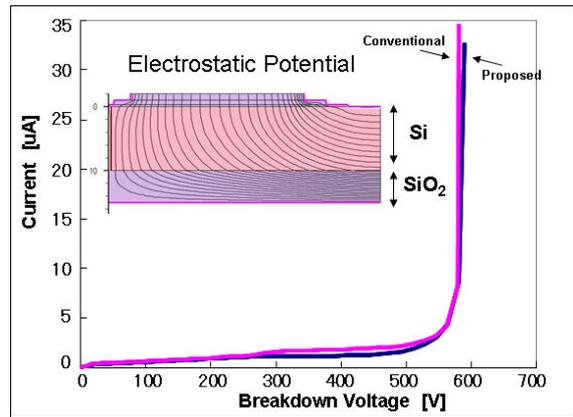

Figure 6. Reverse blocking characteristic for proposed diode in comparison with that of conventional structure.

III-2 Reverse Recovery Simulation Results

We simulate reverse recovery characteristics of proposed structure. The external circuit at reverse recovery simulation is simplified as shown in Fig.7. Reverse recovery waveform example is shown in Fig.8. The reverse recovery time for V_F=1.82 V diodes is about 100 ns (normalized RR time [4], Q_{RR}/I_F = 10 ns as shown in Fig.9).
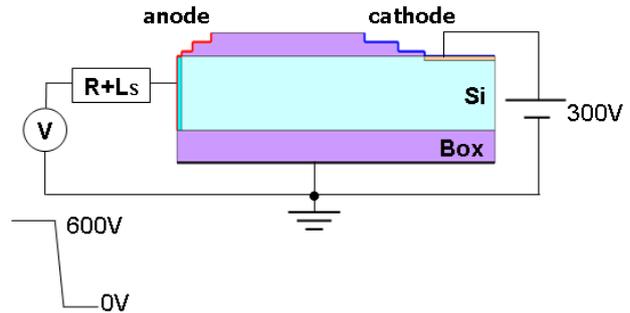

Figure 7. Circuit model at reverse recovery simulation. First, apply forward voltage to diode. Second, apply reverse voltage by grounded anode.
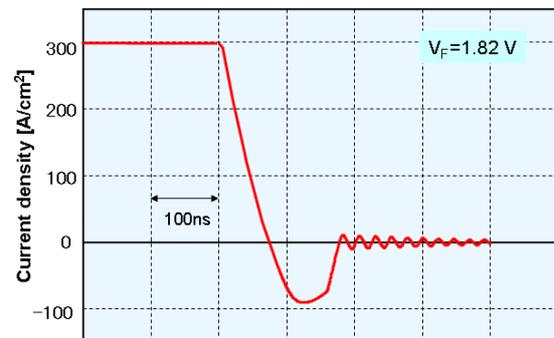

Figure 8. Reverse recovery wave form example for the proposed diode.

Figure 9 compares the normalized reverser recovery time for SiC-SBDs and the PiN diodes. The proposed SOI PiN diode shows potential of significant improvement in the

reverse recovery characteristics with slight increase in the forward voltage drop.

Through out the simulation, it is found that the major bottle neck to realize the high speed SOI PiN diode will be the oscillation phenomena in the tail current region due to the stray inductance. Figure 10 shows the waveforms for the reverse recovery for stray inductances of 100nH and 1nH as examples. The reduction of the stray inductance in the main circuit is crucial to realize the high speed SOI-PiN diodes.
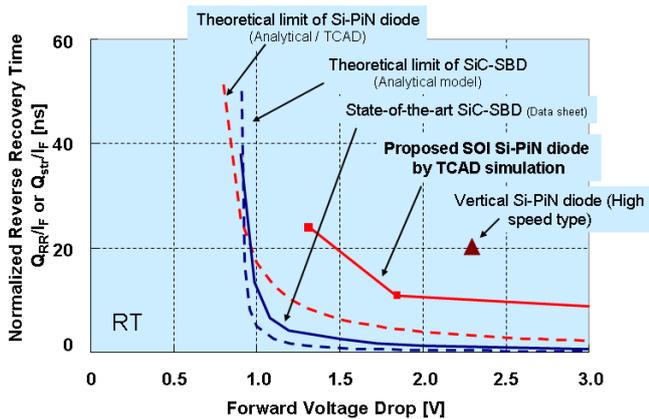

Figure 9. Theoretical, TCAD and datasheet level reverse recovery times for silicon PiN and SiC-SBD. Si-PiN diodes have large room to improve. (The normalized reverse recovery time is Q_{RR} or stored charge (Q_{str}) in a diode divided by forward current.) The proposed SOI diode shows potential of significant improvement.
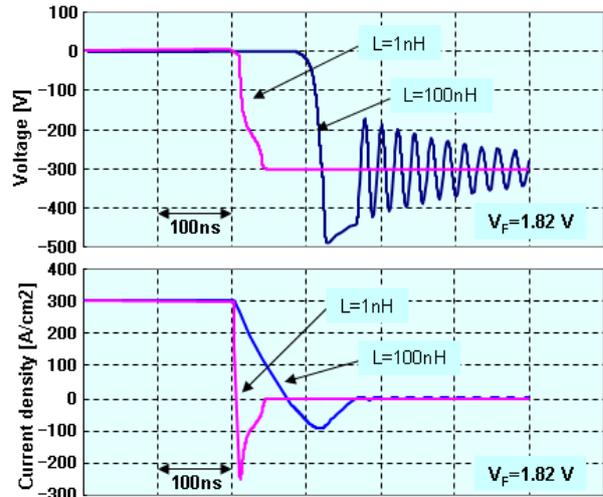

Figure 10. Reverse recovery waveform of voltage and current density for the proposed diode. The circuit inductance is 1nH or 100nH.

IV. CONCLUSION

We find that silicon PiN diodes still have a large room of improvement approaching to state-of-the-art SiC-SBD. The proposed SOI PiN diode shows potential of significant improvement in V_F-Q_{RR} trade off. The oscillation phenomena in the tail current region in the reverse recovery will be the major bottle neck to realize the high speed SOI PiN diodes. To improve recovery characteristics of silicon PiN diode, it is necessary to control of the oscillation.

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