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著者	Tanaka Masahiro, Omura Ichiro
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IGBT Scaling Principle Toward CMOS Compatible Wafer Processes

Masahiro Tanaka* and Ichiro Omura

Kyushu Institute of Technology, 1-1 Sensui-cho, Tobata-ku, Kitakyushu-city, 804-8550, JAPAN

1. Abstract

A scaling principle for trench gate IGBT is proposed. CMOS technology on large diameter wafer enables to produce various digital circuits with higher performance and lower cost. The transistor cell structure becomes laterally smaller and smaller and vertically shallower and shallower. In contrast, latest IGBTs have rather deeper trench structure to obtain lower on-state voltage drop and turn-off loss. In the aspect of the process uniformity and wafer warpage, manufacturing such structure in the CMOS factory is difficult. In this paper, we show the scaling principle toward shallower structure and better performance. The principle is theoretically explained by our previously proposed "Structure Oriented" analytical model. The principle represents a possibility of technology direction and roadmap for future IGBT for improving the device performance consistent with lower cost and high volume productivity with CMOS compatible large diameter wafer technologies.

Keywords: IGBT, More than Moore, constant field scaling, roadmap, compact model

1. Introduction

The 300mm to 450mm "More Moore" field semiconductor technology based on the high resolution lithographic techniques enhances significant performance and mass-productivity improvements in the digital integrated circuits by Moore's Law as a scaling by a factor of 0.7 every 2 years for critical dimension [1] [17]. On the other hand, the importance of "More than Moore" field like that analog and mixed signal processors, sensors and actuators, micro-mechanical devices, and power devices, is increased a lot. And these "More than Moore" devices also will be forced to be designed in the compatibility of the large diameter wafer process technology to realize better performance and lower cost.

Trench gate IGBTs are currently mass produced on the wafers of ~200mm diameter. Current structures have rather deep trench gate on the Cathode side to obtain better trade-off relationship between on-state voltage drop V_{ce}(sat) and turn-off loss[2]-[16]. Thus, current technical direction for the trench gate IGBT is different from the "More Moore" process technologies.

In this paper, we propose a scaling principle for the trench gate IGBT. By applying the principle, the "More Moore" process technologies can be used for the trench gate IGBT fabrication and the scaled IGBT shows better performance even with shallower Cathode structure; shallower trench gate and shallower P-base. The principle directs new IGBT design trends with the compatibility for the large diameter wafer process technology.

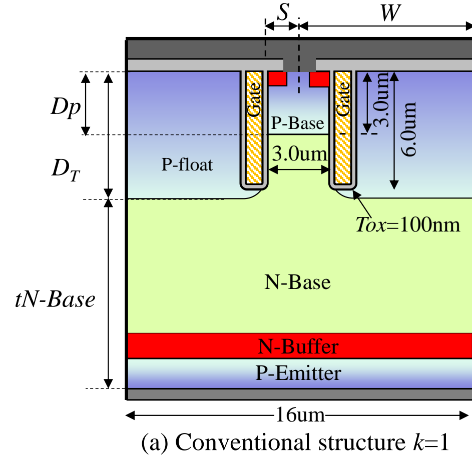
* Corresponding author. mtanaka@hotmail.com
Tel/Fax: +81 (93) 884 3268

From next section, we begin with the concept for our scaling principle. Then we show the verification results for the scaling principle by two-dimensional TCAD simulations. The results show that the IGBT even with shallower Cathode structure which designed by the proposed scaling principle has lower on-state voltage drop than the conventional structure. After that, we discuss about this improvement by referring our previously proposed "Structure Oriented" analytical model [18]. The improvement can be theoretically explained by the compact model formation. Finally we show a potential of the IGBT's further performance improvement by reducing wafer thickness margin, which is enabled by narrower trench-trench spacing.

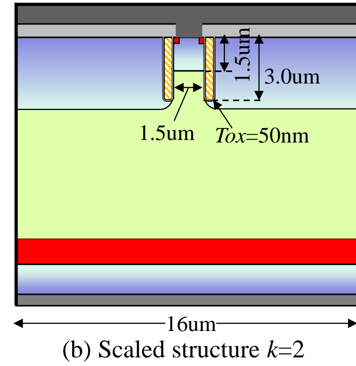
2. IGBT Scaling Principle

The scaling principle is based on the general CMOS scaling principle with considering the Cathode side electron injection efficiency γ_n . The principle realizes both shallower Cathode structure and higher γ_n than the conventional structure. It leads higher carrier concentration in the Cathode side and lower on-state voltage drop.

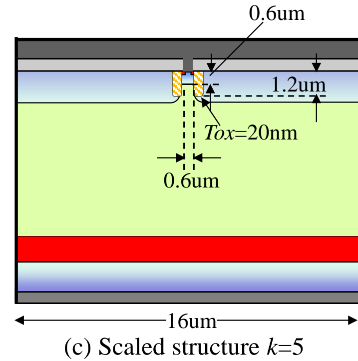
Figure 1 shows the concept of the scaling principle. Figure 1 (a) shows commercially available IGBT that has a 6um depth trench gate and a 3um depth P-base. Trench-trench spacing is 3um and cell pitch is 16um. It uses a 1000 angstrom gate oxide thickness and the P-base concentration is chosen to give suitable gate threshold voltage V_t of around 5V. The applied gate voltage is 15V. In this paper, we introduce a scaling factor "*k*" for these structure parameters and the gate voltage. Figure 1 (b) and (c) show the scaled IGBTs with *k*=2 and 5 respectively. Four parameters are reduced by the scaling factor *k*; trench-trench spacing *S*, gate oxide thickness T_{ox}, trench depth D_T and P-base depth D_P. In the other words, $S'=S/k$, $T_{ox}'=T_{ox}/k$, $D_T'=D_T/k$ and $D_P'=D_P/k$ where the primed parameters refer to the scaled device. The cell pitch *W* keeps constant. There are no arrangements in the Anode side. For example, the scaled device with *k*=2 has a 3um depth trench gate, a 1.5um depth P-base, a 1.5um trench-trench spacing and a 500 angstrom thickness gate oxide. But the cell pitch keeps 16um as the conventional structure.



(a) Conventional structure *k*=1



(b) Scaled structure *k*=2



(c) Scaled structure *k*=5

Figure 1. Scaled trench IGBT

Unlike the CMOS scaling principle, the P-Base doping concentration is not scaled to keep similar saturation current level to the conventional structure. But, as discussed later, slight adjustment for the P-Base concentration is required to obtain same switching characteristics and saturation current as the conventional structure.

The gate voltage for the scaled device is reduced by the scaling factor. In the other words, $V_g' = V_g/k$. So, for example, the gate voltage for k=2 device is 7.5V. The applied electric field in the gate oxide is kept as the conventional structure.
In order to produce highly scaled device such as k=5, several developments for the fabrication process would be required. First, high quality large diameter Floating Zone (FZ-) wafers should be established while the Czochralski (CZ-) wafers or epitaxial wafers are used for the "More Moore" devices. Second, the short channel effect due to the shallower P-Base should be eliminated to reduce leakage current. Third, the high-k gate dielectric and the metal gate processes should be developed for the trench gate to keep dielectric reliability and lower gate resistivity.

3. Verification of the Scaling Principle

Proposed scaling principle was verified by two-dimensional TCAD simulations. We used 1.2kV thin wafer PT-IGBT vertical structure for the validation. Table 1 shows structure parameters for k=1 to 5. *CP-Base* is the P-Base doping concentration at the junction between the N-Emitter and P-Base. Gaussian distributions are assumed to P-Base doping profiles. The concentrations are adjusted so that the threshold voltage of the scaled devices are 1/k of the conventional (k=1) device. The N-Base doping concentration is 7.0x10^{13}cm^{-3}. The P-Emitter doping concentration and thickness are 1.0x10^{17}cm^{-3} and 1um respectively. The N-Buffer doping concentration and thickness are 9.0x10^{16}cm^{-3}and 1um respectively. A constant doping profile is assumed for the P-Emitter and N-Buffer.

Table 1. Structure parameters used for the scaling principle verification.

k	1	2	3	4	5
W[um]	16.0	16.0	16.0	16.0	16.0
D_T[um]	6.0	3.0	2.0	1.5	1.2
D_P[um]	3.0	1.5	1.0	0.8	0.6
S[um]	3.0	1.5	1.0	0.8	0.6
T_{ox}[A]	1000	500	333	250	200
V_g[V]	15.00	7.50	5.00	3.75	3.00
CP-Base [x10^{17}cm^{-3}]	2.80	3.50	4.00	4.40	4.80
tN-Base[um]	120	120	120	120	120

Calculated I_c-V_{ce} characteristics of the scaled structures are shown in Figure 2. The on-state voltage drop is reduced with incrementing k. Calculated N-Base carrier distributions of the scaled structures are shown in Figure 3. It shows that higher carrier concentration can be obtained in the Cathode side with incrementing k. The result means that this IGBT scaling principle realizes higher electron injection efficiency γ_n than the conventional structure. It also means the performance of the scaled device is better than the conventional structure. Calculated inductive turn-off waveforms are shown in Figure 4. The scaled devices show same switching characteristics because the gate charge Q_g and the difference of the gate voltage and threshold voltage, V_g-V_t, are equally scaled by k. The Q_g is scaled as $Q_g' = Q_g/k$ due to $T_{ox}' = T_{ox}/k$, $D_T' = D_T/k$ and $V_g' = V_g/k$. Calculated breakdown characteristics are shown in Figure 5. The scaled devices show higher breakdown voltage because the electric field distribution around the bottom of the trench gate is improved by narrower trench-trench spacing.

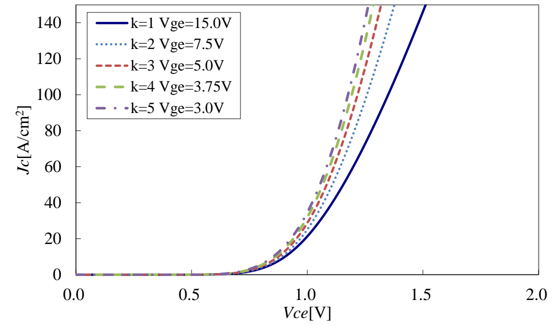


Figure 2. Calculated I_c-V_{ce} characteristics for the scaling factor k=1 to 5.

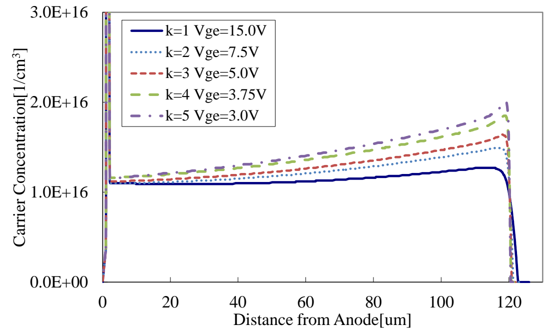


Figure 3. Calculated carrier distribution in the N-

Base region for the scaling factor k=1 to 5. (Jc=150A/cm^2)

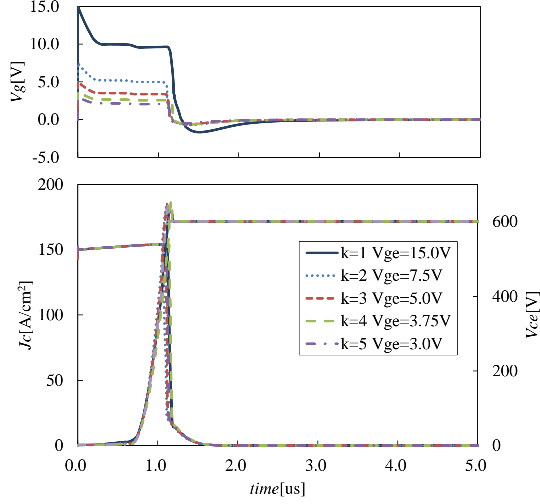


Figure 4. Calculated inductive turn-off waveforms for the scaling factor k=1 to 5.

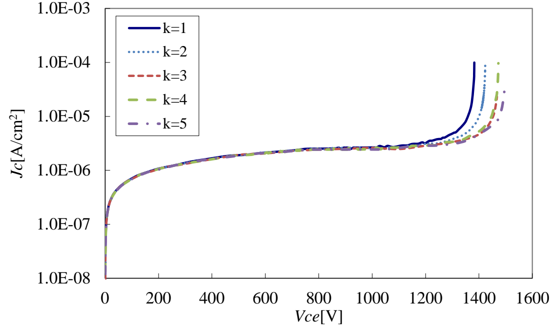


Figure 5. Calculated breakdown characteristics for the scaling factor k=1 to 5.

4. Discussion with the "Structure oriented compact model"

2. *Cathode side analytical modelling*

In this section we discuss about the detailed mechanism to obtain lower on-state voltage drop instead of shallower Cathode structures. It can be explained by previously proposed "Structure Oriented" analytical model for the trench gate IGBTs [18]. Stripe cell structure is assumed in this paper. We review the Cathode side formulation.

In this model, we assumed a conductive modulation (n~p) and no carrier recombination in the mesa region. We also assumed that a part of electron current flows along the accumulation layer beside the trench gate. Figure 6 shows the current elements under the P-base region. I_n^{acc} is the electron current via the accumulation layer per unit length for the third direction. J_p^{mesa} and J_n^{mesa} are the electron current density and hole current density in the mesa region, respectively. J_p^{cell} and J_n^{cell} are the electron current density and hole current density in the N-Base region, respectively.

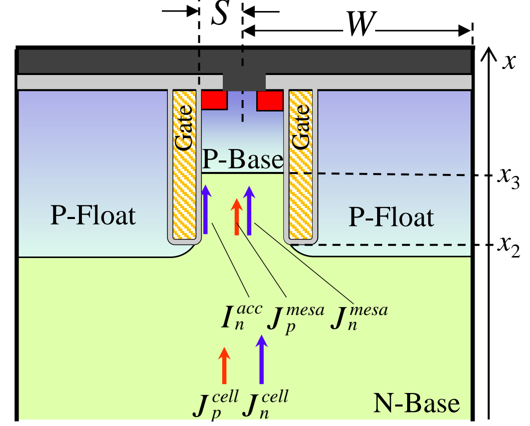


Figure 6. Assumed current elements in the trench gate structure

Following relationships are held between the mesa region and N-Base region.

$$W \cdot J_p^{cell}(x_2) = S \cdot J_p^{mesa}(x) \tag{1}$$

$$W \cdot J_n^{cell}(x_2) = I_n^{acc}(x) + S \cdot J_n^{mesa}(x) \tag{2}$$

The electron current flowing in the accumulation layer I_n^{acc} can be calculated by the electron quasi-Fermi potential and the electron mobility of MOS gate.

$$I_n^{acc}(x) = -\mu_{n-acc}\varepsilon_{ox}\frac{V_g}{T_{ox}}\frac{d\phi_n}{dx} \tag{3}$$

The electron mobility in the accumulation layer μ_{n-acc} is degraded by the normal electric field and can be calculated by [19].

The electron current density in the mesa region can be formed by the electron concentration and electron quasi-Fermi potential as

$$J_n^{mesa}(x) = -q \cdot \mu_n \cdot n(x)\frac{d\phi_n}{dx} \quad (4)$$

From the drift-diffusion equations under the conductive modulation condition, following differential equation for the carrier density can be formulated in the mesa region.

$$\mu_p J_n^{mesa}(x) - \mu_n J_p^{mesa}(x) = 2\mu_p \mu_n kT\frac{dn}{dx} \quad (5)$$

From (1) to (5), we obtain the Cathode side carrier distribution equation with the structure parameters as

$$\left(\frac{\mu_p}{\mu_n}\left(\frac{\varepsilon_{ox}\mu_{n-acc}V_g}{T_{ox}q\mu_n n(x)S}+1\right)^{-1}+1\right)\gamma_n - 1 = \frac{2qD_p}{J}\frac{S}{W}\frac{dn}{dx} \quad (6)$$

Where

$$\gamma_n = \frac{J_n^{cell}(x_2)}{J_p^{cell}(x_2) + J_n^{cell}(x_2)} \quad (7)$$

and J is the total current density.

1.1. Theory for IGBT performance improvement

The theory for the principle is delivered from eq. (6). The differential equation can be arranged to the scaled Cathode structures.

$$\left(\frac{\mu_p}{\mu_n}\left(\frac{\varepsilon_{ox}\mu_{n-acc}(V_g/k)}{(T_{ox}/k)q\mu_n n(x)(S/k)}+1\right)^{-1}+1\right)\gamma_n' - 1 = \frac{2qD_p}{J}\frac{(S/k)}{W}\left(k\frac{dn}{dx}\right) \quad (8)$$

The right hand side of (8) is equal to that of (6). For the left hand side of (6) and (8), following relationship is held for $k > 1$.

$$\frac{\varepsilon_{ox}\mu_{n-acc}V_g}{T_{ox}q\mu_n n(x)S} < \frac{\varepsilon_{ox}\mu_{n-acc}(V_g/k)}{(T_{ox}/k)q\mu_n n(x)(S/k)} \quad (9)$$

It leads higher injection efficiency from the Cathode side.

$$\gamma_n' > \gamma_n \quad (10)$$

It leads higher carrier concentration in the N-Base Cathode side and lower on-state voltage drop. It means the device characteristic improvement can be obtained by scaled Cathode structure and applying same electric field for the gate oxide.

Other electrical characteristics are changed by introducing the scaling factor k as Table 2: The gate-emitter capacitance C_{ge} is unchanged because $T_{ox}'=T_{ox}/k$ and $D_p'=D_p/k$. The gate charge Q_g is reduced by the scaling factor k as described before, $Q_g'=Q_g/k$. The current density of the contact metal J_{Metal} is increased by the scaling factor k, $J_{Metal}=k J_{Metal}$ because the contact hole width is reduced by k. Electro migration should be considered for large k structures.

One characteristic that the principle fails to scale is the threshold voltage. The threshold voltage V_t can be calculated as following

$$V_t = \frac{\sqrt{2\varepsilon_0\varepsilon_{Si}qN_A\phi_S}}{C_{ox}} + \phi_S \quad (11)$$

Where C_{ox} is the gate capacitance per unit area, N_A is the acceptor concentration and ϕ_S is the surface potential of the MOS channel. V_t is reduced because the gate capacitance per unit area is increased by the scaling principle as $C_{ox}'=kC_{ox}$. But the V_t is not scaled by k exactly. To adjust the threshold voltage so that keeping scaling principle, $V_t'=V_t/k$, the P-Base doping concentration at the junction between the N-Emitter and P-Base should be set as following.

$$N_A' = \frac{(kC_{ox})^2(V_t/k - \phi_S)^2}{2\varepsilon_0\varepsilon_{Si}q\phi_S} \quad (12)$$

Established scaling principle is summarized in

Table 2.

Table 2. Established scaling principle.

Parameters and Characteristics	Symbol	Scaling Factor k
Cell Width	W	1
Trench-Trench Spacing	S	$1/k$
P-Base Depth	D_P	$1/k$
P-Base Doping Concentration	$CP\text{-}Base$	Eq.(12)
Trench Depth	D_T	$1/k$
Gate Oxide Thickness	T_{ox}	$1/k$
Gate Voltage	V_g	$1/k$
Estimated Gate Resistance	R_g	1
Electric Field in Gate Oxide	E_{ox}	1
Gate-Emitter Capacitance	C_{ge}	1
Gate Charge	Q_g	$1/k$
Current Density of Contact Hole	J_{Metal}	k
On-state Voltage Drop	$V_{ce}(sat)$	<1
Electron Injection Efficiency	γ_n	>1
Stored Carrier Density	n	>1

2. Further trade-off improvement for on-state voltage drop and turn-off loss

As calculated before, the breakdown voltage is improved by applying the scaling principle because narrower trench-trench spacing relaxes the electric field around the bottom of the trench. With large scaling factor, the electric field distribution should be closed to that of an ideal one-dimensional BJT structure. The margin of the N-Base thickness can be reduced with incrementing k. It leads further performance improvement.

TCAD simulations with adjusted N-Base thickness were performed. The structure parameters are shown in

Table 3. The N-Base thickness *tN-Base* is set to obtain similar breakdown voltage of k=1 as shown in Figure 7. Calculated I_c-V_c characteristics are shown in Figure 8. As comparing with Figure 2, on-state voltage drop improvement of the reduced N-Base thickness devices are greater than simply scaled devices.

Table 3. Structure parameters used for the scaling principle verification with reduced N-Base thickness.

Scaling Factor k	1	3	5
W[um]	16.0	16.0	16.0
D_T[um]	6.0	2.0	1.2
D_P[um]	3.0	1.0	0.6
S[um]	3.0	1.0	0.6
T_{ox}[A]	1000	333	200
V_g[V]	15.00	5.00	3.00
$CP\text{-}Base$[x10^{17}cm^{-3}]	2.80	4.00	4.80
tN-Base[um]	120	110	100

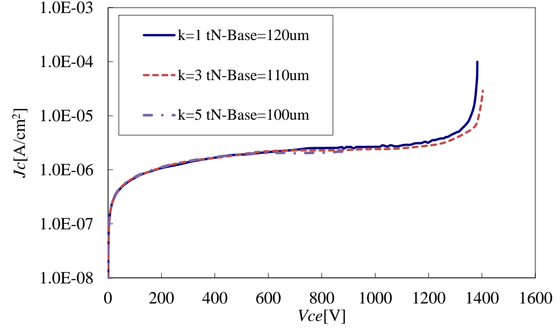


Figure 7. Calculated breakdown characteristics for scaling factor k=1, 3, 5 with reduced N-Base thickness.

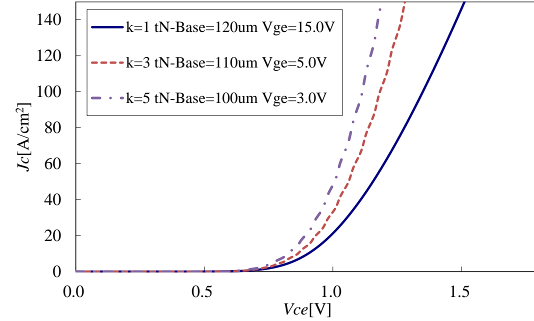


Figure 8. Calculated I_c-V_c characteristics for scaling factor k=1, 3, 5 with reduced N-Base thickness.

3. Conclusion

We proposed new scaling principle for the Trench gate IGBT to make compatibility with the CMOS large diameter wafer process. By the principle, the scaled device has shallower trench gate, shallower P-Base and thinner gate oxide. The scaled device can have process compatibility to the CMOS with better process uniformity and no wafer bowing.
In spite of the shallower trench gate, lower on-state voltage drop can be obtained by applying scaled gate voltage which gives same electric field in the gate

oxide. The improvement was simulated by two-dimensional TCAD and theoretically proved by referring our previously proposed compact model. Additionally, further improvement was predicted by reduced N-Base thickness margin.
The principle has large impact to be used for new IGBT development direction. The productivity should be improved dramatically because it is formed on the large diameter wafer with smaller thermal budget and shorter etching time.

Appendix: N-Base modelling

Figure 9 shows cross-sectional view of the trench gate IGBT. The N-Base carrier concentration $n(x)$ can be formulated by the ambipolar equation that has the carrier lifetime τ and diffusion length L_A of high injection condition [20].

$$L_A^2 \frac{d^2 n(x)}{dx^2} = n(x) + \tau \frac{dn(x)}{dt} \qquad (10)$$

For the steady state conditions, the time dependent term is omitted and the solution can be formed as [21]

$$n(x) = L_A \frac{-\frac{dn}{dx}(x_1)\cdot\cosh\left(\frac{x_2 - x}{L_A}\right) + \frac{dn}{dx}(x_2)\cdot\cosh\left(\frac{x - x_1}{L_A}\right)}{\sinh\left(\frac{x_2 - x_1}{L_A}\right)}$$

(11)

where x_1 and x_2 are the positions of Anode edge and Cathode edge of the N-Base region as shown in Figure 9. Eq.11 means that the N-Base carrier distribution depends on the differentials of the carrier distribution at both edges.
Following differential equation of the carrier density can be also formulated in the N-Base region.

$$\mu_p J_n - \mu_n J_p = 2\mu_p \mu_n kT \frac{dn}{dx} \qquad (12)$$

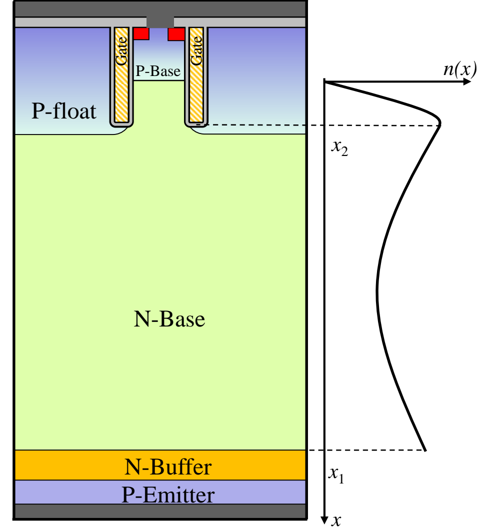


Figure 9. On-state carrier distribution

The differentials can be obtained as follows.

$$\frac{dn}{dx}(x_1) = -\frac{J\left(\gamma_p - \frac{\mu_p}{\mu_p + \mu_n}\right)}{2\frac{\mu_p \mu_n}{\mu_p + \mu_n} kT} \qquad (13)$$

$$\frac{dn}{dx}(x_2) = \frac{J\left(\gamma_n - \frac{\mu_n}{\mu_p + \mu_n}\right)}{2\frac{\mu_p \mu_n}{\mu_p + \mu_n} kT} \qquad (14)$$

where γ_p and γ_n are the hole injection efficiency at the Anode side and the electron injection efficiency at the Cathode side, respectively.

$$\gamma_p = \frac{J_p(x_1)}{J} \qquad (15)$$

$$\gamma_n = \frac{J_n(x_2)}{J} \qquad (16)$$

The voltage drop in the N-Base can be calculated based on the stored carrier concentration.

$$V_{N-base} = -\frac{(\mu_n - \mu_p)\cdot kT}{(\mu_n + \mu_p)\cdot q}\int_{x=x_1}^{x_2}\frac{1}{n}\frac{dn}{dx}dx + \frac{J}{q(\mu_n + \mu_p)}\int_{x=x_1}^{x_2}\frac{1}{n}dx$$

(17)

From these equations, the on-state N-Base carrier distribution can be calculated by γ_p and γ_n. In the other words, by keeping γ_p and γ_n as constants, same carrier distribution and voltage drop are obtained even if the structure is scaled. The scaling principle is based on this idea.

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