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Scaling Rule for Very Shallow Trench IGBT toward CMOS Process Compatibility

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***Abstract*—Deep trench gate is used for latest IGBT to improve device performance. By large difference from deep submicron CMOS structure, there is no process compatibility among CMOS device and trench gate IGBT. We propose IGBT scaling rule for shrinking IGBT cell structure both horizontally and vertically. The scaling rule is theoretically delivered by structure based equations. Device performance improvement was also predicted by TCAD simulations even with very shallow trench gate. The rule enables to produce trench gate IGBT on large diameter wafer in CMOS factory with superior productivity.**

Keywords: 300-450mm wafer, CMOS process, Shallow trench

I. INTRODUCTION

The 300mm to 450mm wafer CMOS technology enhances the mass-productivity in digital integrated circuits, and hence every semiconductor devices, including power semiconductors, will be forced to be designed in the compatibility of the large diameter wafer process technology, so that IGBTs won't be an exception. In previous works, rather deep trench gate structures have been employed to improve the device performance ([1]-[4]) under present process technology standard for discrete power. Some extreme structures such as nanometer trench-trench spacing have been demonstrated showing limits and possibilities of the future IGBT ([5]-[7]).

In this paper, we theoretically show a roadmap of IGBT technology by the scaling rule with a factor "*k*". Scale down concept is shown in Fig. 1. The ratios of the design parameters are maintained similar to CMOS scaling for all scaling factor *k*. We show the simulation results to prove the scaling rule for IGBT design in scaled structure with shallower trench gate, lower thermal budget, shallower doping and etching processes similar to CMOS scaling roadmap [8]. Based on previously proposed "Structure Oriented" analytical model [9], the scaling rule is established and the results show that very shallow structure even improves the performance of IGBT. This scaling rule can predict the device performance with high scaling factor because the proposed model shows high accuracy for wide range of structure and temperature.

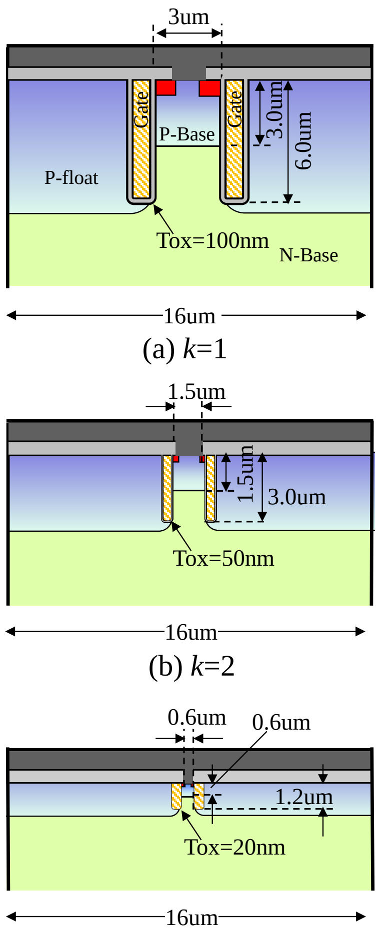

Fig. 1. Concept of trench gate IGBT scaling rule.

II. IGBT SCALING RULE

A. *Cathode Side Formulation by "Quasi-2D MOS-ADE" model*

We firstly modelled Cathode side injection efficiency by only structure parameters of trench gate IGBT. The model, named "Quasi-2D MOS-ADE model", is simple yet very accurate for wide range of structure parameters and device temperature. In this model, the electron current flowing from MOS gate is assumed to be divided for two paths, mesa region between trenches under P-Base and accumulation layer of MOS gate, as shown in Fig. 2.

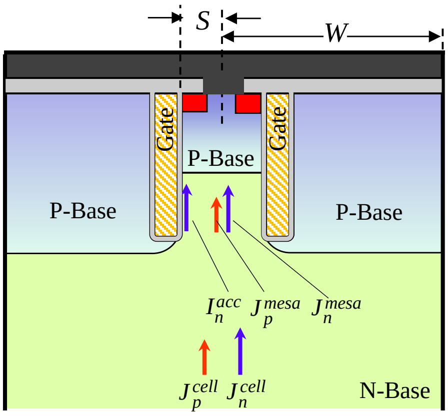

Fig. 2. Current flow of trench gate IGBT. Electron current in mesa region is assumed to divide J_n^{mesa} and I_n^{acc}.

First, the electron current flowing in mesa region (J_n^{mesa}) is modelled as following. The electron and hole are assumed to distribute one dimensionally. And they keep same concentration by conductive modulation. In result, following differential equation can be formed as ADE (Ambipolar Diffusion Equation).

$$\mu_p \cdot J_n^{mesa} - \mu_n \cdot J_p^{mesa} = 2 \cdot \mu_p \cdot \mu_n \cdot kT \frac{dn}{dx} \qquad (1)$$

Where μ_p, μ_n and n are the mobility for hole, electron and carrier concentration, respectively.

Second, the electron current flowing via the accumulation layer of trench MOS gate (I_n^{acc}) can be formed with the electron mobility of the accumulation layer μ_{acc}, accumulated charge Q_{acc} and potential ϕ_n as following.

$$I_n^{acc} = -\mu_{acc} \cdot Q_{acc} \frac{d\phi_n}{dx} \qquad (2)$$

Here, we assume same potential is applied for both electron current elements.

By considering cell width W and mesa width S as shown in Fig. 2, following equations can be formed for cell current and mesa current.

$$W \cdot J_p^{cell} = S \cdot J_p^{mesa} \qquad (3)$$

$$W \cdot J_n^{cell} = I_n^{acc} + S \cdot J_n^{mesa} \qquad (4)$$

Following differential equation can be established by combining (1) to (4).

$$\left(\frac{\mu_p}{\mu_n} \left(\frac{\mu_{acc} \cdot Q_{acc}}{q \cdot \mu_n \cdot n(x) \cdot S} + 1 \right)^{-1} + 1 \right) \gamma_n - 1 = \frac{2q \cdot D_p}{J} \frac{S}{W} \frac{dn}{dx} \qquad (5)$$

Where γ_n is electron injection efficiency from trench structure. It will be fundamental equation for the scaling rule.

B. The IGBT Scaling Rule

Proposed scaling rule is summarized in Table 1. The rule is theoretically delivered from previous equation. Equation (5) indicates that the scaled device has same injection efficiency of original device with following conditions:

$$\frac{\mu_{acc} \cdot Q_{acc}}{q \cdot \mu_n \cdot n(x) \cdot S} = const. \qquad (6)$$

$$\frac{S}{W} \frac{dn}{dx} = const. \qquad (7)$$

By applying the scaling rule with scaled electric field in gate oxide as $E_{ox}' = E_{ox}/k$, (6) and (7) are held completely. Gate voltage is squarely scaled as $V_g' = V_g/k^2$ in this case.

By applying the scaling rule with constant electric field in gate oxide as $E_{ox}' = E_{ox}$, the left hand side of (6) should be higher. So, higher γ_n and lower $V_{ce}(sat)$ are obtained. Gate voltage is scaled as $V_g' = V_g/k$ in this case. IGBT performance improvement can be done with shallower trench, without higher stress for gate oxide by the scaling rule.

Table 1. Summary of proposed scaling rule

Parameters	**Scaling Ratio**	
	Electric field in gate oxide $E_{ox}'=E_{ox}/k$	Electric field in gate oxide $E_{ox}=constant$
Gate voltage V_g	$1/k^2$	$1/k$
Half P-Base width S	$1/k$	
Half cell pitch W	1	
N-Emitter width W_E	$1/k$	
Trench depth D_T	$1/k$	
P-Base depth D_P	$1/k$	
N-Emitter depth D_E	$1/k$	
Half contact hole width W_C	$1/k$	
Gate oxide thickness T_{ox}	$1/k$	
Gate-Emitter capacitance C_{ge}	1	
Gate-Collector capacitance C_{gc}	1	
Collector-Emitter capacitance C_{ce}	$1/k$	
Current density in contact hole J_{ch}	k	
Gate charge Q_g	$1/k^2$	$1/k$
Electron injection efficiency γ_n	1	>1
Stored carrier density $n=p$	1	>1

III. Calculation Results and Discussions

Two-dimensional TCAD simulations were performed to prove the scaling rule and predict performance improvement. 1.2kV-class Field-Stop type IGBT structures were assumed.

A. *On-state characteristic*

I_c-V_c characteristics of scaled devices with scaled electric field in gate oxide as $E_{ox}'=E_{ox}/k$, are shown in Fig. 3. The curves for k=1 and 2 show good agreement but more scaled devices show smaller saturation current. It is due to V_{th} shift by the scaling.

$$V_{th} = \frac{\sqrt{2\varepsilon_0 \varepsilon_{Si} q N_A \phi_S}}{C_{ox}} + \phi_S \qquad (8)$$

Where C_{ox} is gate capacitance per unit area, N_A is acceptor concentration in P-Base and ϕ_S is surface potential of MOS channel. V_{th} is reduced by scale down because gate capacitance per unit area is increased as $C_{ox}'=kC_{ox}$. But V_{th} is not scaled by k exactly even if N_A and ϕ_S are unchanged.

I_c-V_c characteristics with constant electric field in gate oxide as $E_{ox}'=E_{ox}$, are shown in Fig. 4. Lower $V_{ce}(sat)$ is obtained by scale down. On-state carrier distribution in N-Base region is shown in Fig. 5. Cathode side carrier concentration is increased by scale down. Higher γ_n and lower $V_{ce}(sat)$ are achieved by scale down even with shallower trench, as mentioned in previous section.

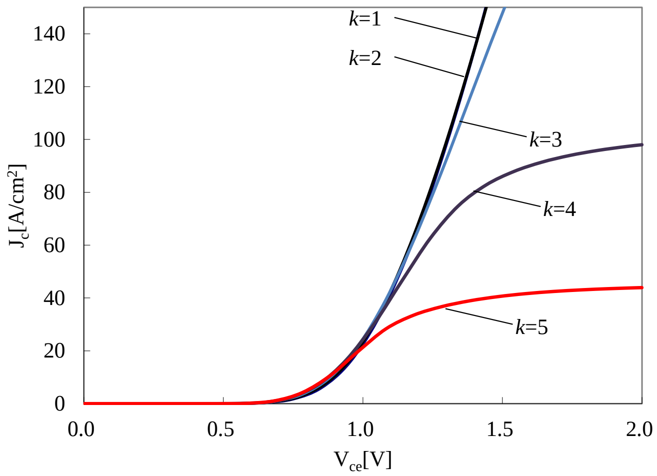

Fig. 3. Calculated I_c-V_c characteristics of scaled devices with scaled electric field in gate oxide as $E_{ox}'=E_{ox}/k$. k=1 and 2 show good agreement but more scaled devices show lower saturation current.

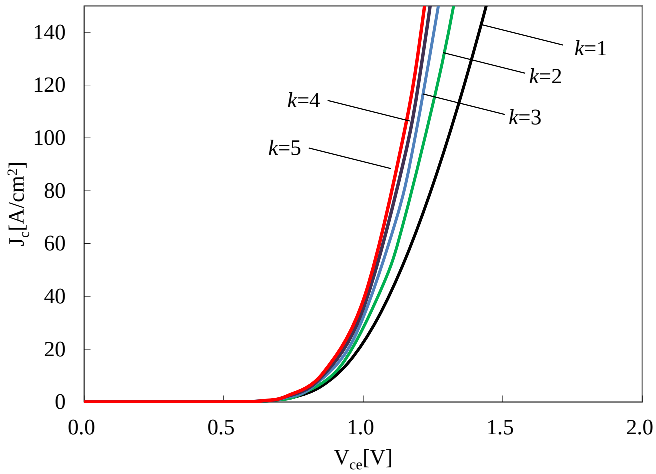

Fig. 4. Calculated I_c-V_c characteristics of scaled devices with constant electric field in gate oxide as $E_{ox}'=E_{ox}$. $V_{ce}(sat)$ is improved by increasing scaling factor k.

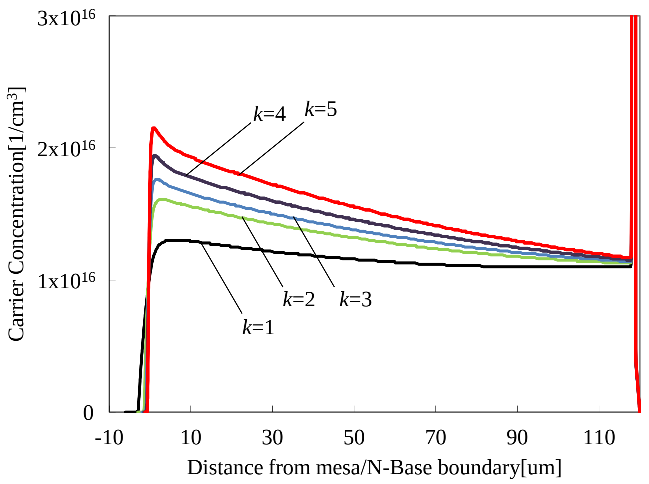

Fig. 5. Calculated carrier distribution in N-Base region for scaling factor k=1 to 5. The zero point of horizontal scale is set to mesa/N-Base boundary. Cathode side carrier concentration is increased by scale down.

B. *Turn-off characteristic*

Turn-off waveforms of scaled devices with constant electric field in gate oxide are shown in Fig. 6. External gate resistance is constant. Scaled devices show slight delays because the difference of gate voltage and threshold voltage, (V_{ge}'-V_{th}'), is not scaled by k exactly. The length of miller plateau is constant because of C_{ge} and C_{gc} are constant.

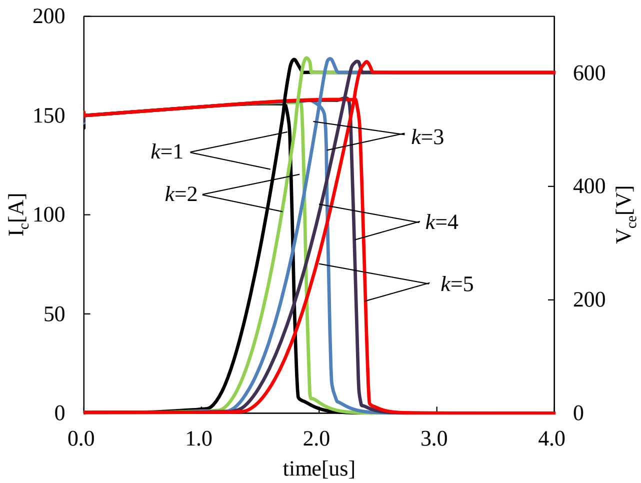

Fig. 6. Calculated Turn-off characteristics of scaled devices with constant electric field in gate oxide as $E_{ox}'=E_{ox}$ and same external gate resistance.

C. *Short-circuit characteristic*

Short-circuit waveforms of scaled devices are shown in Fig. 7. Scaled device shows slightly higher saturation current because (V_{ge}'-V_{th}') is not scaled by *k* exactly.

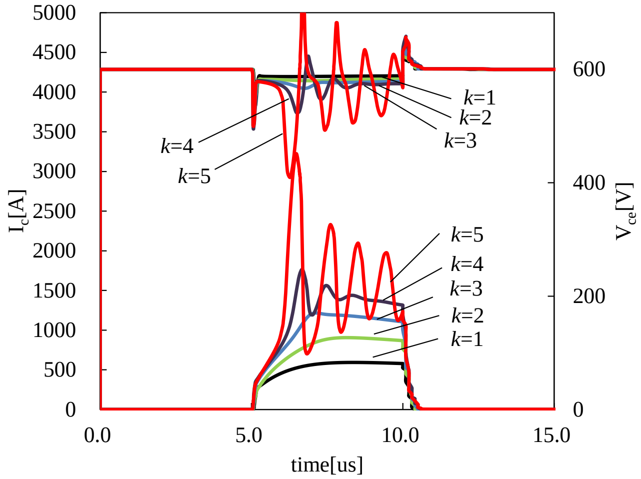

Fig. 7. Calculated short-circuit waveforms of scaled devices with constant electric field in gate oxide as $E_{ox}'=E_{ox}$.

IV. Conclusion

We proposed trench gate IGBT scaling rule, which is theoretically delivered from "Quasi-2D MOS-ADE model". The rule is simple and accurate as demonstrated by two-dimensional TCAD simulations. The scaling rule theoretically proves, for the first time, that the higher carrier storage is realized with shallower trench gate and shallower doping structure.

The scaling down in the trench IGBT structure accomplishes both the higher device performance and the higher compatibility to the large diameter wafer process with reduced trench depth, thermal budget, doping depth and oxide thickness. The collector-emitter voltage drop has significantly reduced with the scaling factor without increasing gate oxide electric field stress.

The proposed scaling rule represents a possibility of technology direction and roadmap for future IGBT for improving the device performance with high volume productivity by CMOS compatible large diameter wafer technology.

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