High Speed Turn-on Gate Driving for 4.5kV IEGT without Increase in PiN Diode Recovery Current

High Speed Turn-on Gate Driving for 4.5kV IEGT without Increase in PiN Diode Recovery Current

Yamato Miki[1], Makoto Mukunoki[2], Takashi Matsuyoshi[1], Masanori Tsukuda[1,3], and Ichiro Omura[1]

[1]Kyushu Institute of Technology, 1-1 Sensui-cho, Tobata-ku, Kitakyushu-city, Fukuoka, 804-8550, JAPAN.
[2]Toshiba Mitsubishi-Electric Industrial Systems Corporation
Mita 43 Building 13-16 Mita 3 chome, Minato-ku Tokyo, 108-0073, JAPAN.
[3]The International Centre for the Study of East Asian Development, Kitakyushu
11-4 Otemachi, Kokurakita-ku, Kitakyushu-city, Fukuoka, 803-0814, JAPAN.
E-mail: m349536y@tobata.isc.kyutech.ac.jp, omura@ele.kyutech.ac.jp

Abstract— **4.5 kV IEGT turn-on loss reduction is experimentally and numerically achieved by employing the proposed simple two step gate drive method without affecting PiN diode reverse recovery performance. It was found that 14% of turn-on loss is reduced only by the simple method. This study determines, for the first time, the optimum gate driving in the two step gate drive which can reduce IEGT turn-on loss maximally without affecting PiN diode reverse recovery performance by TCAD simulation. The method is simple yet effective for reducing switching loss of high voltage IEGT.**

Keywords-component; IGBT, IEGT, PiN diode, switching loss

(a)

(b)

Fig.1. Two step gate drive circuit (a) designed 4.5kV IEGT and PiN diode (b)

I.   INTRODUCTION

Switching loss reduction of high voltage power device has been required for downsizing of high power inverters. In addition to improving the device design, gate control technology is potentially effective to reduce the switching loss. In conventional approach, however, IEGT switching loss has been reduced simply by using smaller gate resistance inducing high *di/dt*, *dv/dt* increase. Specially, the PiN diode reverse recovery current increases with the small gate resistance and which can cause device failure or oscillation in PiN diodes dynamic waveform. The trade-off relation between the IEGT turn-on loss reduction and the increase in PiN diode reverse recovery current has been the problem for the reduction of switching loss with reduction of gate resistance. The two step gate drive methods have been proposed to solve this problem. In previous works ([1]-[4]), however, the 2nd gate time interval Δt has not been clearly determined and thus the loss has not been sufficiently reduced.

In this paper, new gate driving method with the two step drive method is proposed for reducing turn-on loss of IEGT, for the first time, without affecting PiN diode reverse recovery performance. We firstly simulate 4.5kV IEGT Turn-on loss reduction effect by adjusting the 2nd gate time interval Δt of the two step gate drive method by 2-dimentional T-CAD simulation. And then the method was experimentally demonstrated.
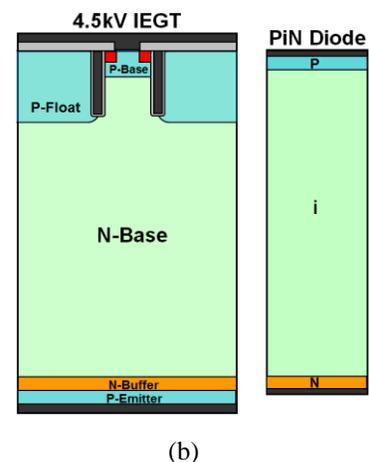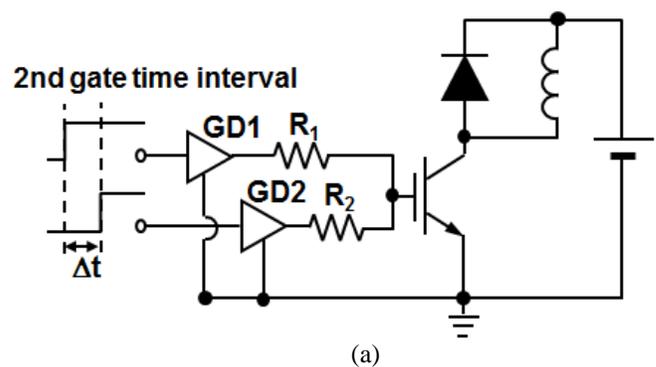
II.   IEGT TURN-ON LOSS REDUCTION

IEGT turn-on loss is reduced by two step gate drive method and loss reduction effect varies for 2nd gate time interval Δt. Figure 1(a) shows schematic circuit for the driving method. The two step gate drive circuit consists of two paralleled gate drive. The 2nd gate pulse is delayed from 1st gate pulse with time interval of Δt. First, the MOS gate of IEGT starts to be charged through R_1. Once 2nd gate is triggered, gate resistance becomes equivalent to paralleled combination of R_1 and R_2 and thus the IEGT MOS gate is

charged up in shorter time. In the new driving method, 2nd gate is triggered so that the waveform before collector current peak (reverser recovery current peak for diode) is not affected by the 2nd gate driving.

A. Simulation Results

The loss reduction effect is confirmed with 2-dimensional T-CAD simulation with varying the 2nd gate time interval Δt. The simulated 4.5kV IEGT and PiN diode structure is schematically shown in Fig.1 (b). The active areas of IEGT and PiN Diode are 1cm^2 and 0.5cm^2 respectively. The simulation condition is 2250V for DC voltage under collector current of 30A. 1st gate resistance is100Ω and 2nd gate resistance is 2Ω. The simulation results is shown in Fig.2. It is found that the turn-on loss of IEGT is gradually reduced with decrease of the2nd gate time interval Δt, while the loss of PiN diode is increased. IEGT turn-on loss and total loss are respectively reduced by 53% and 34% at Δt=1.65μs.
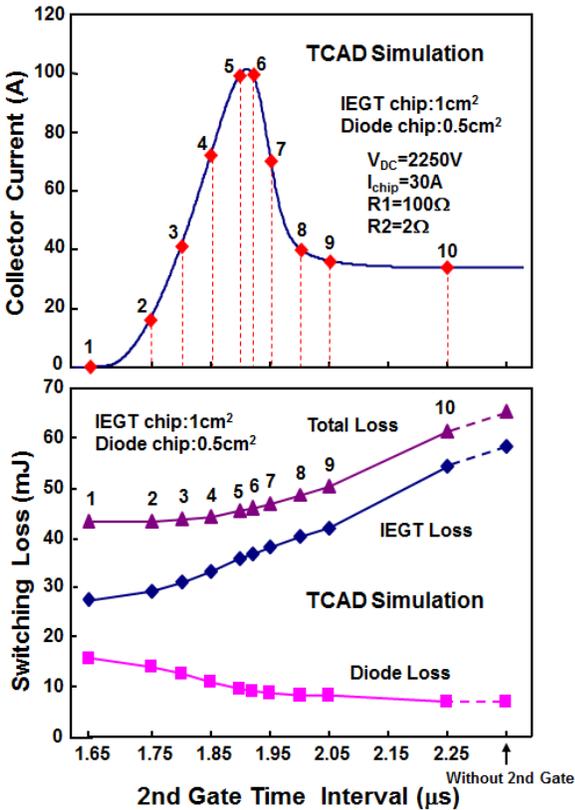

Fig.2. The timing of 2nd gate driving and loss reduction effect by changing 2nd gate time interval Δt obtained by T-CAD simulation.

B. Experimental Results

The simulation results of IEGT turn-on loss reduction are confirmed by experiment. IEGT and PiN diode one-chip packages are used in experiment set up shown in Fig.3. The chips are pressure contacted to reduce stray inductances ([5]). The experimental results of IEGT turn-on loss reduction are shown in Fig.4. At this time, DC voltage is 2250V, collector current is 30A, IEGT chip and PiN diode chip size is 15mm X

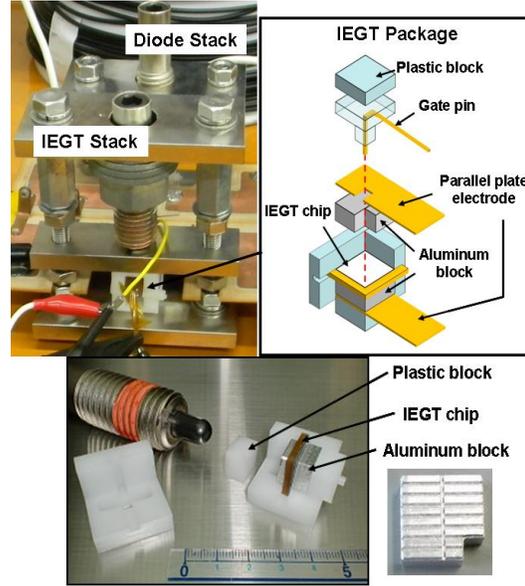15mm including edge termination area. 1st gate resistance is 100Ω and 2nd gate resistance is 30Ω.

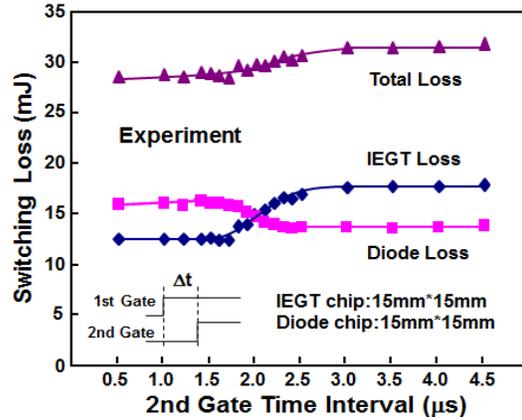Fig.3. IEGT and PiN diode single chip pressure contact package used in experiment.

Fig.4. Loss reduction effect by changing 2nd gate time interval Δt obtained by experiment.

It is found that the turn-on loss of IEGT is gradually reduced with decrease of the time interval Δt, while the loss of PiN diode is increased. These results are similar to the simulation results. IEGT turn-on loss and total loss are reduced by 30% and 10% at Δt=0.5μs respectively. Since diode chip current density is about a half of simulation condition, the loss reduction ratio is rather smaller than the simulation results.

IEGT turn-on loss and total loss are reduced with decrease of the 2nd gate time interval Δt, while peak collector current is drastically increased when the 2nd gate time interval Δt becomes shorter than a certain point as shown in Fig.5 and Fig.6. Thus the 2nd gate time interval Δt must be restricted. Under this condition IEGT turn-on loss and total loss can be

reduced without affecting PiN diode reverse recovery performance. With the restriction of time interval, loss reduction ratios are 14% and 7% at Δt=2.1μs for IEGT turn-on loss and total loss as shown in Fig.5.
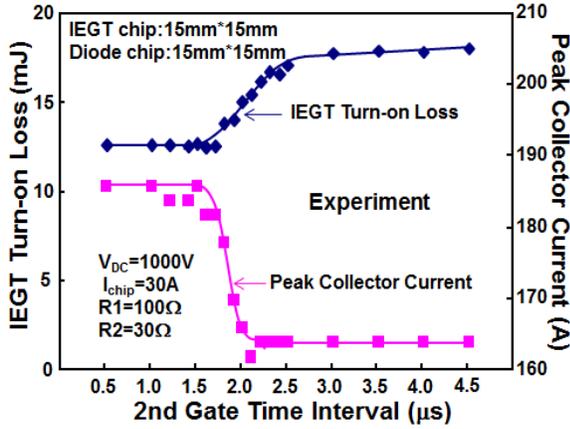

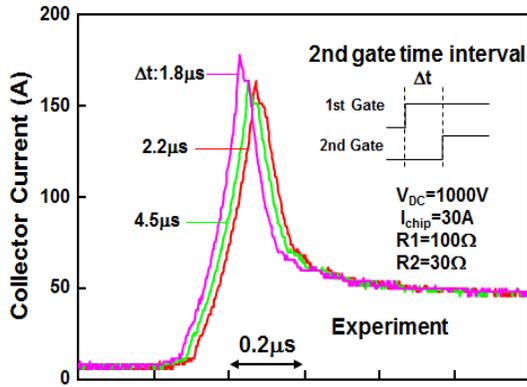Fig.5. The relation ship between IEGT turn-on loss reduction and increase in peak collector current.

Fig.6. Increase of peak collector current caused by shortening Δt.

III. DISCUSSION

A. Mechanism of increase in collector current peak

It is found that the change of peak collector current is closely related to the hole velocity in depletion region in the PiN diode (Fig. 7).

During reverse recovery, depletion layer starts to develop near the main junction of the PiN diode just after the reverse recovery current peak. In the depletion layer, holes are the carrier for reverse current with a certain velocity. If the hole velocity reached up to saturation velocity, hole density in the depletion layer is proportional to reverse recovery current ($J=qpv_s$) so that the increase in the reverse current induces increase of positive charge with the holes in the depletion layer. The positive charge negatively affects the depletion layer expansion and while the depletion layer expansion is the origin of the recovery current. This negative feedback shows the stability of current waveform even under the IEGT starting

pull down the collector voltage with the 2nd gate effect after the hole velocity reached up to the saturation velocity.

If the 2nd gate drive effects the waveform before hole velocity reaching up to the saturation velocity on the other hand, the hole current is proportional to electric field ($J=q\mu_p pE$), so that increase in the electric field in the depletion layer in PiN diode with the 2nd gate drive directly increase the reverse current.
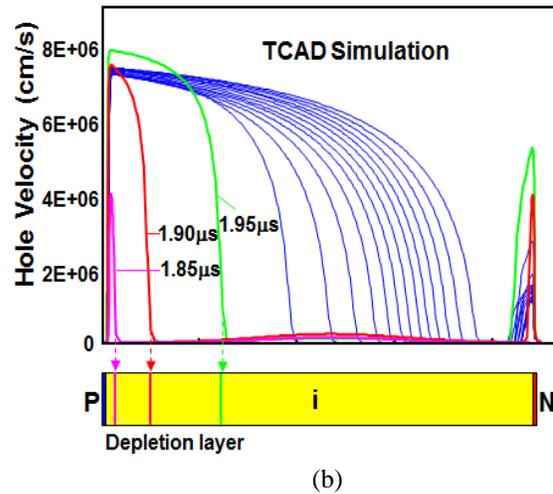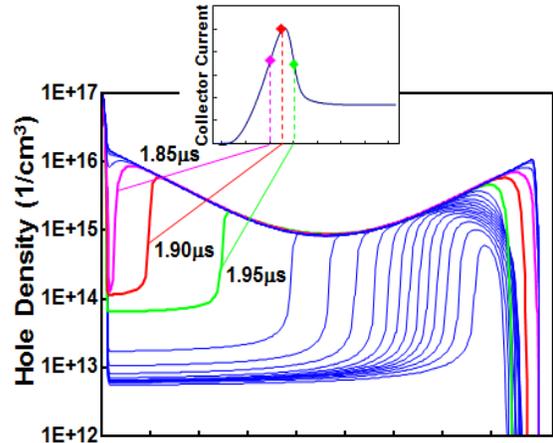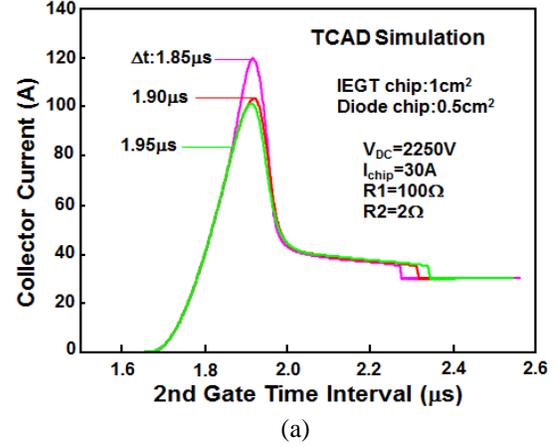

(a)

(b)

Fig.7. Increase in peak collector current (a) the time change of hole density and hole velocity in PiN diode (b).

In the simulation results shown in Fig. 7, the time interval longer than Δt = 1.90us, the velocity reached up to saturation velocity, so that no increased peak in reverse recovery current (collector current) appears. For the time interval of Δt = 1.85us, on the other hand, increased peak appears. In this simulation case, the optimum Δt is right after hole velocity reaches saturation velocity which is equal to the point of peak reverse recovery current. In simulation results, IEGT turn-on loss and total loss reduction effect are respectively 37% and 29% at Δt=1.92µs

This mechanism implies that the two step gate drive method with optimum Δt can reduce IEGT turn-on loss without affecting reverser recovery characteristics and SOA (safe operating area) of the PiN diode.

B. Effects of 2nd gate to tail current waveform

The two step gate drive forces to diode to sweep out the stored carrier with the reduction of IEGT dynamic resistance during turn-on. This can cause sudden vanishing of stored carrier resulting high *di/dt* at the tail current of the reverse recovery, specially, when small R_2 is chosen [6].
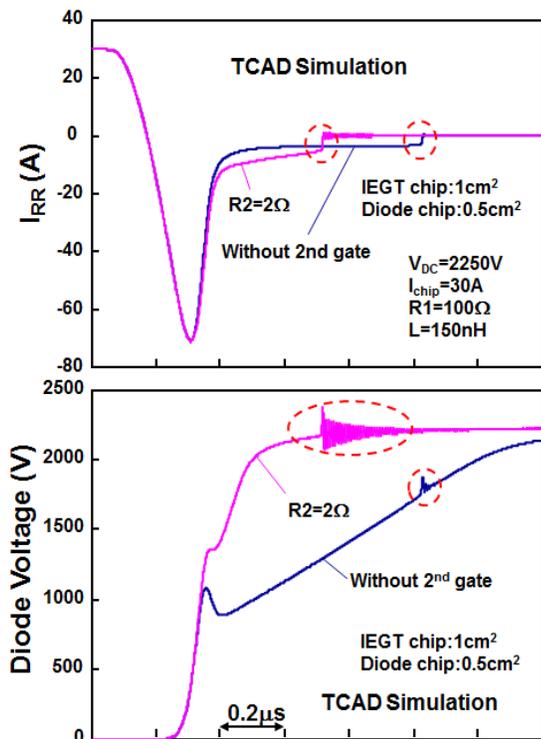

Fig.8. The ringing at step part in PiN diode reverse recovery current caused by using small 2nd gate resistance.

Figure 8 shows an example of oscillation appearing in the tail current at the end of terrace shape with the high *di/dt* when smaller gate resistance for 2nd gate of 2Ω is chosen. In the simulation 2nd gate drove after the recovery current peak with, stray inductance of 150nH.

C. Effect of 2nd gate to avalance induced loss increase

The two step gate driving method is limited in case of high reverser current density condition with such as smaller chip size or high carrier injection P-emitter. The diode reverse current after the peak must be lower than the following dynamic avalanche condition [7].

$$ J_R < qv_s \left(\frac{\varepsilon E_{crit}^2}{2q \cdot V_R} - N_{i-layer} \right) $$

Once the reverse current exceeds the limit avalanche phenomena starts near the main junction which induces re-injection of electron to the stored carriers in i-layer resulting substantial increase in switching loss.

IV. CONCLUSION

New gate driving method with the two step drive method is proposed for reducing turn-on loss of IEGT, for the first time, without affecting PiN diode reverse recovery performance. The reduction of IEGT turn-on loss was 30% for T-CAD simulation and 14% for experiment. The optimum gate drive trigger time for the 2nd gate is right after collector current peak. The limitation of this method is also discussed regarding the effect of the 2nd gate drive to the tail current oscillation and avalanche induced loss increase.

REFERENCES

[1] K. Ogawa, K. Ishikawa, S. Yukutake, N. Kameshiro H. Onose, M. Nagasu, "Development of Low Surge Voltage Driver for SiC Hybrid Module," JIASC2012, pp. 173-175, 2012 (in Japanese).

[2] N. Sakurai, "Reduction of IGBT Switching Delay Time and Switching Loss with Restraining Surge Voltage and Noise Caused by Ringing," Japan Patent JP2009-54639A (in Japanese).

[3] K. Ishikawa, M.Nagasu, Tsugawa, "Reduction of IGBT Turn-on Loss and SiC Diode Recovery Loss with Reducing the Noise Caused by Ringing," Japan Patent JP2008-92663A (in Japanese).

[4] K. Ichikawa, M. Tsukakoshi, R.Nakajima, "Higher efficiency three-level inverter employing IEGTs," APEC'04, Vol.3, pp. 1663-1668, 2004.

[5] T. Matsuyoshi, M. Tsukuda, H. Hirai, I. Omura, "Development of scale down testbed for high voltage power device," IEICE Tech. Rep., Vol. IEICE-112, No. 396, pp. 105-109, January 2013 (in Japanese).

[6] M. Tsukuda, Y. Sakiyama, H. Ninomiya and M. Yamaguchi, "Dynamic Puhch-Through Desing of High-Voltage Diode for Suppressiono of Waveform Oscillation and Switching Loss," Proc. of ISPSD'09, pp. 128-131, 2009.

[7] M. Tsukuda, I. Omura, Y. Sakiyama, M. Yamaguchi, K. Matsushita and T. Ogura, "Critical IGBT Design Regarding EMI and Switching Losses," Proc. of ISPSD'08, pp. 185-188, 2008.