Ultra Low Loss Trench Gate PCI-PiN Diode with VF<350mV

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***Abstract*— PiN diode forward voltage drop was reduced to as low as 325mV by the pulsed carrier injection (PCI) mechanism with trench MOS gate as the integrated injection control switch. The conventional PiN diodes have voltage drop of about 0.8V which is equivalent to 1%-2% energy loss in home appliances. The proposed PCI-PiN diode reduces the loss by more than 50% and the diode structure has process compatibility to conventional IGBTs and trench MOSFETs for easy implementation into mass production. The authors also confirmed PCI concept with the experiment with BSIT.**

I. INTRODUCTION

The conduction threshold voltage of 0.8V for conventional PiN diode (see Fig. 1 (a)) results in the substantial loss in rectifying circuit in power electronics systems. The estimated loss due to the PiN diode is 1%-2% for home appliances. The pulsed carrier injection (PCI) concept [1] has been proposed to reduce the conduction voltage drop to the level of 0.3V (see Fig. 1 (b)), which has potential to reduce the loss in rectifying circuit.

The PCI-PiN diode is different from conventional PiN diode in carrier injection control mechanism. In the forward condition for PCI-PiN diode, holes are injected into the i-layer in pulse wise with MHz range frequency, while the holes are continuously injected during forward bias condition for the conventional PiN diode. The PCI concept device has an extra N-layer next to P-emitter in PiN diode, low voltage switches to control the hole injection from P-emitter and electron conduction from the cathode to the extra N-layer. During electron conduction pulses, the stored carriers are reduced since holes are not injected. No PN junction appears along the current path during this pulse, the conduction threshold voltage of 0.8V is eliminated. However the original concept structure needs two external switches like MOSFETs for PCI control. The switch need other power supply to operate, therefore it is not practical.

This work newly proposes a practical structure for future production of the new low loss PCI-diode. The structure is integrated the PCI control switches. And, PCI concept is confirmed by the experiment with a feasible device.

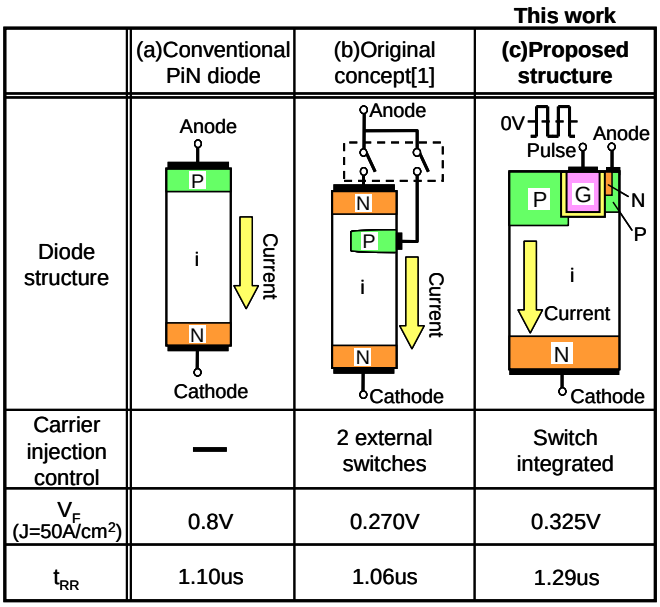
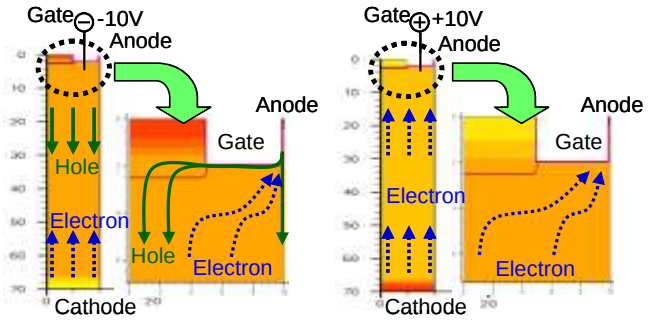


Figure 1. Schematic illustration of the conventional PiN diode, the original concept, and the practical structure. The practical structure has the trench instead of external switches.

II. SIMULATION

The new structure was demonstrated with 2-D TCAD simulations [2]. The structure has a trench MOS gate to switch the hole injection and the electron conduction in the anode of the diode during conduction state and the structure of the diode has the compatibility in fabrication process to state-of-the-art IGBTs and trench MOSFETs (see Fig. 1 (c)). Instead of external switches (see Fig. 1 (b)), the -10V/+10V square pulse voltage to form the P-channel/N-channel on the surface of the trench is applied to the gate. When the negative voltage -10V is applied, the holes are accumulated at the surface of

gate oxide around the trench i.e. the P-channel is formed, and the holes are injected from anode side into the i-layer. This mode is similar to conventional PiN diode conduction operation. We call this mode the hole injection mode (see Fig. 2 (a)). Oppositely, when the positive voltage +10V is applied, the N-channel is formed, and only the electrons flow and it is expected that no PN junction appears along current path therefore the threshold voltage of 0.8V will not be appeared during this mode. We call this mode the electron conduction mode (see Fig. 2 (b)). The average forward voltage drop is decreased by repeating the hole injection mode and the electron conduction mode.



(a) Hole density of hole injection mode

(b) Electron density of electron conduction mode

Figure 2. Behavior of carriers at hole injection mode and electron conduction mode. Holes and electrons flow at hole injection mode, while only electrons flow at electron conduction mode.

The conduction threshold voltage of 0.8V is reduced by PCI concept in this structure. Figure 3 shows the transient forward voltage drop of the proposed diode at 1MHz pulse frequency. It was confirmed that the forward voltage drop was about 0.1V during the electron conduction mode, while the 0.85V voltage drop appears during the hole injection mode. The average forward voltage drop is as low as 362mV which is more than 50% lower than the conventional PiN diode.

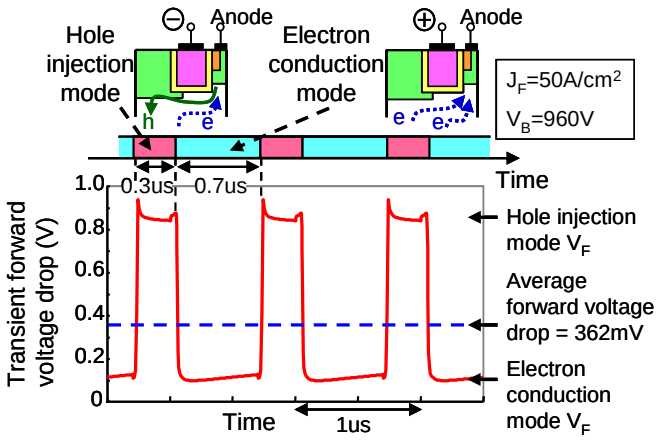


Figure 3. The transient forward voltage drop of the proposed diode at 1MHz pulse frequency at 50A/cm^2. The average forward voltage drop is as low as 362mV for this case.

The optimum average forward voltage drop V_F is changed by injection control frequency. Figure 4 shows the average V_F for various frequencies as functions of hole injection time ratio. The conditions of simulations are as follows; the gate switch frequencies are fixed various values, the time of the hole injection mode and the electron conduction mode are changed respectively. The optimum average V_F was improved as increasing of the gate switch frequency and decreasing of the ratio of the hole injection mode time. The optimum V_F of 325mV was obtained at 1MHz under the hole injection time ratio of 0.2.

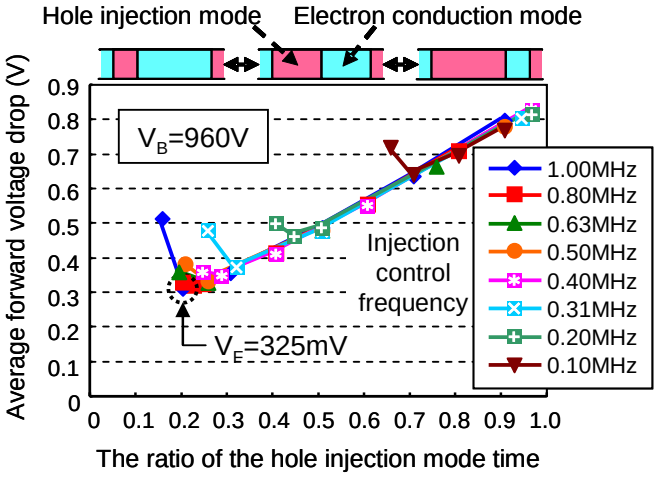


Figure 4. TCAD results of the average forward voltage drop for the proposed diode. The optimum value of 325mV was obtained with 1MHz pulse frequency at 50A/cm^2.

The comparison between the forward I-V_F characteristics of the proposed diode and that of conventional PiN diode, it seems that the conduction threshold voltage could be decreased to about 0.2V when hole injection mode time is 0.2us and electron conduction mode time is 0.8us. I-V_F characteristic is shown in Fig. 5. The simulated blocking voltage was 960V. This implies that the diode can dramatically reduce losses at diode bridge circuits in variety of appliance applications.

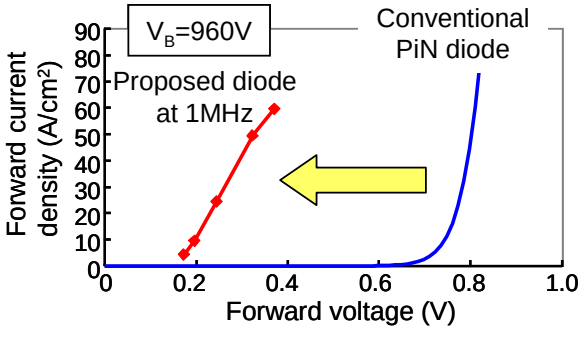


Figure 5. I-V_F characteristics. The conduction threshold voltage decreased to about 0.2V when hole injection mode time is 0.2us and electron conduction mode time is 0.8us.

The conduction losses at 50A/cm^2 including gate driving losses are shown in Fig. 6. As the injection control frequency is increased, the gate driving loss of the proposed diode is increased, while the conduction loss is gradually decreased. Thus, when the injection control frequency is extremely high, the average forward voltage drop is a little lower than the high frequency case, but the sum of these losses for the proposed diode is bigger. Considering these losses, the optimum injection control frequency is about 0.3MHz and the optimum V_F in that frequency is about 370mV. Then, the proposed PCI-PiN diode reduces the loss to about 50%.

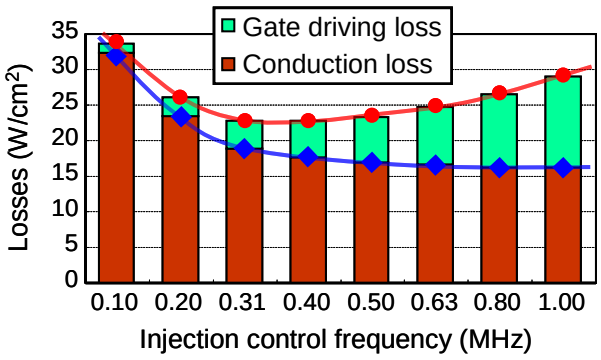


Figure 6. The conduction losses at 50A/cm^2 including gate driving losses. The optimum injection control frequency is about 0.3MHz.

The reverse recovery characteristic [3] of the proposed diode is shown in Fig. 7. After switching the hole injection mode and the electron conduction mode, reverse voltage is applied the proposed diode. Then, -10V is applied to the gate, the diode has the hole injection mode and is considered to be a usual PiN diode. The simulated reverse recovery time is about 1.29us which is sufficiently fast for rectifying 50Hz-60Hz AC current.

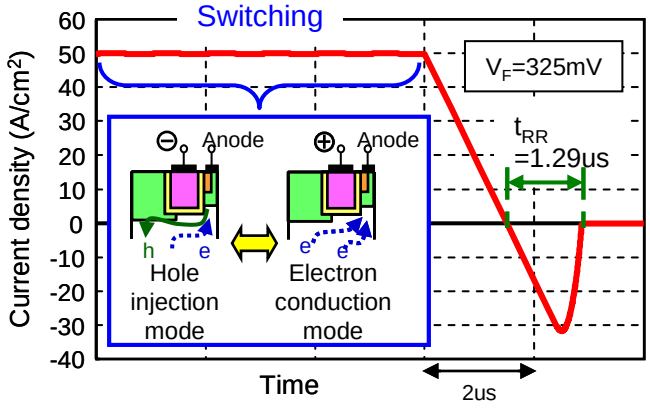


Figure 7. Reverse recoverry wave form for the proposed diode after switching. That time is about 1.29us which is sufficiently fast for rectifying 50Hz-60Hz AC current.

III. Experiment and Result

The authors experimentally verified the PCI concept by using a BSIT (Bipolar Mode Static Induction Transistor) [4]. The structure of the BSIT and the experiment circuit with the BSIT are shown in Fig. 8. The BSIT has the source N-layer, the gate P-layer and the drain N-layer, which corresponds to the cathode N-layer, the anode P-layer and the anode N-layer for the PCI-diode structure so that the concept can be experimentally demonstrated with this particular device.

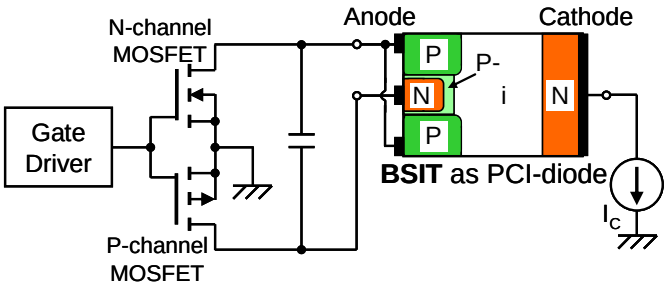


Figure 8. The structure of BSIT and the experiment circuit used BSIT. The circuit has two MOSFETs that switch the hole injection mode and the electron conduction mode. In addition, the circuit has a switch adjust the period passing a current BSIT.

The experiment circuit has N-channel MOSFET and P-channel MOSFET connected to the anode P-layer and the anode N-layer respectively, to switch the hole injection mode and the electron conduction mode. Two MOSFETs are alternately turned on and off.

When the N-channel MOSFET is turned on, the holes are injected from the anode P-layer into the i-layer in the BSIT. This mode is corresponding to the hole injection mode. Oppositely, when the P-channel MOSFET is turned on, only the electrons flow between cathode N-layer and the anode N-layer. This mode is corresponding to the electron conduction mode.

The PCI concept was experimentally demonstrated, as follows. Figure 9 shows the switching signal to two MOSFETs and the transient forward voltage drop of BSIT at 10A cathode current (I_C) at 0.1MHz pulse frequency. It was confirmed that the forward voltage drop was about 0.3V during the electron conduction mode, while the 1.1V voltage drop appears during the hole injection mode. It is verified the experiment that the PCI concept is feasible to reduce the losses with the forward voltage drop of a PiN diode. In this case, the average forward voltage drop is as low as 731mV.

The optimum average V_F is changed by switching signal frequency and I_C. Figure 10 shows the average V_F for various frequencies as functions of hole injection time ratio when I_C is 10A and the optimum average V_F when I_C is 5A and 18A. The optimum V_F of 620mV was obtained at 0.25MHz under the hole injection time ratio of 0.3. Moreover when I_C is 5A and 18A, optimum V_F of 346mV and 913mV was obtained at 0.25MHz and 0.5MHz respectively.

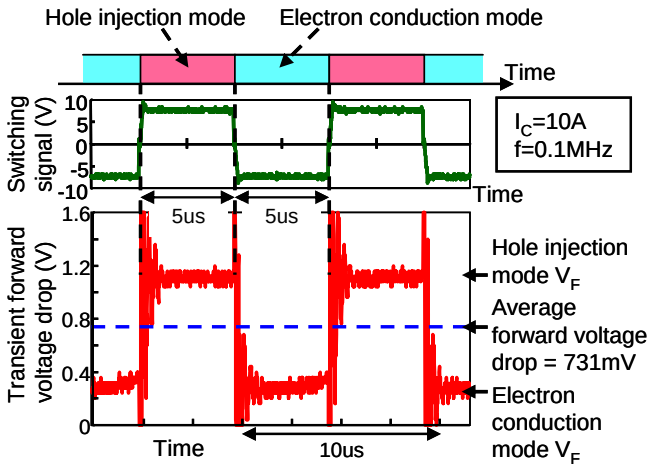


Figure 9. The transient forward voltage drop of BSIT at 0.1MHz pulse frequency when I_C is 10A. The average forward voltage drop is as low as 731mV for this case.

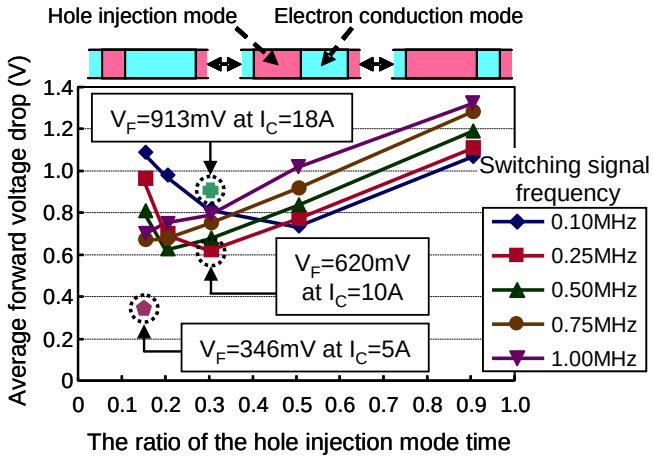


Figure 10. Experiment results of pulsed carrier injection concept with BSIT. The optimum average values of forward voltage drop are as low as 913mV at 18A and 620mV at 10A and 346mV at 5A.

It is different from the simulation that the average V_F is increased with switching signal frequency when the ratio of the hole injection mode time is high. From the transient V_F waveform, it is found the huge overshoot voltage due to the stray inductance in the circuit is appeared. The overshoot causes the increase in the average forward voltage drop at the switching (see Fig. 9).

As I_C is increased, the average V_F is increased because the voltage drops of the MOSFETs are increased by Ohm's law. It includes voltage drop due to N-channel MOSFET at the hole injection mode and P-channel MOSFET at the electron conduction mode. Therefore, the experimentally obtained average forward voltage drops in each mode are higher than the value from the simulation.

IV. Conclusion

Proposed trench gate PiN diode structure can achieve the PCI concept without external switches. The proposed PCI-PiN diode reduces the conduction loss to about 50%. This structure can be manufactured by present technologies. This concept potentially contributes to save energy because the waste of electricity is decreased and the electrical energy can be efficiently used. The PCI concept was also confirmed by the experiment.

References

[1] Yasuaki Matsumoto, "Challenge to the Barrier of Conduction Loss in PiN Diode toward VF<300mV with Pulsed Carrier Injection Concept", Proc. of ISPSD 2010, pp.119-122, 2010.

[2] Sentaurus Device User Guide Ver.A-2007.12, 2007.

[3] Hansjochen Benda and Eberhard Spenke, "Reverse Recovery Processes in Silicon Power Rectifiers", Proc. of the IEEE, Vol. 55, No. 8, August 1967, pp.1331-1354, 1967.

[4] Masayasu Ishiko, Sachiko Kawaji, Hiroshi Tadano, Susumu Sugiyama, and Haruo Takagi, "A Normally-Off Bipolar Mode Static Induction Transistor (BSIT) with High Current Gains", Proc. of ISPSD 1992, pp. 92-97, 1992.