IEICE TRANS. FUNDAMENTALS, VOL.E92–A, NO.5 MAY 2009

PAPER

A Current-Sampling-Mode CMOS Arbitrary Chaos Generator Circuit Using Pulse Modulation Approach

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SUMMARY This paper proposes a new chaos generator circuit with a current sampling scheme. This circuit generates an arbitrary nonlinear function corresponding to the time-domain current waveform supplied from an external source by using a pulse phase modulation approach. The measurement results of a fabricated chip with TSMC 0.25 μm process technology demonstrate that the proposed circuit can generate chaos signals even if D/A conversion is used for nonlinear waveform generation, because a current integral by sampling with a short pulse smooths the quantized nonlinear function.

key words: *CMOS chaos generator circuit, pulse phase modulation, current sampling*

1. Introduction

Many recent studies in neural networks have revealed the important role of nonlinear analog dynamics from the viewpoint of intelligent information processing. A chaotic neural network model [1] is a typical example. For various applications, VLSI hardware implementing such nonlinear dynamics is required.

In the VLSI implementation, digital approaches essentially cannot implement analog dynamics, although they offer high precision and controllability. Moreover, because the digital circuits require large layout areas, the digital approach cannot implement massively parallel systems on a single chip. On the other hand, analog approaches are obviously suitable for realizing continuous-time continuous-state dynamical systems. However, it is difficult to realize arbitrary nonlinear transformation including piecewise-linear functions such as the tent map because the transformation functions realized by the analog approach strongly depend on the characteristics of devices and/or circuits used [2]–[5].

As the third approach, one of the authors proposed a merged analog-digital approach that can achieve time-domain analog information processing by using pulse width/phase modulation (PWM/PPM) signals, and proposed a circuit technique generating arbitrary nonlinear functions. CMOS circuits generating arbitrary chaotic signals were also designed and fabricated [6], [7].

Some similar works were reported before. N.F. Rul'kov et al. proposed a chaotic system using pulse timing and a nonlinear waveform [8], and P.A. Bernhardt proposed a circuit in which a capacitor is charged up by a constant current source [9]. Although our circuits are partly similar to such work, our approach targets on VLSI implementation of large-scale nonlinear dynamical systems by sharing the common waveform generators.

Our ultimate goal is to analyze large-scale nonlinear dynamical systems such as the globally coupled map (GCM) [10] and the threshold coupled map [11] composed of analog circuits. The advantages of our time-domain approaches are realizing arbitrary nonlinear transformation and high controllability. Thus, we can construct large-scale flexible dynamical systems by using our approach. A possible application is chaotic neural networks for solving combinatorial optimization problems.

Our circuits proposed before use a principle of sampling of the nonlinear voltage waveform supplied externally [7]. If an analog nonlinear waveform is supplied, pure analog processing is performed in the time domain, and therefore chaotic signals can be generated. However, if we use a quantized nonlinear waveform, which can arbitrarily be generated by using D/A conversion, the voltage sampling scheme may fail to generate chaos. In order to solve this problem, we designed a current-sampling-scheme chaos generator circuit. In this sampling scheme, because the sampled charge amount is determined by current integral with PPM signals, it is expected that the realized nonlinear function is smoothed even if a quantized nonlinear waveform is used. We confirmed the effectiveness of our current-sampling scheme by HSPICE circuit simulation [12].

We have designed this circuit using TSMC 0.25 μm CMOS process technology. The measurement results of a fabricated chip demonstrate that the proposed circuit can generate chaotic signals with a low-precision quantized waveform by which the conventional voltage-sampling-scheme circuit cannot generate chaos.

2. Arbitrary Nonlinear Transformation Schemes Using Voltage or Current Sampling with Pulse Modulation Signals

The circuit principle that achieves arbitrary nonlinear transformation from voltage to voltage via PWM/PPM signals is shown in Fig. 1 [7]. The basic circuit operation is as follows:

Manuscript received October 10, 2008.
Manuscript revised December 26, 2008.

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DOI: 10.1587/transfun.E92.A.1308

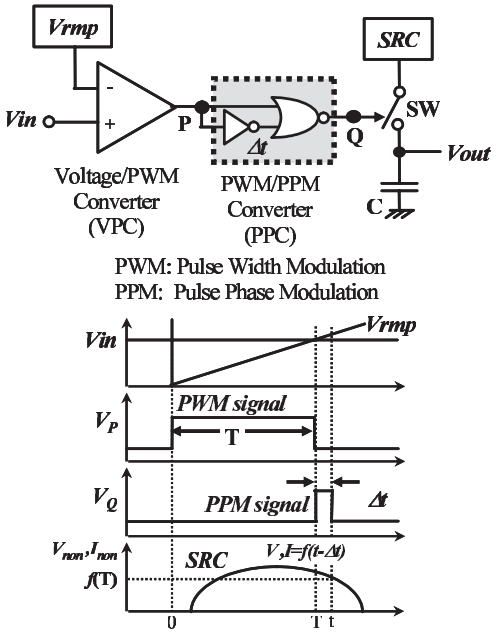


Fig. 1 Circuit principle for generating arbitrary transformation using pulse modulation: Circuit diagram and its timing diagram.

1. Input voltage V_{in} is transformed into a PWM pulse having width T. This transformation can be achieved by comparing V_{in} with ramped reference voltage V_{rmp}. If V_{rmp} is linearly ramped, then $T \propto V_{in}$.
2. The PWM pulse is transformed into a PPM pulse having a certain small width Δt and its leading edge coincides with the trailing edge of the PWM pulse. This transformation is achieved by a circuit consisting of an inverter (chain) with delay time Δt and a NOR gate.
3. Voltage or current source SRC that changes its value with a nonlinear waveform in the time domain is connected to capacitor C via switch SW. Switch SW is switched by the PPM signal, and is turned on during period $[T, T + \Delta t]$.

2.1 Voltage-Sampling Scheme

Let us consider the case where we use a voltage source as SRC, and its voltage waveform is given by $V_{non}(t) = f(t-\Delta t)$, where $f(\cdot)$ is an arbitrary nonlinear function. When SW is turned off at the trailing edge of the PPM pulse, the voltage of the capacitor node, V_{out}, is kept at $f(T)$. Here, the charging time constant is assumed small enough compared with Δt. Thus, we can obtain the following nonlinear transformation by assuming appropriate scaling:

$$V_{out} = f(V_{in}). \tag{1}$$

When the output V_{out} is fed back to the input V_{in}, the following discrete-time dynamical systems can be implemented:

$$V_{out}(t+1) = f(V_{out}(t)). \tag{2}$$

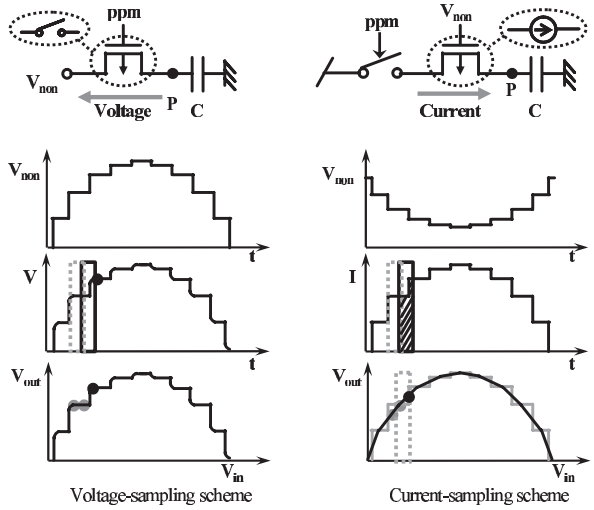


Fig. 2 Sampling schemes.

2.2 Current-Sampling Scheme

Now, let us consider the case where we use a current source as SRC, and its current waveform is given by $I_{non}(t) = Cf(t-\Delta t)$. Because the capacitor is charged up only during period $[T, T + \Delta t]$, the following discrete-time transformation can be achieved provided that $V_{out} = 0$ before sampling:

$$V_{out} = \int_{T}^{T+\Delta t} f(t-\Delta t)dt. \tag{3}$$

If Δt is small enough to neglect the change in $f(t)$, we also obtain the following nonlinear transformation:

$$\Delta V_{out} = f(V_{in})\Delta t. \tag{4}$$

Although both approaches can achieve arbitrary nonlinear transformation, if the nonlinear waveform is quantized, which occurs when a D/A converter is used, the transformation results of both approaches are slightly different. The sampling results are schematically shown in Fig. 2.

In the voltage sampling scheme, the quantization characteristics of the input nonlinear waveform are still preserved because of direct sampling of the voltage although the waveform is slightly smoothed due to the time constant of the circuit.

On the other hand, in the current sampling scheme, a current integral by sampling with a short pulse smooths the quantized nonlinear function, and therefore the realized nonlinear function is expected to be piece-wise linear.

Here, the current sampling scheme in Fig. 2(b) shows the case of using a PMOS transistor as a current source. In order to realize the function shape as shown in Fig. 2(a), a waveform with the inverse function shape should be applied to the gate of the PMOS transistor.

3. Voltage-Sampling-Mode Chaos Generator Circuit

This section briefly reviews the voltage-sampling-mode

chaos generator circuit (VSCG), which is based on the principle described in Sect. 2.1 [7]. The circuit and its operation timing diagram are shown in Fig. 3.

As the voltage/PWM converter (VPC) in Fig. 1, we use a clocked CMOS comparator. As shown in Fig. 3, the comparator consists of capacitor C, CMOS inverter I_1 and switches S_0 and S_1, which also correspond to switch SW in Fig. 1. Capacitor C in Fig. 3 is used as the capacitor in the clocked CMOS comparator and also as the sampling capacitor C in Fig. 1. Voltage source V_{non} generates a nonlinear voltage waveform, which corresponds to SRC in Fig. 1.

The circuit operation proceeds as follows. Here, the time step n is defined by the clock signal CLK and V_n indicates a voltage at each time step. The voltage of each node is represented by V with the node name as a suffix. At the initial step ($n = 0$), it is assumed that capacitor C holds the voltage difference between an initial voltage V_0 and the threshold voltage of inverter I_1, V_{th_I1}.

1. Switch S_2 is turned on by CLK, and the ramped voltage V_{rmp} is supplied at node P_L. V_{P_R} follows V_{P_L} having the above-mentioned voltage difference. Because node P_1 is "High" while $V_{P_R} > V_{th\_I1}$, S_2 is still turned on after CLK becomes "Low."
2. When V_{P_R} reaches V_{th_I1}, I_1 inverts and PWM and PPM signals are generated. The pulse width of the PWM signal corresponds to V_n. The PPM signal turns on S_0 and S_1, and capacitor C holds the voltage difference between V_{non} and V_{th1_I1} at that timing; this creates V_{n+1}.
3. After S_1 turns off, S_3 is turned on and node P_L is fixed at a predefined constant voltage V_C, which guarantees stable circuit operation. Here, voltage V_C is determined in order to satisfy the following condition: $V_{th\_I1} < V_{P_R} < V_{DD}$, where V_{DD} is the supply voltage.

Thus, the pulse width of PWM signals or the pulse timing of PPM signals T_n is updated as follows: $T_{n+1} = f(T_n)$.

4. Current-Sampling-Mode Chaos Generator Circuit

This section proposes a current-sampling-mode chaos generator circuit (CSCG). The proposed circuit is based on the current sampling scheme described in Sect. 2.2.

The proposed circuit and its operation timing diagram are shown in Fig. 4. As well as the VSCG, a clocked CMOS comparator is used as VPC, the comparator consists of I_1, C_1, S_0 and some other switches. Capacitor C_2 and switched current source SCS_2 correspond to C and SRC shown in Fig. 1, respectively.

As described in the operation of the VSCG, the time step n is defined by a set of signals SW_rst and SW_stt. On the other hand, unlike the VSCG, the proposed circuit only requires the nonlinear waveform V_{non}. No ramped voltage waveform is required. Instead of the ramped voltage source, a set of timing signals SW_rst and SW_stt is required. A constant reference voltage is supplied at node REF. The circuit operation proceeds as follows.

1. For setting an initial value, control signal SW_rst is turned to "High." The input and output of inverter I_1 are shorted, and V_{P_R} is set at the threshold voltage of in-

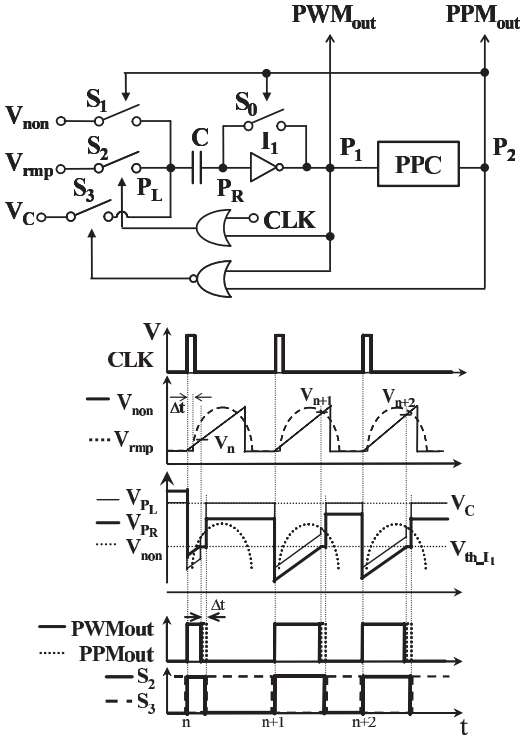


Fig. 3 Voltage-sampling-mode chaos generator circuit.

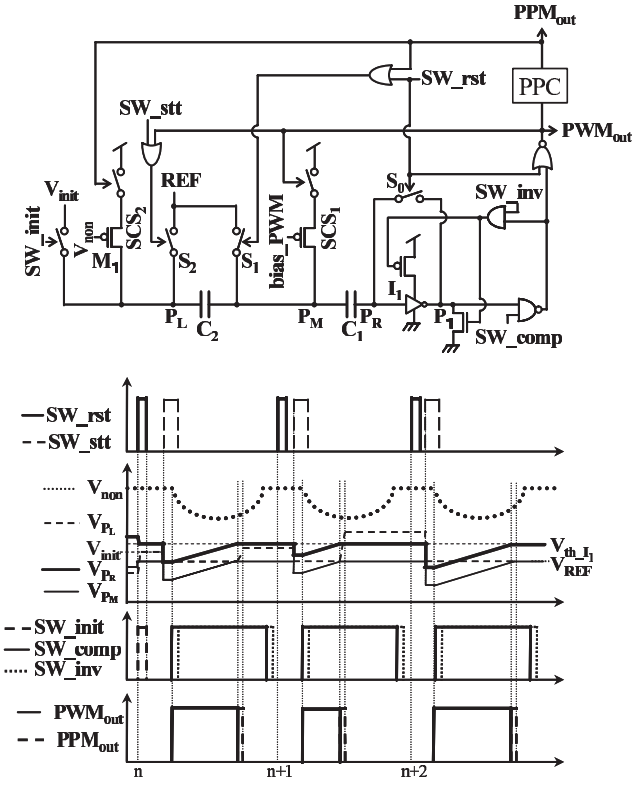


Fig. 4 Current-sampling-mode chaos generator circuit.

verter I_1, V_{inv_th}. Switch S_1 is also turned on by SW_rst, and V_{P_M} fixed at V_{REF}. At the same time, control signal SW_init is turned to "High," V_{P_L} set at initial value V_{init}. Thus, capacitor C_1 holds the voltage difference between V_{inv_th} and V_{REF}, and capacitor C_2 holds the voltage difference between V_{init} and V_{REF}. This voltage is defined by V_{chg}.

2. When control signal SW_stt is turned to "High," the node voltage V_{P_L} is fixed at V_{REF}. Thus, V_{P_M} and V_{P_R} drop by V_{chg}. Therefore, V_{P_R} falls below V_{inv_th}, and V_{P_1} is set at "High" level.
3. When control signal SW_comp is turned to "High," $V_{PWM_{out}}$ is turned to "High." Switched current source SCS_1 and S_2 turned on. Node P_L is fixed at V_{REF}, and C_1 is charged up by SCS_1, therefore V_{P_R} as well as V_{P_M} increases linearly. When V_{P_R} reaches V_{inv_th}, $V_{PWM_{out}}$ turns to "Low." Thus, PWM and PPM signals are generated from nodes PWM_{out} and PPM_{out}, respectively.
4. While V_{PPMout} is at "High" (time span Δt), S_1 and SCS_2 are turned on. Node P_M is fixed at V_{REF}, C_2 is charged up by SCS_2 with the nonlinear current waveform controlled by the gate voltage V_{non}, which creates the voltage for next time step at C_2.
5. When SW_inv is turned to "High," node P_1 is fixed at "Low" level, which guarantees stable circuit operation.

By repeating these steps, arbitrary nonlinear transformation is achieved.

5. Circuit Design, Measurement Results and Discussion

The VSCG and CSCG were designed and fabricated using TSMC 0.25 μm CMOS process technology. Both circuits were designed assuming the supply voltage of 3.3 V. The layout results and chip specifications of VSCG and CSCG are shown in Fig. 5. For the VSCG, the capacitance value of C was set at 0.8 pF. For the CSCG, the capacitance values of C_1 and C_2 were 0.5 pF and 0.9 pF, respectively. The power consumptions for the VSCG and CSCG were 625 μW and 274 μW, respectively, when the updating cycle was set at 2 μs.

Measurement waveforms in the fabricated VSCG are shown in Fig. 6. The VSCG can realize arbitrary nonlinear transformation using an appropriate nonlinear waveform V_{non}. Here, we measured about the logistic map and the tent map. The logistic map is expressed by

$$x_{n+1} = 4ax_n(1 - x_n), \tag{5}$$

and the tent map is expressed by

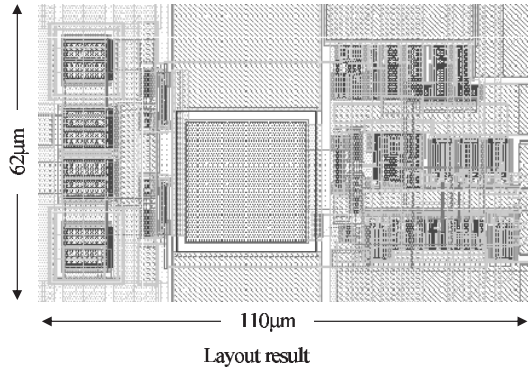
$$x_{n+1} = \begin{cases} 2hx_n & (0 \le x_n < 1/2) \\ 2h(1 - x_n) & (1/2 \le x_n \le 1), \end{cases} \tag{6}$$

where a and h are constant and were set at 0.98.

The pulse signals PWMout changes a pulse width depending on V_{non}. The duration of V_{non} was set at 1 μs, and the amplitude was set at 1 V. The waveforms V_{rmp} and V_{non} were supplied by an arbitrary waveform generator (Tektronix: AWG2021, 250 MHz). In this measurement, the time resolution of V_{non} was nearly 8 bits.

Figure 7 shows measurement results of the CSCG. In order to operate M_1 in Fig. 4 in the saturation region, V_{non} was limited from 1.5 to 2.1 V, and its amplitude was 0.6 V. The rising edges of PWMout signals were set 200 ns earlier than the onset time of V_{non} to cancel the offset pulse width, because the sampling value with a PPM signal at V_{non} = 2.1 V was converted to a PWMout signal having a 200 ns pulse width.

We made return maps for the VSCG and the CSCG using the normalized PWMout signals to compare their char-

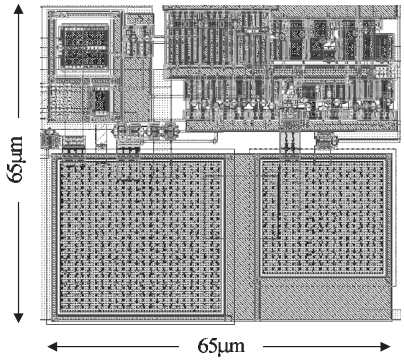


Layout result

Chip specification

Technology	0.25 μm CMOS
Chip size	62*110 μm²
Supply voltage	3.3 V
Update cycle	2.0 μs
Power consumption	625 μW

VSCG



Layout result

Chip specification

Technology	0.25 μm CMOS
Chip size	65*65 μm²
Supply voltage	3.3 V
Update cycle	2.0 μs
Power consumption	274 μW

CSCG

Fig. 5 Layout results and chip specifications for VSCG and CSCG.

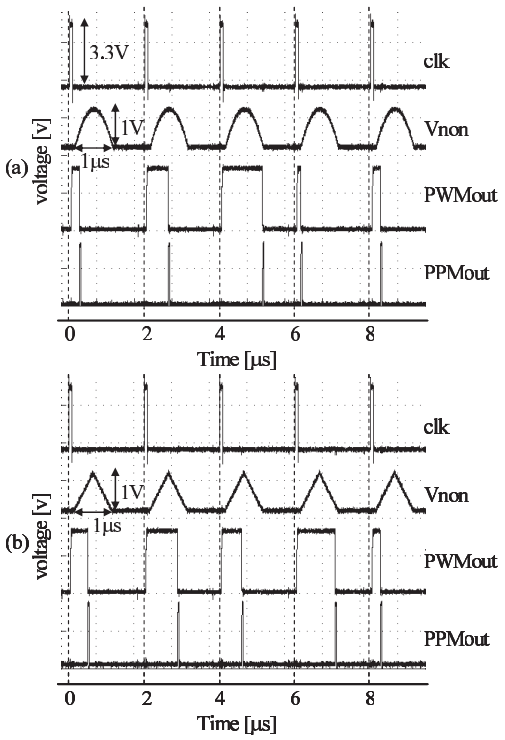


Fig. 6 Measurement result of VSCG: (a) logistic map and (b) tent map.

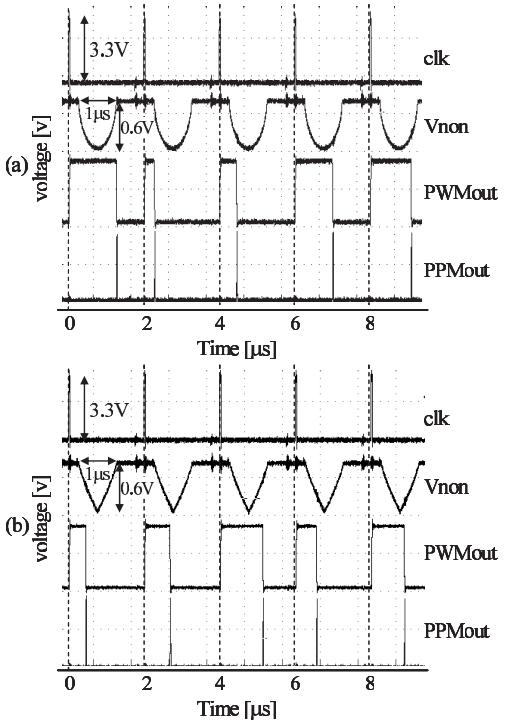


Fig. 7 Measurement result of CSCG: (a) is for logistic map and (b) is for tent map.

acteristics of nonlinear transformation. Figures 8(a), (b) and (c) show measurement results with logistic maps, tent maps, and chaotic neuron maps, respectively.

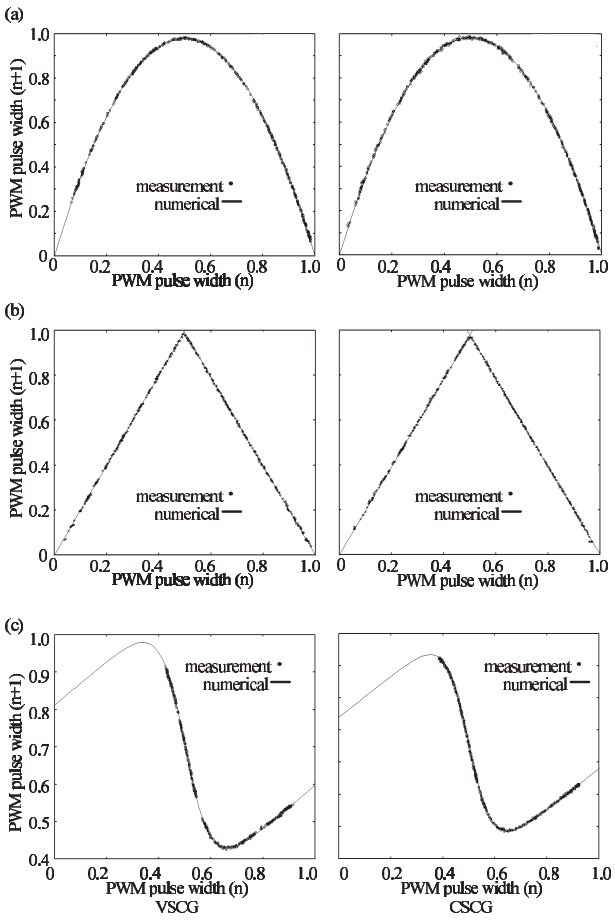


Fig. 8 Return map of VSCG and CSCG: (a) logistic map, (b) tent map and (c) chaotic neuron map.

In the return maps in Fig. 8(a), the calculation precisions for the VSCG and CSCG were 7.70 and 7.41 bits, respectively, which were obtained from root-mean-square errors between measurement and numerical calculation results. For logistic map, we set at $a = 0.98$ for both circuits. In Fig. 8(b), the calculation precisions for the VSCG and CSCG were 7.64 and 7.63 bits, respectively, where, we set at $h = 0.98$ for both circuits. The chaotic neuron map used in Fig. 8(c) is expressed by

$$x_{n+1} = b(x_n - e) - \frac{c}{1 + \exp(-(x_n - e)/d)} + p, \qquad (7)$$

where $p = 1.10$, $b = 0.59$, $c = 0.80$, $d = 0.05$, and $e = 0.5$ for the VSCG, and $p = 1.08$, $b = 0.63$, $c = 0.78$, $d = 0.04$, and $e = 0.5$ for the CSCG. In general, chaotic neuron maps deal with positive and negative values, but our circuits cannot deal with negative values. Therefore, we introduced parameter e, and the nonlinear waveform V_{non} was shifted to drive the circuit within the positive domain. The calculation precision for the VSCG and CSCG were 8.09 and 7.64 bits, respectively. From these return maps, we found that the CSCG can achieve arbitrary nonlinear transformation as well as the conventional VSCG, and the calculation precision for the CSCG was slightly lower than that for the VSCG.

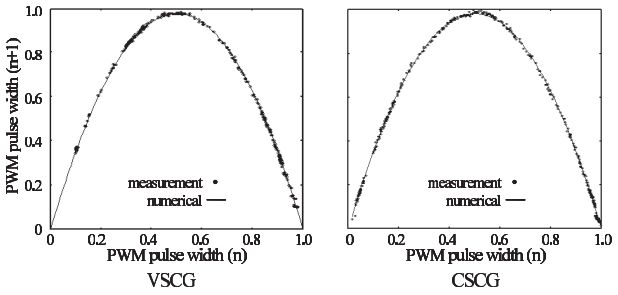


Fig. 9 Return maps of VSCG and CSCG with an operation frequency of 1 MHz.

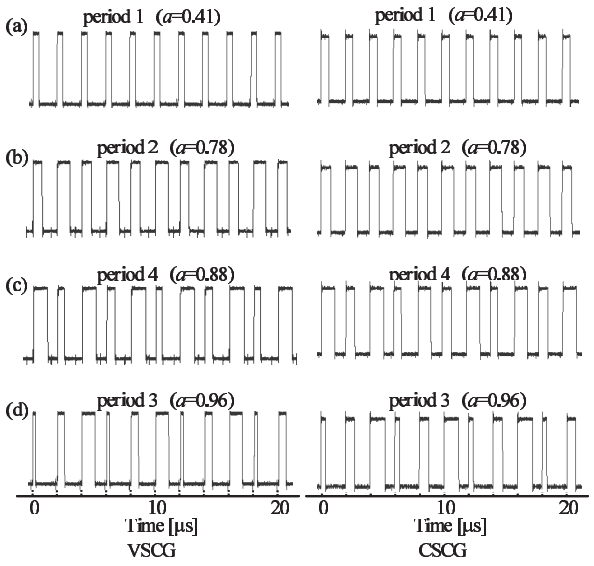


Fig. 10 Periodical solutions of VSCG and CSCG for logistic map.

The reason for such a slightly low precision is considered fluctuations of V_{non} and the PPM signal width, channel charge injection and clock feed through although they should be minimized in the circuits design. For a fluctuation of V_{non}, the VSCG is more tolerant than the CSCG, since the amplitude of V_{non} for the VSCG is larger than that for the CSCG. Amplitude of V_{non} were set at 1 and 0.6 V for the VSCG and the CSCG, respectively. V_{non} for the CSCG must be applied with the appropriate voltage to drive the MOS transistor in the saturation region.

In the measurements shown above, the update cycle of the CSCG and VSCG was set at 2 μs, thus the operation frequency of these circuits was 500 kHz. We measured the circuits with a different operation frequency. Figure 9 shows return maps with an operation frequency of 1 MHz. In these return maps, the calculation precision for the VSCG and CSCG were 6.89 and 6.55 bits, respectively. These results show that the circuit precisions drop as the operation frequency increases.

By setting the appropriate bifurcation parameter a for the logistic map, some periodical solutions can be observed. Figure 10 shows the measurement results of output signals with some values for a. We can confirm period-1, -2, -4, and -3 states for the VSCG and the CSCG. The results show that both circuits can hold some periodical states.

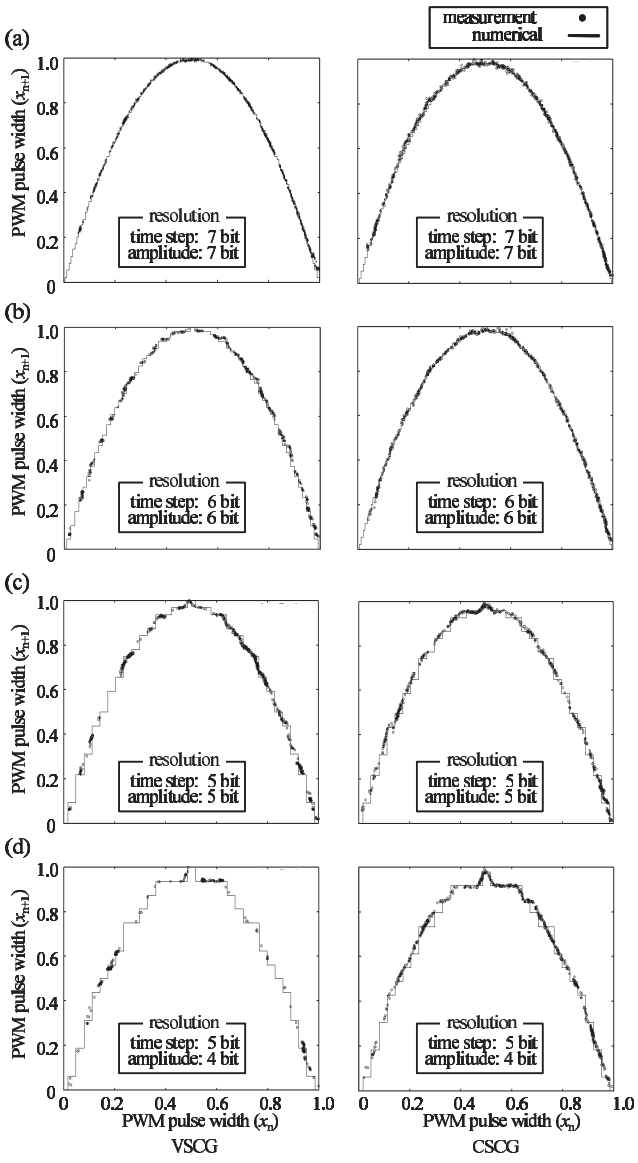


Fig. 11 Return maps with quantized nonlinear waveforms for VSCG and CSCG.

Here, let us discuss the calculation precision of our circuits regarding possible applications. When we solve the combinational optimization problem using chaotic neural network, it is known that chaotic properties near a "window" lead to a good solution search [13]. Thus, it is required that the calculation precision is high enough to enable such window generation. In Fig. 10, we can observe period-3 states. This means that our circuits have such a high precision. Therefore, it is expected that our circuits have a good performance when they are applied to chaotic neural networks.

If the nonlinear waveform V_{non} is quantized with low-bit precision, the CSCG is expected that the chaos signals are generated due to an integral effect in current sampling.

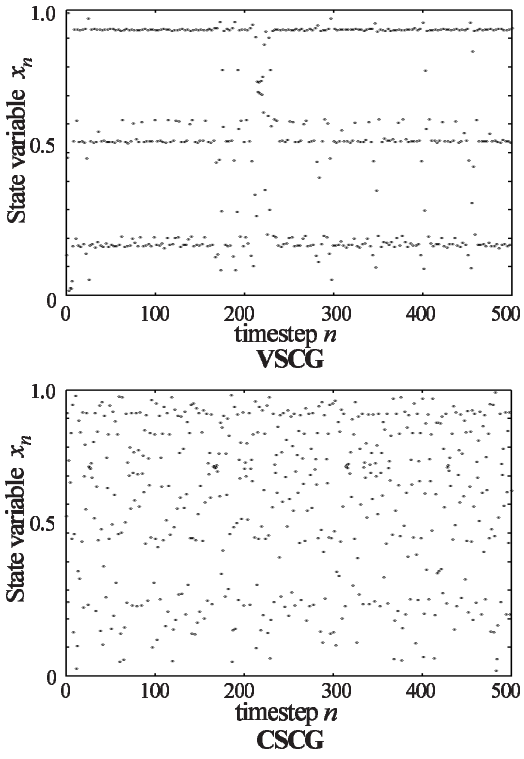


Fig. 12 Measurement results with a quantized nonlinear waveform: Time series data for Fig. 11(d).

We measured return maps with quantized parabolic waveforms for the CSCG as well as the VSCG. Figure 11 shows their return maps with quantized nonlinear waveforms. The waveforms are quantized in time and amplitude domains. The quantization characteristics are represented by a bit precision, which is defined by the ratio between the step size and the full-scale size of the time or amplitude.

When a 7 bit-quantization waveform was used, we can observe chaos in both chaos generator circuits. As a lower-bit-quantization waveform was used, the VSCG has more periodical solutions. On the other hand, the CSCG manages to hold chaotic characteristics, even below 5-bit precision waveforms are used because a current integral by sampling with a short pulse smooths the quantized nonlinear waveform.

We analyzed time-series data used for Fig. 11(d), and they are shown in Fig. 12. For the VSCG, although illegular oscillation was sometimes observed, periodic oscillation was obserbed for almost all periods. On the other hand, for the CSCG, illegular oscillation was observed. We calculated the Lyapunov exponent for the CSCG in this case by using the method proposed in [5]. We obtained a positive Lyapunov exponent $\lambda = 0.24$, and therefore we can conclude that the CSCG can generate chaos.

We compared the performance with other previous studies [3], [4]. The comparison results are shown in Table 1. The results show that only our CSCG can realize arbitrary nonlinear transformation. For the circuit area, although the fabrication technology used is different, it can be concluded that our CSCG is relatively compact and with low power consumption. For the operation frequency, our CSCG operation is slower than other circuits because the information is represented on time domain. However, there is a trade-off between operation frequency and calculation precision. Thus, we cannot correctly compare the operation frequency because calculation precision is not described for the other circuits.

Table 1 Performance comparison.

	Our CSCG	Juncu et.al	Horio et.al
Arbitrary nonlinear transformation	Possible	Impossible	Impossible
Circuit area (Technology)	$4.23\times10^3\,\mu m^2$ ($0.25\,\mu$m CMOS)	$1.22\times10^3\,\mu m^2$ ($0.60\,\mu$m CMOS)	$7.60\times10^3\,\mu m^2$ ($1.20\,\mu$m CMOS)
Power comsumption	0.274 mW	7.85 mW	No information
Operation frequency	0.5 MHz	2.5 MHz	2.0 MHz
Calculation precision	7.5 bit	No information	No information

6. Conclusion

A new chaos generator circuit with a current sampling scheme was designed and fabricated by using TSMC $0.25\,\mu$m CMOS process. The measurement results show that the conventional VSCG has slightly higher precision than the CSCG. However, when we use low-bit-quantized nonlinear waveforms, the VSCG cannot generate chaos, but is trapped in periodical solutions. On the other hand, the CSCG can generate chaos. Therefore, the CSCG is more suitable for arbitrary chaos generation using D/A conversion. By using our current-sampling scheme, large-scale nonlinear dynamical systems such as GCM and the threshold coupled map controlled with digital circuits can be constructed.

Acknowledgments

This work was partly supported by fund from MEXT, Japan, via a 21st Century COE program (center #J19) granted to Kyushu Institute of Technology. The LSI chip design was supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. Synopsys, Inc. and Mentor Graphics, Inc.

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