Dead-time Evaluation with Switching frequency for GaN-based Non-inverting Buck-Boost DC-DC Converter using FPGA-based High-frequency Control

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***Abstract*- The distinctive characteristics, such as fast switching and higher power density of gallium nitride (GaN) power semiconductor devices, are fascinating for power electronic applications. That makes it suitable for achieving high efficiency at high switching frequency operation. However, the control at higher switching frequency operation and evaluation of dead time is pivotal to achieving it. This paper presents the GaN-based non-inverting buck-boost (NIBB) dc-dc converter for high-frequency and high-efficiency operation. The feedback control was designed and implemented using FPGA for the operation of the converter at a switching frequency of 500kHz and 800kHz under different operating load conditions. Furthermore, the dead time evaluated corresponds to switching frequencies and load conditions. The PCB layout was designed to develop an experimental prototype of the NIBB converter developed using the LMG5200 GaN half-bridge chip (80V, 10A). The converter is tested for the 48V-48V operation considering the LED applications with a one-to-one voltage ratio, and a Pareto front curve is given for the 250kHz, 500kHz, 800kHz and 1MHz switching frequency.**

I. Introduction

The variety of power electronic converters, i.e. DC-DC converters, are an integral part and possess a unique role in different applications such as lighting, battery charging, power supplies, fuel cells and power adapters [1, 2]. The different topologies of DC-DC converters have been proposed and used corresponding to the requirements of the applications. The fundamental behavior of DC-DC converters is to provide buck and boost capability considering the operating range and to regulate the voltage if any perturbation occurs. The advent of new technologies and applications propelled the requirement for DC-DC converters with fast switching and higher power density. The higher passive component counts of sepic and zeta converters designed based on the conventional buck converter and boost converter can provide non-inverting output voltage and buck-boost operation, which is a disappointing factor considering the power density of the system [3 In addition, the increased power losses associated with passive power components are an additional factor. The buck and boost operating capability is one of the functionalities of the non-inverting buck-boost (NIBB) DC-DC converter with the feature of non-inverting output voltage as its name suggests, therefore, NIBB topology is an appropriate solution in various applications [4].

The wide-bandgap GaN power device has been one of the potential customers to satisfy the requirements of fast switching and higher power density with higher temperature-withstanding capability [5, 6, 7]. Power MOSFET goes through the third quadrant operation by conduction through the body diode/channel to provide the current flow from the source to the drain. Unlike the case of SiC and Si devices, GaN devices possess the inherent capability of reverse conduction without any body diode or additional anti-parallel diodes [8,9]. However, the GaN devices suffer from comparatively high reverse-conduction losses [10, 11, 12, 13]. Therefore, the operation of the switching devices with appropriate switching methodology to minimize the reverse-conduction time and the fast feedback control loop is imperative to achieve the desired response from the converter.

The forward voltage drop during reverse conduction is comparatively high for the GaN devices, and the deadtime role is prominent in the case of the GaN power converters operating at higher switching frequencies. A comparative analysis is conducted [14], [15] considering the losses for Si MOSFET and GaN-based synchronous buck converter. The impact of deadtime is analyzed for the synchronous boost converter [16] and the buck converter [17], considering the optimal selection of deadtime for operation under light and heavy load conditions. The deadtime control implemented [18] for the GaN-based synchronous boost converter to realize the dynamic selection of deadtime corresponding to the load current condition. And a dynamic deadtime controlled gate drive in [19] is employed for the GaN-based NIBB with ZVS operation having a maximum output of 20W.

The fundamental and commonly used switching methodologies are carrier-based pulse width modulation (PWM) control and direct duty PWM control [20, 21, 22]. In principle, the PWM methodology governs the output voltage regulation corresponding to changes in the duty cycle/operational mode. The phase-shifting technique is combined with the PWM methodology to reduce the ripple current across the inductor [22]. However, in the case of a GaN-based converter, this method is not very appropriate due to poor reverse conduction performance. The current mode hysteresis control implemented for Si-MOSFET NIBB using FPGA with an analogue comparator [23], [24], which requires three feedback signals: output voltage, input voltage and inductor current. The drawback of hysteresis control is the requirement of high sampling for the digital implementation and not appropriate for high switching frequency systems. The digital control is employed for the Si-MOSFET NIBB using FPGA

with an enhanced duty cycle overlap technique [25, 26].

The losses across the inductor consist of DC loss and AC loss [27]. AC losses are due to the core materials of the inductor, which are termed core losses/iron losses. The core losses are the main constituent of the total loss under light load conditions; conduction and switching losses are the major contributors to the full-load/high-load conditions [28]. A dual pole switching algorithm is proposed [28] for Si-MOSFET-based NIBB to minimize the inductor current ripple by increased/longer freewheeling time. The duty cycle is decided using a maximum efficiency tracking algorithm. However, this method is inappropriate for the GaN-based NIBB due to the higher reverse conduction losses.

The previous switching control techniques proposed in the literature and implemented for the NIBB converter are inappropriate for the GaN-based NIBB converter. A new modulation option was exploited to reduce the ripple current across the inductor using the fixed duty method [29] and validated through simulation. The modulation strategy is explored to optimize the operational modes of the NIBB converter by eliminating or minimizing the freewheeling mode operation. This paper presents direct duty PWM with fixed duty control for the high-frequency operation of a GaN-based NIBB converter. A fast feedback control loop has been developed to regulate the converter output voltage according to the different load conditions. Proportional-integral (PI) based feedback control is implemented with FPGA, and dead conditions are investigated to exploit the performance of GaN devices. The conventional digital counter-based approach was adopted for the duty cycle generation considering the fundamental clock frequency of 200MHz and switching frequency operation of 800kHz. The simulation and experimental results are used to analyze the performance of the NIBB DC-DC converter. The following are the features of this paper:

1. Constant extended duty control that reduces the current ripple in the inductor.
2. Synchronized turn-on duty signal for the buck switch and boost switch in Fig 1.
3. Single duty variable d_φ that provides lower control complexity for high frequency control.
4. Eliminating the redundant freewheeling mode and reduced inductor ripple current provides reduced reverse conduction losses.
5. Hybrid simulation environment of PLECS-MATLAB Simulink for the development of high frequency feedback control.
6. FPGA hardware-in-the-loop (HIL) simulation for initial validation of high frequency control.

II. Design and Working Principle of NIBB

A. Circuit Configuration

NIBB dc-dc converter comprises four fully controlled GaN switches in this paper. The circuit configuration of NIBB in Fig.1 consists of two half bridges corresponding to the input and output stage of the converter and capacitors at the input and output of the converter. An inductor is connected between the

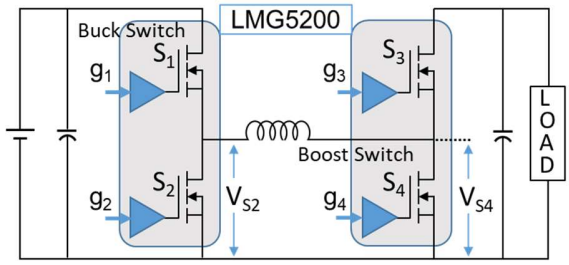


Fig. 1. Circuit configuration of NIBB dc-dc converter.

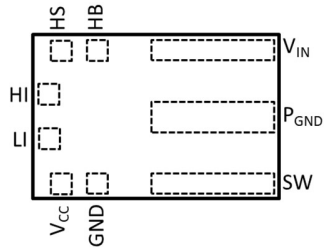


Fig. 2. Top view of LMG5200 [30].

switching node of the input leg and the output half-bridge leg. The circuit operation is defined by the relation of the input voltage (V_{in}) and output voltage (V_{out}) with the duty cycle. The duty cycle (d_1) for the high side switch (S_1) of the input half bridge governs the buck operation and is termed buck switch and similarly, the duty cycle (d_2) for the bottom switch (S_4) of the output half bridge governs the boost operation and termed boost switch as in eq. (1). The packaged half-bridge switches (LMG5200) in Fig.2, consisting of GaN switches, are used for the NIBB converter design and development. This packaged GaN-based half bridge only requires the independent high and low logic signal with deadtime for switching.

$$V_{out}=\frac{d_1}{1-d_2}V_{in};\qquad \begin{cases} d_1 > 1-d_2 & boost \\ d_1 < 1-d_2 & buck \end{cases} \tag{1}$$

The appropriate switching strategy, power circuit board design and inductor selection are required for the desired operation of the NIBB converter. In the buck-mode operation of the converter, the input buck-leg transistors are switched and conducted through the high-side transistor of the output leg. And in the boost-mode, output-boost leg transistors are switched and conducted through the top transistor of the input leg. The input and output switches S_2 and S_4 respectively provide freewheeling through reverse conduction mode operation. The switching strategy to minimize the reverse conduction operation is crucial to reduce the significant power losses in GaN. Further, the switching strategy, power circuit board, inductor power loss and inductor measurement for high switching frequency operation is discussed in this section.

B. Switching strategy

NIBB converter fundamentally can be operated in four cycles in Fig.3a corresponding to switching signals that have duty cycles d_1 and d_2 corresponding to buck and boost switch respectively. The modes described Fig. 3b, cycle I is conduction mode switch S_1 and S_4 conducting, cycle II is freewheeling

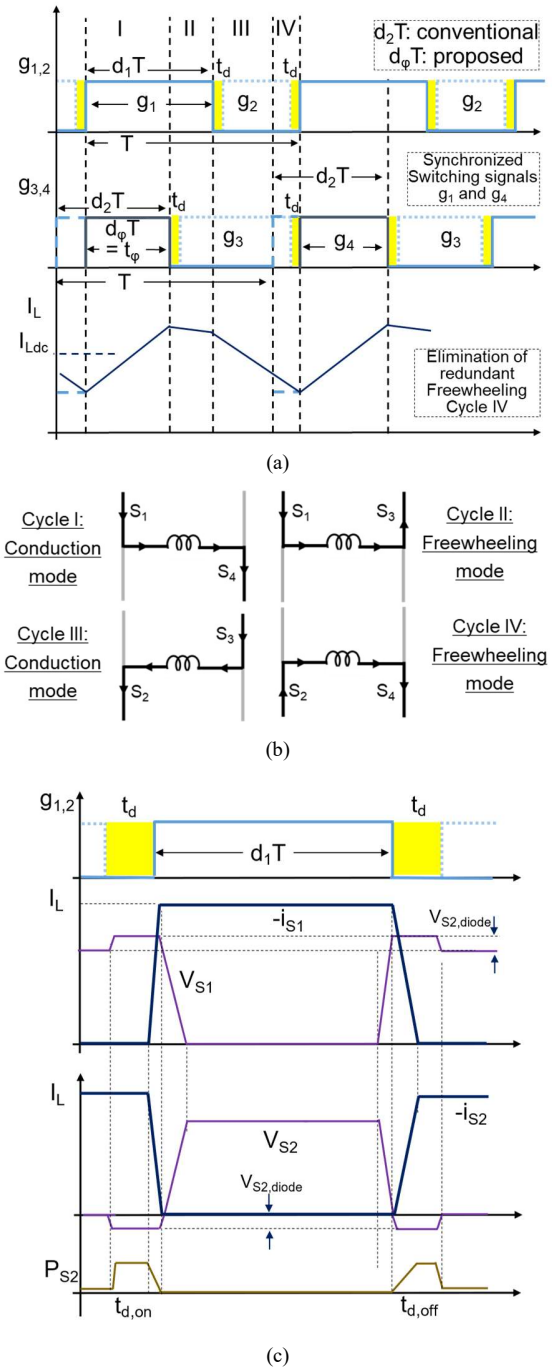


Fig. 3. NIBB operation (a) Switching signals and inductor current in boost mode, (b) Operational modes of NIBB dc-dc converter, (c) deadtime switching losses for the low side GaN device of the input half-bridge cell.

mode having S_3 in reverse conduction. Similarly, cycle III is conduction mode switch S_2 and S_3 conducting, and cycle IV is freewheeling mode switch S_2 in reverse conduction and S_4 normal conducting mode. The simulation-based study in [29] for different d_1 condition demonstrates that the inductor ripple current reduced, corresponding to an increase in d_1 under boost operation and unchanged d_2 condition. That is exploited in this paper proposing fixed extended duty control.

The fixed extended control utilizes the maximum possible duty d_1, and a constant d_1 is used for the control rather than a variable for the operation under boost mode control. Furthermore, duty d_2 synchronized with d_1 Fig.3 eliminates the redundant freewheeling mode of the NIBB operation. The constant extended duty d_1 synchronized with duty d_2 provides a lower inductor current ripple and reduced reverse conduction time of GaN devices, consequently reducing converter power losses. The single variable duty parameter d_φ is considered to reduce the complexity of the control. Corresponding to the load conditions, the change in d_φ regulates the output voltage of the converter, and this d_φ switching strategy replaces the d_2 Fig.3a.

The different conditions for deadtime (t_d) and switching frequency are investigated for the proposed switching strategy. The constant extended duty time d_1T is slightly changed according to the t_d, however, the same d_1T is used for all t_d cases. d_1T is decided considering maximum t_d case, i.e. 50ns accommodating all deadtime conditions. Constant extended d_1T is defined as eq. (2) where T is the switching period.

$$d_1T = T - 2 * t_d \tag{2}$$

C. Power loss analysis

The losses in the converter are made up of the conduction losses and the switching losses of the devices. The conduction losses depend on the duty cycle during the operation of the converter, considering the switching of the high-side switch and the low-side switch. In the proposed modulation strategy, d_1T is set to the maximum possible duty cycle, which is why the high side switch of the input leg has a higher conduction loss. The conduction losses eq. (3) for the high side and low side switch is dependent on the on-state resistance ($R_{ds,on}$) of the switch and the rms current (I_{rms}), which depends on the ripple current in the inductor (32). The switching loss is due to the overlap time of the voltage (V_s) and current (i_s) Fig.3c during the turn-on and turn-off of the switch. The switching loss mainly occurs in the high side switch as the low-side switch goes through the zero-voltage switching (ZVS) during turn-on and turn-off.

The switching loss for the high side switch eq. (4) dependent on the switching time (t_{sw}) and switching frequency (f_{sw}). GaN devices do not have the reverse recovery losses because of the majority carrier device, however, possess comparatively higher third quadrant reverse conduction losses compared to Si-MOSFET due higher conduction voltage during third quadrant operation and exhibit higher dead time losses. Turn-on and turn-off t_d and f_{sw} impacts the reverse-conduction losses during deadtime Fig.3c, and reverse conduction losses are crucial during t_d. The loss equations indicate that the conduction losses of the switch increase with the increase in inductor ripple current and load current. The switching and reverse-conduction losses increase corresponding to the switching frequency and the load current. In addition, reverse-conduction losses dominantly depend on the deadtime of the switching devices and significantly contribute to overall losses for the GaN-based converter.

$$P_{cond(HS,\ LS)} = R_{ds,on\ (HS,LS)} * I^2_{RMS(HS,LS)} \tag{3}$$

$$P_{switching(HS)}=V_s*i_s*t_{sw}*f_{sw} \quad (4)$$

$$P_{reverse}=V_{sd}*i_s*(t_{d,on}+t_{d,off})*f_{sw} \quad (5)$$

The power loss due to the inductor core losses is given as eq. (6), (7) [28] and the power loss due to the ac effect is given as eq. (8) [31]. In the case of eq. (4) and (5) t_{sw} overlap time of the voltage (V_s) and current (i_s), V_{sd} is the voltage across device for the gate off condition during deadtime; for the eq. (6) and (7) a, b, and c are the constants values of the core, B is the flux density, I_L is the inductor current, N is the number of turns, A is the cross-sectional area of the core, ΔI_L is the inductor ripple current, L is the inductance. In the case of eq. (8); K_1 is the constant, ΔI_L is the inductor ripple current, L is the inductance, f_{sw} is the switching frequency and Roper is the equivalent inductor resistance considering the skin effect and operating temperature. The core losses as well as the losses due to an ac effect in the inductor are directly proportional to the ripple current across the inductor. The reduction in ripple current across the inductor leads to the reduction of core losses as well as the losses due to an ac effect in the inductor.

$$P_{core}=a*f_{sw}^{b}*\Delta B^{c} \quad (6)$$

$$P_{core}= a * f_{sw}^{b} * \left(\frac{\Delta I_L*L}{N*A}\right)^{c} \quad (7)$$

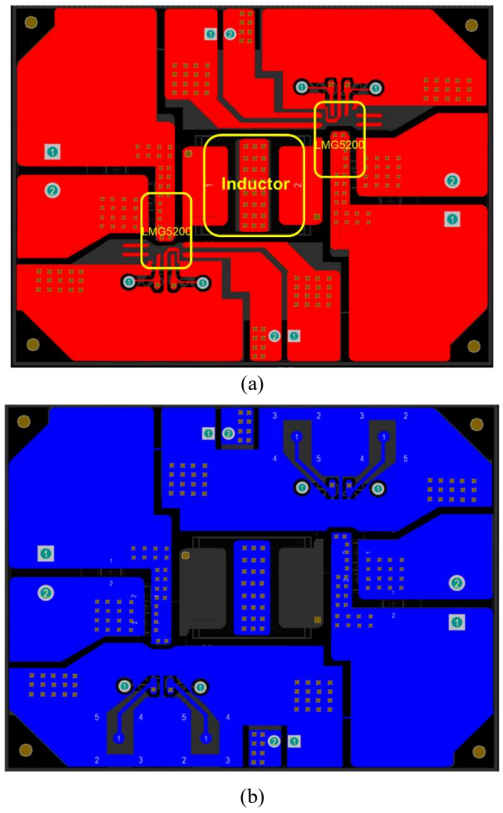
$$P_{ac}=K_1*\Delta I_L^2*\sqrt{f_{sw}}*R_{oper} \quad (8)$$

D. PCB Design

The power circuit board design is one of the crucial aspects of high frequency switching GaN devices. This circuit board design becomes different in the case of a power converter involving the appropriate placement of the surface mount power devices and passive components to minimize parasitic problems and noise. The half-bridge device in Fig.2 includes the inbuilt gate driving unit with a bootstrap connecting requirement across HS and HB. The switching of half-bridge devices requires independent logic signals HI and LI corresponding to the top and bottom switches of the half-bridge. The gate driving unit requires a DC voltage supply across V_{cc} and GND and the dc input power between V_{IN} and P_{GND} for the DC-DC converter operation.

The PCB in Fig.4 was designed for the implementation of a GaN NIBB DC-DC converter. The technical document [33] gives an insight into the design of a four-layer PCB for a conventional buck converter using the LMG5200 GaN power device half-bridge. A two-layer PCB is used to develop the NIBB converter circuit in this study following some general recommendations of technical documents. The basic requirements for the design are summarized as follows:

1. Inductors should be connected as close as possible to switching node SW to minimize the common mode capacitance Fig. 4a.
2. The copper below the SW should be removed in the bottom layer Fig.4b.
3. Ground shielding in between the logic signal to minimize the interference and noise Fig. 4a.



(a)

(b)

Fig. 4. PCB layers (a) Top layer, (b) bottom layer

4. A substantial ground shielding across the logic signal on the bottom layer Fig.4b.
5. The input and output capacitor are placed as close to V_{cc} and GND to provide better decoupling; placed on the bottom layer.
6. Pad on via to minimize the power loop inductance Fig.4.

E. Inductor Measurement

This measurement is performed to estimate the inductance and equivalent series resistance (ESR) of the inductor for the operating frequency range. A 4.7µH inductor of Vishay is selected with a DC rating of 5A and a DC saturation current rating of 9.1A. The measurement of the inductor Fig.5a demonstrates the almost constant inductance value over 500kHz to 1MHz. The DC resistance of the inductor is 26.6-28.46mΩ specified in the datasheet [34]. The resistance in the low-frequency range is almost the same as the DC resistance. The resistance increases significantly in the frequency range of 100kHz to 1MHz; this is due to the skin effect in the inductor. DC bias characteristic of the inductor [34], inductance is decreasing corresponding to an increase in current, and it is significant for the DC more than 3A. The AC resistance of the inductor Fig.5b increases after 10kHz and is dominant around the frequency range of 1MHz.

III. Feedback Control

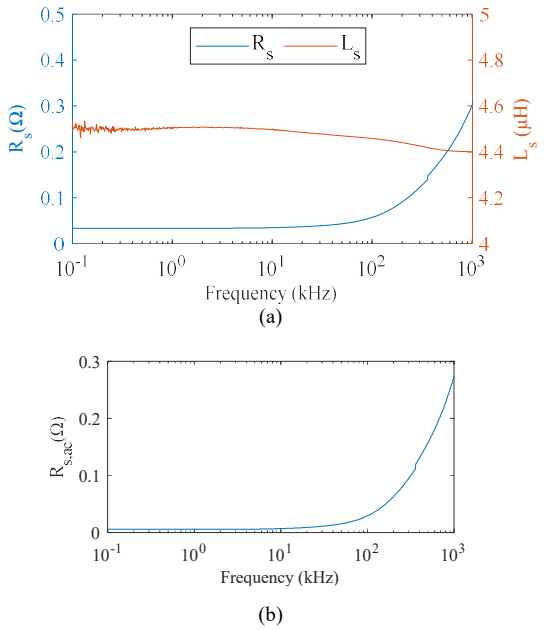


Fig 5. Measured inductor characteristic (a) ESR and inductance, (b) inductor ac resistance due to skin effect.

The high-frequency feedback control system is imperative for the closed-loop operation of the GaN-based power converter system to realize high-frequency switching in real time. This section discusses the controller development methodology and voltage only feedback control technique for the NIBB dc-dc converter.

A. Controller development

A simulation platform is essential for the development of a high-frequency feedback controller before the actual implementation for troubleshooting to avoid damaging the power board equipped with expensive high-frequency switching devices. A hybrid simulation platform is used to develop the control of the GaN-based NIBB converter [35]. The NIBB circuit model and feedback controller Fig. 6 was developed in the PLECS and FPGA emulator environment in MATLAB-Simulink. In addition, the controller is programmed with FPGA for real-time control of the GaN-NIBB power board.

The feedback control is implemented with an FPGA [36], and the output voltage is fed to the FPGA via a voltage divider and an ADC. The control system for the pure voltage feedback Fig.7 consists of a PI controller that processes the error in the output voltage. The direct duty PWM approach is used, and the output of the PI controller t_φ ($=d_\varphi T$) is equivalent to the time corresponding to duty d_φ to regulate the output voltage of the DC-DC converter. Following that manipulation in the d_φ, the subsequent duty signals are generated and applied to the converter with t_d and constant extended duty d_1.

The resistive voltage divider and ADC as delay are also modeled for the system simulation. In the first phase, the system was simulated with the PLECS and FPGA emulator

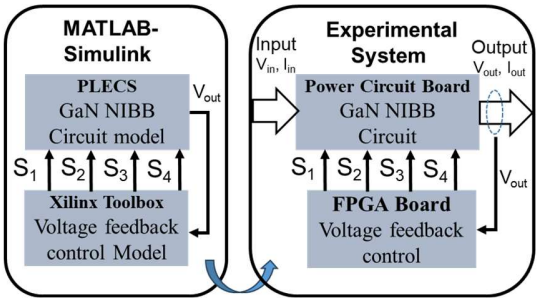


Fig 6. Block diagram of NIBB dc-dc converter system.

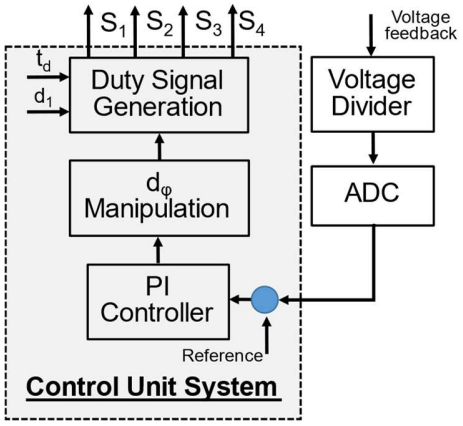


Fig 7. Block diagram of feedback control implemented using FPGA for NIBB dc-dc converter.

environment and with FPGA hardware-in-the-loop (HIL) for further authentication before the experimental validation.

B. Voltage only feedback control implementation

High-frequency feedback control has challenges considering experimental implementation in terms of PWM resolution, sampling, and throughput time of ADC to provide the appropriate system parameter regulation and feedback to the control unit. It is directly related to the system operating conditions: operating voltage/current criteria and switching frequency. In addition, system performance requirements such as output voltage/current ripple.

In this paper, the system is designed for 48-48V operation constrained by the output voltage ripple of ±5%. And the maximum switching frequency considered for the study is 800kHz. It means a PWM resolution is required to provide voltage control with a resolution of 240 mV. In addition, an ADC has a sampling of a minimum of 1.6MSPS and a resolution of more than 240mV, which is required to provide the appropriate feedback data to ensure high frequency switching control for desired system regulation.

IV. Results and Discussions

The simulation model of NIBB is developed in a hybrid simulation environment of MATLAB-Simulink consisting of PLECS and FPGA emulator for initial design and analysis of

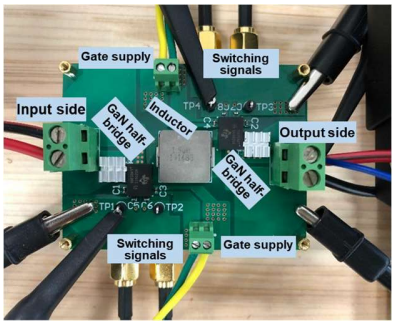


Fig 8. GaN-based NIBB dc-dc converter board.

the system considering the feedback control response in terms of variable duty cycle d_φ and voltage regulation. Further, an experimental system is developed using FPGA for real-time high-frequency voltage-only feedback control of GaN-based NIBB dc-dc converter Fig. 8 mounted on a printed circuit board.

A. Simulation results

GaN-based NIBB DC-DC converter and voltage-only feedback control are simulated in an integrated hybrid environment of MATLAB-Simulink using PLECS and Vitis model composer FPGA simulator. The system simulation is investigated for the switching frequency 500kHz and constant extended duty d_1=0.85 and t_d =50ns. The load condition is changed to analyze and understand the performance of NIBB DC-DC converter in terms of variable duty cycle time $d_\varphi T$ and voltage regulation. The $d_\varphi T$ and voltage regulation summarized in Table I for the load conditions of 48 Ω, 24 Ω, 16 Ω, 12Ω.

The output voltage is appropriately regulated, corresponding to a change in the load condition following the effect of d_φ manipulation. The $d_\varphi T$ is increasing, corresponding to an increase in load condition to compensate the power losses occurring in the power circuit and regulate the output voltage. The software-based simulation and FPGA HIL simulation both demonstrate the effective working of voltage-only feedback control, however, there is a significant difference in both the simulation results for $d_\varphi T$ under low operating load condition and $d_\varphi T$ difference becoming smaller for the higher load conditions.

B. Experimental Results

The performance of the NIBB converter is evaluated experimentally with an IT8512C electronic load, which can be used as an LED load condition in CR-LED mode. The performance is investigated under different load conditions in CR-LED mode. The proposed switching strategy is confirmed for the NIBB converter operation. The switching logic signals g_1 and g_4 for the S_1 and S_4 switches Fig. 9a demonstrate the synchronization of the switching signals during on-time that is essential to eliminate the redundant freewheeling operation mode Fig.3a and Fig.3b in cycle IV for the conventional method of NIBB operation. The switching node voltages are measured corresponding to the bottom switches S_2 and S_4 of the input and output half-bridges. The switch node voltages in Fig. 9b demonstrate the voltage across the S_2 and S_4 corresponding to

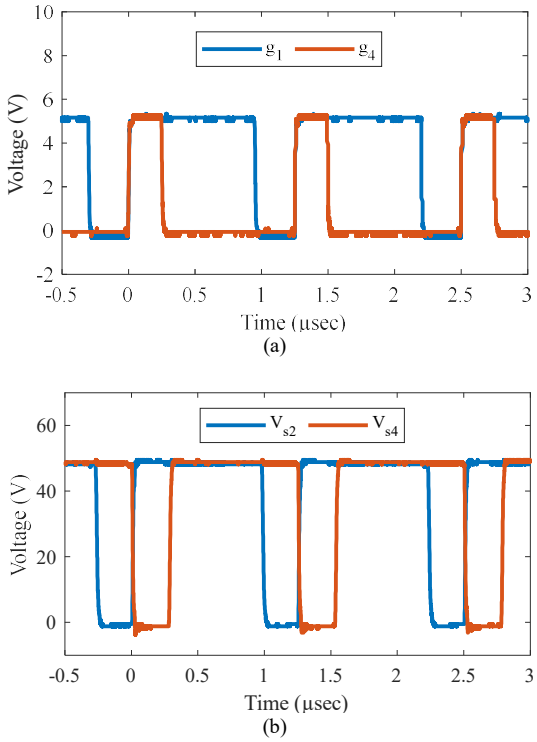


Fig.9 Experimental waveform (a) Gate signal waveform for switches S_1 and S_4 for 800kHz switching frequency, load 48Ω and the deadtime 20ns, (b) voltage measurement at the switching nodes across S_2 and S_4 for 800kHz switching frequency, load 48Ω and the deadtime 20ns.

switching signals S_1 and S_4 in Fig.9a.

The switching logic signal g_1 represents constant extended mode duty d_1 for switch S_1. When switch S_1 is turned on then S_2 is turned off, and the input DC voltage appears across S_2. Further, the switching logic signal g_4 represents the variable duty d_φ for switch S_4, therefore, when S_4 is off, the dc voltage appears across the switch S_4 authenticated by Fig. 9a and 9b.

The on-time interval of S_1 is fixed, and on-time interval ($d_\varphi T$) for S_4 is the main control parameter to regulate the output voltage corresponding to change in the load conditions. The increased load draws the higher current and the output voltage dips. Therefore, the on-time interval $d_\varphi T$ is changed correspondingly to boost the output voltage for desired regulation. The gate signal waveforms in Fig.9a and 9b are demonstrated under the load condition of 48Ω and t_d=20ns.

GaN-NIBB converter system performance is examined for

TABLE I
NIBB FEEDBACK CONTROL RESPONSE (500kHz, 50ns)

LED Load [Ω]	V_{in} [V]	Software simulation		FPGA HIL Simulation	
		V_{out} [W]	d_φ*T [ns]	V_{out} [W]	d_φ*T [ns]
48	48	48.2	490	47.9	435
24	48	48.2	500	48	460
16	48	48.1	530	48.1	500
12	48	48.1	540	48	510

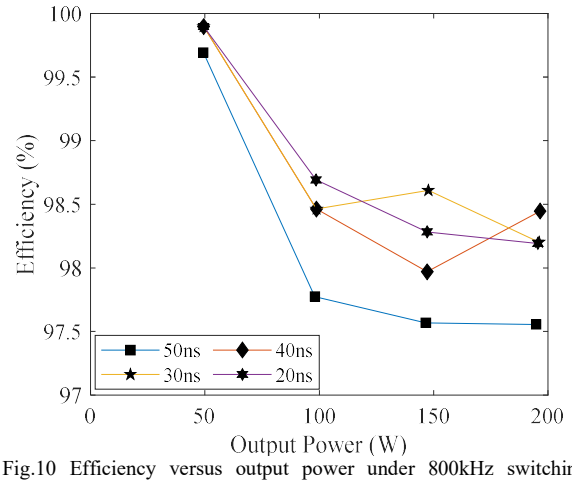


Fig.10 Efficiency versus output power under 800kHz switching frequency operation.

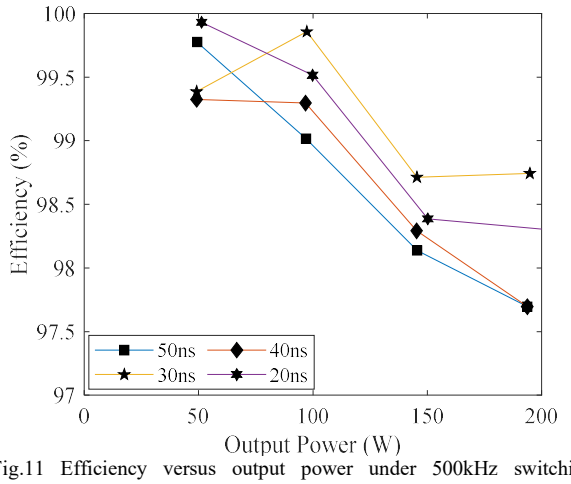


Fig.11 Efficiency versus output power under 500kHz switching frequency operation.

the voltage-only feedback control considering the operating switching frequency of 800kHz and 500kHz; deadtime t_d conditions of 20ns, 30ns, 40ns and 50ns; and the operation under load conditions of 48 Ω, 24 Ω, 16 Ω, 12Ω like the simulation. The deadtime condition of 20ns to 50ns is selected considering the deadtime recommendation of EPC GaN FETs for the optimum deadtime selection [37]. The converter efficiency is demonstrated in Fig. 10 for the 800kHz and 50ns to 20ns deadtime under different operating load conditions.

The converter achieves the highest efficiency for the operating switching frequency of 800kHz under low load conditions Fig.10 for all dead time cases from 50ns to 20ns below, and when the load current increases, the converter efficiency starts to decrease. There is a decreasing trend of efficiency, corresponding to changes in load conditions from 48 Ω, 24 Ω, 16 Ω and 12Ω for 50ns and 20ns conditions for operating switching frequencies of 800kHz. There is a similar trend for 40ns and 30ns dead time, however, there is an increase in efficiency at 12Ω and16 Ω for the 40ns and 30ns dead-time.

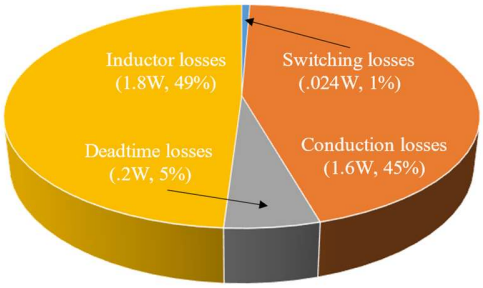
The efficiency of the NIBB DC-DC converter is investigated, for a switching frequency of 500kHz Fig.11. There is a similar declining trend in efficiency with increasing load conditions for the operation under 50ns, 40ns and 20ns dead time conditions. And the efficiency increases at 24 Ω and 12Ω for the 30ns deadtime. The performance phenomenon of GaN devices is mentioned in [37], corresponding to the load conditions and dead time efficiency changes. Therefore, adaptive dead time corresponding to the load conditions can be a choice to achieve the best possible efficiency for GaN devices and GaN-based converter systems.

Under low load conditions, the conduction losses are low, which can lead to higher efficiency under load conditions at both 500kHz and 800kHz switching frequencies. Efficiency tends to decrease as conduction losses increase with increasing load conditions. There may be factors such as dominant conduction losses in the devices, more contribution from reverse conduction losses and inductor losses as the load increases. GaN devices have very low switching losses that are common under almost all operating conditions. The reverse conduction and inductor losses at higher load conditions can be important dominating factors. Inductor losses can rise significantly due to higher ripple current, ESR and skin effects with higher load conditions.

It is worth noting that the efficiency is better at the lower dead time condition for switching frequencies of 800kHz and 500kHz under all load conditions. It is predominantly because of lower reverse conduction losses in the GaN devices for shorter dead time cases. There is a significant drop in the efficiency for the converter operation under higher deadtime conditions for 800kHz as well as 500kHz, especially for the higher load conditions. This decrease in efficiency is possibly due to the predominant reverse conduction losses that can be

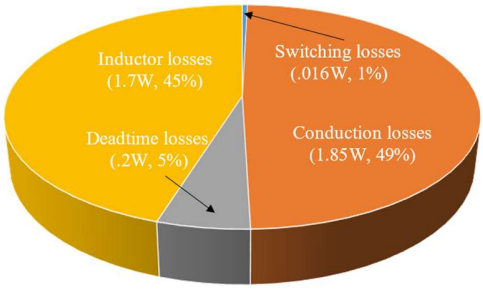
TABLE II
NIBB FEEDBACK CONTROL PERFORMANCE UNDER DIFFERENT LOAD CONDITIONS

Input Voltage V_{in} [V]	**Switching frequency(f_{sw}): 800kHz, deadtime (t_d)=20ns**							**Switching frequency(f_{sw}): 500kHz, deadtime (t_d)=20ns**						
	V_{out} [V]	**I_{out} [A]**	**d_φ*T**		**P_{in} [W]**	**P_{out} [W]**	**Efficiency [%]**	**V_{out} [V]**	**I_{out} [A]**	**d_φ*T**		**P_{in} [W]**	**P_{out} [W]**	**Efficiency [%]**
			[ns]	**% of T**						**[ns]**	**% of T**			
48	48.9	1.01	300	24.8	49.44	49.39	99.90	48.85	1.05	450	22.9	51.36	51.29	99.87
48	48.9	2.015	340	28.1	99.84	98.53	98.69	48.85	2.04	475	24.23	100.32	99.65	99.34
48	48.9	3.01	350	28.9	149.76	147.19	98.28	48.95	3.06	520	26.5	152.64	149.79	98.13
48	48.9	4	355	29.33	199.20	195.60	98.19	48.9	4.07	530	27	202.56	199.02	98.25



Estimated losses: 3.674W, Experimental: 3.6

(a)



Estimated losses: 3.77W, Experimental: 3.54

(b)

Fig.13 Distribution of estimated losses for 20ns deadtime and 4A load current (a) 800kHz switching frequency, (b) 500kHz switching frequency.

more dominant in the higher load conditions with higher current flowing in the reverse conduction mode. According to equation (7), the reduced dead time during the switch-on and switch-off process leads to a reduction in the reverse conduction losses and thus an improvement in the converter efficiency. The reverse conduction losses also depend on the switching frequency. However, a lower switching frequency leads to a longer conduction time which affects the conduction losses.

Furthermore, the converter performance data is summarized in Table II for in depth analysis under the operating condition of t_d=20ns and switching frequency of 800kHz and 500kHz considering the output voltage regulation and control duty parameter $d_\varphi T$ that is responsible for the regulation of output voltage corresponding to change in the load condition. The converter operates around 200W for the maximum load condition. The losses are estimated in Fig.13 using the mathematical equation discussed in section II for the comparison with the losses in the experiments. Duty cycle d_φ increases as expected corresponding to change in the load condition that ultimately increases the on-time of the boost switch to provide the regulation of output voltage. The output voltage is regulated appropriately following the change in $d_\varphi T$. The regulated output voltage is slightly higher than the 48V due to offset in feedback system, however, the value is well regulated corresponding to different load conditions considering the ripple criteria of 5% for the output voltage.

The controller performance was investigated for the NIBB DC/DC converter by introducing a step change in load condition. The IT8512C electronic load is used in constant current mode for the transient response of the load, as the CR-LED mode does not have the appropriate function for the load

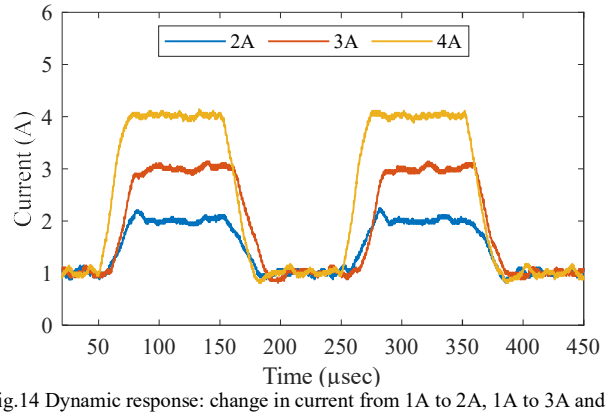


Fig.14 Dynamic response: change in current from 1A to 2A, 1A to 3A and 1A to 4A

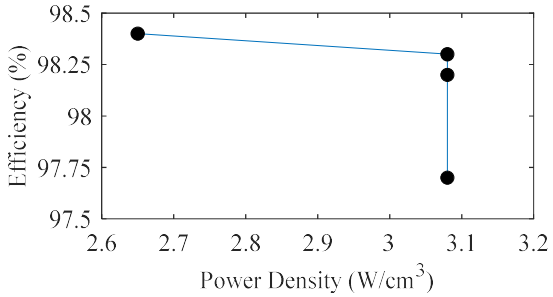


Fig 15. Pareto front curve for the NIBB dc-dc converter.

step. Three different step conditions are explored for the load change to evaluate the dynamic performance of the controller. The load steps from 1A to 2A and 2A to 1A, 1A to 3A and 3A to 1A, 1A to 4A and 4A to 1A Fig.14 shows the stable operation of the converter for all conditions. However, the response behavior is somewhat slower in the case of the low load transients Fig.14a. The load transient condition confirms the voltage regulation and stable output voltage of the converter.

Fig.15 shows the Pareto front curve for the NIBB dc-dc converter considering the switching conditions of 250kHz, 500kHz, 800kHz and 1MHz. The power density calculation considers the identical inductor properties of Vishay IHLP automotive inductors' high-temperature series with similar saturation currents for all the switching conditions. Power density constitutes the inductor, GaN LMG5200 chip, heat sink and input-output capacitors.

V. Conclusions

A two-layer PCB design with voltage-only feedback control is presented for the FPGA-based high switching frequency converter control for the 48-48V operation of a GaN-based NIBB DC-DC converter considering the LED application. A hybrid simulation environment is used for the development of high frequency feedback control. The converter performance was demonstrated under different operating load conditions for the proposed switching strategy with constant extended duty control and synchronized switching signals to eliminate the redundant freewheeling mode. The converter performance

confirms the effect of dead time and significantly affects efficiency. The deadtime is more pronounced at a higher switching frequency of 800kHz considered in the paper. Furthermore, the dead time effect varies with load conditions, and it is more pronounced in the case of higher load conditions as the reverse conduction losses increase with the flow of higher current in the devices. The proposed switching strategy with voltage-only feedback can regulate the output voltage corresponding to a change in the load condition.

The dynamic is demonstrated for the proposed control strategy considering a step change in the load current for a maximum load condition of 4A, and satisfactory controller performance is confirmed. A Pareto front curve exhibits the efficiency corresponding to power density. The switching frequency of 800kHz can lead to better power density, and a decrease in efficiency corresponding to specific load conditions is observed compared to 500kHz for the dead time conditions. The converter configuration and parameters can be evaluated based on the application requirements.

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