Unbalanced Half-bridge Split Capacitor Power Decoupling with Multi-Order Frequency Control for 800V On-board Battery Charger

Tuyen D. Nguyen, *Senior Member, IEEE*, Long H. B. Nguyen, *Student Member, IEEE*, Dong Tran, *Student Member, IEEE*, Ravi Nath Tripathi, *Senior Member, IEEE*, Hai N. Tran, *Member, IEEE*

***Abstract*- This paper proposes a new method for the design and control of a Half-bridge Split Capacitor based Power Decoupling (HSC-PD) circuit to eliminate the bulky Electrolytic Capacitors (E-cap) at dc-link, targeting 800V OBC applications with higher reliability and power density. In the proposed method, both capacitance and dc-offset voltage of the decoupling capacitors are designed unbalanced with the bottom capacitor having a dominant effect over the top one, which reduces the decoupling capacitance requirements compared to the previous works. In addition, the effect of lower dc-link capacitance in reducing power rating of the pre-charge resistor, typically used in OBC applications, is presented. This effect, overlooked in previous literature, leads to reducing volume and cost of the OBC. A small signal model of the HSC-PD is introduced, and a modified feedback control strategy is proposed, offering lower memory usage and calculation effort for the DSP microcontroller when compared with conventional Proportional Resonant (PR) controllers. Comparisons of the proposed method with other HSC-PD counterparts as well as with the conventional E-cap method are given. Finally, a 7.4kW prototype of an 820V interleaved totem-pole PFC with HSC-PD is built and tested to verify the superior performance of the proposed method.**

Index Terms – OBC; power decoupling; electrolytic capacitor; 800V electric vehicles, half-bridge split capacitor.

I. Introduction

Battery Electric Vehicles (BEVs) has been growing rapidly in recent years, and expected to replace the Internal Combustion Engine Vehicles (ICEVs) in the future to reduce CO_2 emission through transportation [1] – [4]. On-board Battery Charger (OBC) is one of the pivotal component of the BEVs, and it's main function is to charge the traction battery at home or office using the available ac grid [5] – [6].

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Tuyen D. Nguyen, Dong Tran are with Ho Chi Minh City University of Technology (HCMUT), VNU-HCM, Ho Chi Minh City, Vietnam. (e-mail: *ndtuyen@hcmut.edu.vn*, *1652154@hcmut.edu.vn*).

Ravi Nath Tripathi is with Kyushu Institute of Technology, 808-0196 Kitakyushu, Fukuoka, Japan. (e-mail: *tripathi.ravi-nath639@mail.kyutech.jp*).

Hai N. Tran, Long H. B. Nguyen are with xEVtech Co. Ltd., Ba Ria city, Ba Ria - Vung Tau, Vietnam. (e-mail: haitran@xevtech.vn; *longnguyen@xevtech.vn*).

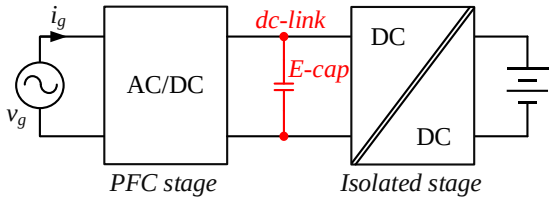


Fig. 1. Conventional OBC with E-cap.

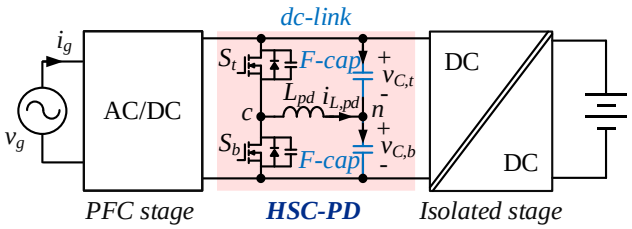


Fig. 2. Proposed E-capless 800V OBC based on *HSC-PD* circuit.

The conventional single-phase OBC shown in Fig. 1 have been widely used in 400V BEVs, in which a large numbers of parallel Electrolytic capacitors are placed between a PFC and an isolated stages to absorb the double-line frequency ripple [7] – [10]. However, these E-caps are short life-time, low current rating, and low power density making it not suitable for the next generation OBC where the requirement of reliability and power density of EV power converters are increased aggressively along with the increasing of charger power rating [5], [11], [12]. In addition, the EV's battery voltage are tend to increase to 800V from current 400V system, leading to many series and parrallel connections of E-cap are required to increase the dc-link votlage in the conventional OBC design method due to low avaiability of high-voltage rating E-cap. This worsens the reliability and power density of the converter. It worth to mention that the use of 800V battery allows to develop a dc fast-charger with higher power rating up to 350kW compared to a typical 50kW-to-100kW fast charger currently available for the 400V system, which significantly reduce charging time. Moreover, various benefits of 800V system over the 400V system such as lighter vehical weight, wider speed range, and higher efficiency have been mentioned in previous literatures [13].

A well-known method to eliminate the E-cap is by integrating an auxiliary Power Decoupling (PD) circuit into the

main power converter. The PD circuit makes the instantaneous power between ac-grid and dc battery sides balanced. Hence, the capacitance requirement for the dc-link is significantly reduced so that the E-cap can be replaced by film or ceramic capacitors [14] - [25]. The auxiliary storage elements of the PD circuit can be inductor, capacitor, or both. However, capacitor is preferable for PD purposes due to lower loss and higher energy density compared to that of the inductor. This paper proposes a new structure for 800V OBC based on PD circuit, as shown in Fig. 2. A new design approach and new control method for the PD circuit are proposed to reduce the required capacitance and improve its performance, power density and efficiency. In addition, the precharge resistor of the OBC is significantly reduced as a result of dc-link capacitance reduction. Furthermore, a modified feedback control based on co-ordinate transformation *αβ/dq* is proposed to reduce the digital control complexity.

The PD circuits in the literatures is classified in to two methods, AC PD and DC PD. In AC PD method [19] – [21], the voltage across decoupling capacitors is equal to ac-grid voltage. Therefore, high capacitance is required due to zero dc-offset voltage. This high capacitance issue of AC PD method is worsen in OBC applications which usually requires the converter to operate with universal grid voltage, typically ranging from $85V_{ac,rms}$ to $265V_{ac,rms}$, thus, higher capacitance is required considering at the lower grid voltage situation. In DC PD methods [14] – [18], the voltage across decoupling capacitor consists of both ac and dc components with the maximum value up to dc-link voltage which is always higher than grid voltage in the boost PFC converter. Therefore, the required decoupling capacitance in the DC PD method is lower than that of the AC PD method due to high dc-offset component, especially in 800V OBC. It's worth noting that even though the voltage rating of decoupling capacitors in AC PD is lower than DC PD due to zero dc-offset, there is not big different in the actual voltage rating of decoupling capacitors between two motheds because the dc-volage rating of film capacitors is usually much higher than its ac-voltage rating [26], [27]. Among various DC PD circuit topologies were presented in the previous works [14] – [18], Half-bridge Split Capacitor based PD (HSC-PD) is frequently used because the dc-link capacitors are directly utilized for power decoupling purpose, thus, no addition capactior is needed [15] – [18].

Several control methods have been developed for the HSC-PD converter [15] – [18]. In [16], the HSC-PD structure was first introduced with the open-loop control method. However, open-loop control is sensitive to system uncertainties, such as parameter tolerances and disturbance, leading to not accuracy. After that, a closed-loop control algorithm for the HSC-PD circuit is proposed in [18], which is much more robust under various uncertainty and steep load change conditions. In both [16] and [18], decoupling capacitors are designed in such a way that their capacitance value and dc voltage component are equal, and their ac voltage component fluctuates at a line frequency. However, this strategies have several drawbacks: 1) large capacitance value of both decouling capacitor, which increases not only capacitor volume but the current rating of the PD circuit; 2) difficult to select the decoupling capacitor since its ac voltage rating is high; 3) low efficiecny because of high current rating and equivalent step-down ratio; 4) low dynamic response since controlling the ac components at line-frequency requires a 90^o-shifting function in the controller.

In [17], a unequal dc voltage component method is introduced in a complete closed-loop control system. This reduces the amplitude of ac voltage component. Moreover, the ac component is controlled at the double-line frequency to avoid the delay in the controller and make it insensitive with the capacitance tolerance. Even though the robustness of this control method has been practically demonstrated under large capacitance tolerance conditions, it is designed based on an equal capacitance approach, resulting in large equivalent capacitance and high current rating. In addition, the effect of unequal dc voltage component on converter efficiency, and the fourth-line frequency harmonic caused by double-line frequency voltage and current in the decoupling circuit have not been discussed.

In [15], unequal capacitance approach was first introduced to improve the robustness of the controller under non-ideal grid, and the ac voltage ripple is obtained with multi-harmonic frequency by using conventional PR controller. However, the ac voltage rating of capacitors is high due to equal dc voltage component, making it not suitable for high dc-link voltage converter such as 800V OBC since the high ac voltage rating capacitor is usually bulky and low avaiability. In addition, the capacitance values in [15] are pretty high of 330μF and 120μF for the top and bottom capacitors, respectively, at 400V dc-link and 1.5kW.

Considering the aforementioned issues, this paper proposes a new design approach and control method for the HSC-PD circuit, in which both dc component and capacitance values of the decoupling capacitors are designed unequally with bottom-bias capacitor approach, reducing not only equivalent capacitance and ac voltage ripple but current rating of the PD circuit. The effect of fourth-line frequency harmonics, which is caused by double-line frequency of voltage and current in the PD circuit, is also analyzed. The dc-offset ratio and its impact on the converter efficiency will be discussed. Furthermore, the feedback control of HSC-PD is developed for the entire system considering the proposed unequal dc component and capacitance. The multi-order frequency harmonic component compensated through the PR controller, however, the implementation in digital domain consdiering *αβ* frame requires considerable amount of delay-time for computation as well as frequency response is poor as compared to the integral control action. In this paper, implementation of PR controller is proposed using *αβ-dq* transformation with an integrator that enables the generation of multi-order frequency component, reduction in DSP memory utilization and calculation effort. Theoretical analysis and experimental results are given to verify the superiority of the proposed method.

II. Proposed Even-order Frequency Unbalanced Half-bridge Split Capacitor Power Decoupling Control

A. Theoretical analysis and design guideline

Circuit diagram of the proposed 800V OBC is shown in Fig. 2, in which bulky E-cap is replaced by HSC-PD circuit using low capacitance Film capacitor (F-cap). The charger is rated at 7.4kW, and the dc-link voltage is fixed at 820V. Compared to the variable dc-link strategy as presented in [7], the use of fixed dc-link voltage at maximum provides the benefits of: 1) minimize the required decoupling capacitance; 2) minimize the current conducted in the primary side of the isolated stage of the OBC reducing current rating and conduction loss. It is worth mention that the cost of 1200V SiC MOSFET, that is used in the primary side of the isolated stage, increases significantly with its current rating. The grid current and voltage as well as its instantaneous power can be expressed as below:

$$\begin{cases} v_g(t) = \sqrt{2}\cdot V_g \cdot \sin(\omega\cdot t + \varphi) \\ i_g(t) = \sqrt{2}\cdot I_g \cdot \sin(\omega\cdot t + \varphi) \end{cases} \quad (1)$$

$$p_g(t) = v_g(t)\cdot i_g(t) = V_g \cdot I_g - V_g \cdot I_g.\cos(2\cdot\omega\cdot t + 2\cdot\varphi) \quad (2)$$

The phase of grid voltage and current φ will be assumed to be zero to reduce the complexity in the later analysis since power factor correction is used. The first term on the right side of (2) represents the average power charged the battery, P_{dc}, while second term is the second-order power that needs to keep away from the battery. In the conventional OBC, this second-order power is stored in the dc-link using bulky electrolytic capacitors leading to low power density and reliability. In this paper, the second-order power is stored in two small film capacitors C_t and C_b by using the proposed design and control method for the HSC-PD, which is described as follows.

The voltage equation for each decoupling capacitors, $v_{C,t}(t)$ and $v_{C,b}(t)$, are proposed as:

$$\begin{cases} v_{C,t}(t) = V_{dc,t} + \sum\limits_{n=2,4,6,\ldots} V_{ac(n)} \cdot \sin(n\cdot\omega\cdot t + \theta_n) \\ v_{C,b}(t) = V_{dc,b} - \sum\limits_{n=2,4,6,\ldots} V_{ac(n)} \cdot \sin(n\cdot\omega\cdot t + \theta_n) \end{cases} \quad (3)$$

The first and second terms on the right side of (3) represent dc and ac voltage components of each decoupling capacitor respectively. The ac voltage components include multiple of even-order frequencies $V_{ac(n)}$ (n = 2, 4, 6, …), and are 180° phase shift between two capacitors to ensure the sum of which are constant at the desired dc-link voltage. The block diagram of the proposed controller is detailed in Section III. Ideally, only second-order ac voltage component is needed for storing the second-order power of the grid in (2). However, fourth-order power is created because of second-order voltage and current conducted through the decoupling capacitors. Similarly, higher even-order powers of 6th, 8th, … are created from its previous even orders. Therefore, the decoupling capacitor voltages must be operated with multi even-order frequencies to suppress the second-order power of the grid and other higher even-order powers created by itself, as shown in (3).

The dc voltage components of two capacitors, $V_{dc,t}$ and $V_{dc,b}$, are unequal with the proposed dc-offset factor m as below:

$$\begin{cases} V_{dc,t} = V_{Link}\cdot\left(\frac{1}{2} - m\right) \\ V_{dc,b} = V_{Link}\cdot\left(\frac{1}{2} + m\right) \end{cases} \quad with\ 0 < m < 0.5 \quad (4)$$

It can be seen from (4) that in the proposed method dc voltage component of the bottom capacitor $V_{dc,b}$ is always kept greater than that of top capacitor, $V_{dc,b} > V_{dc,t}$, since m is the dc-offset ratio, and can be chosen within $0 < m < 0.5$. This proposed approach is different from the previous work presented in [15] that was designed with higher dc voltage component of the top capacitor. The reason for this proposed approach is that if considering the HSP-PD circuit as a buck converter with input and output voltages are V_{Link} and $V_{dc,b}$, respectively, higher $V_{dc,b}$ leads to lower step down ratio of buck converter and narrower duty cycle range. In addition, higher bottom capacitor voltage led to lower decoupling inductor current for the same power rating. Therefore, the proposed unbalancing approach with higher dc voltage component of the bottom capacitor achieves higher efficiency and smaller decoupling inductor as compared to the previous work [15], [17]. It is noticeable that the peak ac voltage component must be smaller than the dc voltage component of the top capacitor to avoid over modulation.

Current conducted through two decoupling capacitors are determined from (3) as below:

$$\begin{cases} i_{C,t}(t) = C_t \cdot \dfrac{dv_{C,t}(t)}{dt} \\ \qquad = C_t \cdot \sum\limits_{n=2,4,6,\ldots} n\cdot\omega\cdot V_{ac(n)} \cdot \cos(n\cdot\omega\cdot t + \theta_n) \\ i_{C,b}(t) = C_b \cdot \dfrac{dv_{C,b}(t)}{dt} \\ \qquad = -C_b \cdot \sum\limits_{n=2,4,6,\ldots} n\cdot\omega\cdot V_{ac(n)} \cdot \cos(n\cdot\omega\cdot t + \theta_n) \end{cases} \quad (5)$$

where C_t and C_b are capacitance values of top and bottom capacitors, respectively. Current conducted through decoupling inductor can be obtained from (5) by:

$$\begin{aligned} i_{L,pd}(t) &= i_{C,b}(t) - i_{C,t}(t) \\ &= -(l+1)\cdot C_t \cdot \sum_{n=2,4,6,\ldots} n\cdot\omega\cdot V_{ac(n)} \cdot \cos(n\cdot\omega\cdot t + \theta_n) \end{aligned} \quad (6)$$

Typical waveforms of the proposed control method are shown in Fig. 3.

Not only dc voltage component but also capacitances of two decoupling capacitors are designed unequally in the proposed method. Assuming that l is capacitance ratio between two decoupling capacitors:

$$l = \frac{C_b}{C_t} \quad (7)$$

The instantaneous power stored in two capacitors is therefore obtained from (3) - (6) by:

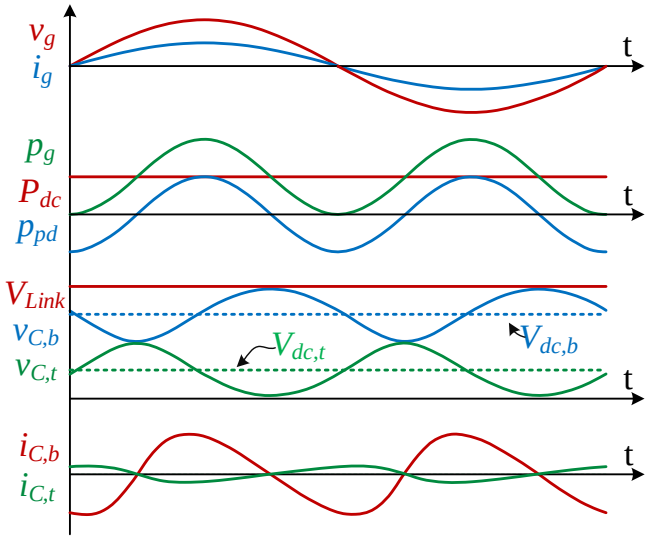


Fig. 3. Typical waveforms of the proposed power decoupling method at full load

$$\begin{aligned} p_{pd}(t) &= p_{C,t}(t) + p_{C,b}(t) \\ &= v_{C,t}(t)\cdot i_{C,t}(t) + v_{C,b}(t)\cdot i_{C,b}(t) \\ &= -\omega\cdot\left(V_{dc,b}\cdot C_b - V_{dc,t}\cdot C_t\right)\cdot \sum_{n=2,4,6,\ldots} n\cdot V_{ac(n)}\cdot\cos(n\cdot\omega\cdot t+\theta_n) \\ &+(l+1)\cdot C_t\cdot \sum_{n=2,4,6,\ldots}\left(V_{ac(n)}\cdot\sin(n\cdot\omega\cdot t+\theta_n)\right)\ldots \\ &\ldots\cdot \sum_{n=2,4,6,\ldots}\left(n\cdot\omega\cdot V_{ac(n)}\cdot\cos(n\cdot\omega\cdot t+\theta_n)\right) \end{aligned} \tag{8}$$

The phase angle θ_n can be determined by:

$$\theta_n = -(n-2)\cdot\frac{\pi}{4} \tag{9}$$

The peak value of each ac voltage components in (8) are determined by:

$$\begin{cases} V_{ac(2)} = \dfrac{V_g\cdot I_g}{\omega\cdot\left[l-1+2\cdot m\cdot(l+1)\right]\cdot C_t\cdot V_{Link}} \\ V_{ac(4)} = \dfrac{(l+1)\cdot V_{ac(2)}^2}{2\cdot\left[l-1+2\cdot m\cdot(l+1)\right]\cdot V_{Link}} \\ V_{ac(6)} = \dfrac{(l+1)\cdot V_{ac(2)}\cdot V_{ac(4)}}{\left[l-1+2\cdot m\cdot(l+1)\right]\cdot V_{Link}} \\ V_{ac(8)} = \dfrac{(l+1)\cdot\left(2\cdot V_{ac(4)}\cdot V_{ac(4)}+4\cdot V_{ac(2)}\cdot V_{ac(6)}\right)}{4\cdot\left[l-1+2\cdot m\cdot(l+1)\right]\cdot V_{Link}} \end{cases} \tag{10}$$

The first term on the right side of (8) represents for the second-order power that is stored in the decoupling capacitors and the rest terms in the right side of (8) are the power naturally generated by the controller itself and is controlled to store within the decoupling circuit. The second order and self-created power components (4^{th}, 6^{th}, 8^{th}, …) with different value of m are shown in Fig. 4. Practically, the waveforms of voltage (current) of decoupling capacitor (inductor) is generated by a controller in the closed loop system, thus to reduce the control complexity

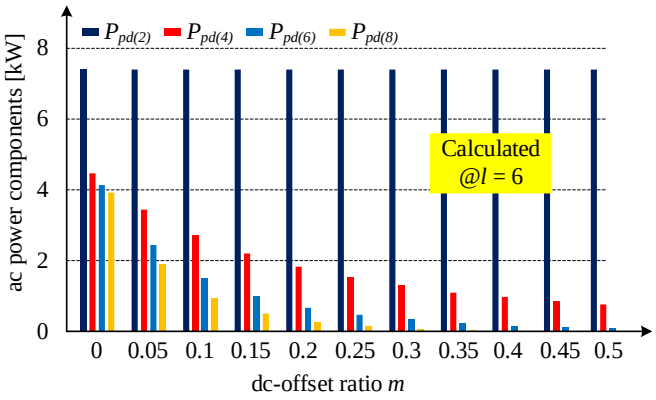


Fig. 4. AC power components of the decoupling circuit calculated at l = 6, C_t = 16 μF, and C_b = 86 μF.

caused by the endless chains of (3) and (6), the orders higher than eight will be ignored since the amplitude of which are negligible. It can also be seen from Fig. 4 that second-order power in the proposed approach is independent from m since it is designed same as OBC rating, and the higher dc-offset ratio m will lead to lower other self-created ac power in the circuit (higher order ac power of 4^{th}, 6^{th}, 8^{th}, …), this has not been investigated in the previous literatures. If second-order power of the grid in (2) are equal to that from (8) to achieve the ideal decoupling purpose, thus:

$$\left[l-1+2\cdot m\cdot(l+1)\right]\cdot C_t = \frac{V_g\cdot I_g}{\omega\cdot V_{ac(2)}\cdot V_{Link}} \tag{11}$$

Since decoupling capacitors are designed to absorb second-order power of the grid, the calculation of which can be done by setting m to zero to reduce the complexity. The relationship of top and bottom capacitors is therefore obtained by:

$$(l-1)\cdot C_t = C_b - C_t = \frac{2\cdot V_g\cdot I_g}{\omega\cdot V_{Link}^2} = \frac{2\cdot P_g}{\omega\cdot V_{Link}^2} \tag{12}$$

The relationship of $C_{bot} - C_{top} \geq 70$ uF is therefore obtained based on (12) with P_g = 7.4kW and V_{Link} = 820V. In the proposed method, the bottom capacitor with higher dc voltage component and capacitance value absorbs a higher amount of second-order power compared to the top capacitor which has lower dc voltage component and capacitance value.

The equivalent capacitance of dc-link as a function of switching frequency and desired ripple is expressed by:

$$C_{eq} = \frac{P_g\cdot D}{V_{Link}\cdot\Delta V_{Link,sw}\cdot f_s} \tag{13}$$

where D is a duty cycle of the PFC circuit, $\Delta V_{Link,sw}$ is the dc-link voltage ripple at switching frequency, and f_s is the switching frequency of the PFC circuit.

The above equivalent capacitance is also obtained based on each decoupling capacitor by:

$$C_{eq} = \frac{C_b\cdot C_t}{C_b + C_t} = \frac{\left(C_t + \dfrac{2\cdot P_g}{\omega\cdot V_{Link}^2}\right)\cdot C_t}{2\cdot C_t + \dfrac{2\cdot P_g}{\omega\cdot V_{Link}^2}} \tag{14}$$

Therefore, minimum capacitance of top capacitor can be obtained from (13) and (14) by:

$$C_{t,\min} = \sqrt{\left(\frac{P_g}{\omega \cdot V_{Link}^2} - C_{eq}\right)^2 + C_{eq} \cdot \frac{2 \cdot P_g}{\omega \cdot V_{Link}^2}} - \left(\frac{P_g}{\omega \cdot V_{Link}^2} - C_{eq}\right) \quad (15)$$

The required capacitances as a function of switching frequency are shown in Fig. 5. In this project, f_s and $\Delta V_{Link,sw}$ is set to 50kHz and 8V, respectively. The minimum capacitance of top and bottom capacitors are therefore obtained by 16uF and 86uF, respectively, yielding l_{min} = 5.4.

The comparison of decoupling capacitors between the proposed method and previous research is shown in Fig. 6. It can be observed that AC power decoupling has larger capacitance due to zero dc voltage component [19] – [21]. The line-frequency decoupling approach with balancing capacitors has large capacitance since its equivalent capacitance is high, which is calculated same as the right side of (12). Moreover, due to balancing capacitance approach, each capacitor must be twice of the equivalent capacitance worsening the required capacitance value [14] - [17]. Authors in [15] used the unequal capacitance to increase the robustness of controller under nonideal grid. However, its unbalancing strategy is opposite from our proposed strategy in such a way that bottom capacitor in [15] has smaller capacitance value than top capacitor. This strategy is however not beneficial because it reduces the power decoupling capability, as seen in (8). Moreover, equivalent capacitance given in [15] is same as [16] – [18] which is much larger than this paper.

The relationship between peak 2nd harmonic current of the decoupling inductor as a function of *m* and *l* is described in (16), which is obtained from (6) and (10), and is shown in Fig. 7.

$$i_{L,pd(2)} = \frac{-(l+1) \cdot C_t \cdot 2 \cdot V_g \cdot I_g \cdot \cos(2 \cdot \omega \cdot t + \theta_2)}{\left[l - 1 + 2 \cdot m \cdot (l+1)\right] \cdot C_t \cdot V_{Link}} \quad (16)$$

It can be observed that with same decoupling capacitors, the peak current of decoupling inductor reduces as *m* and *l* increase. However, with a given second-order power and dc-link voltage, m must be designed so that the peak voltage of the bottom capacitor does not exceed dc-link voltage. The selection of decoupling capacitors is a challenging task since their voltages consist of both dc and low-frequency ac components. The dc-voltage rating of the decoupling capacitor is selected based on its peak voltage which is assumed to be dc-link voltage as the

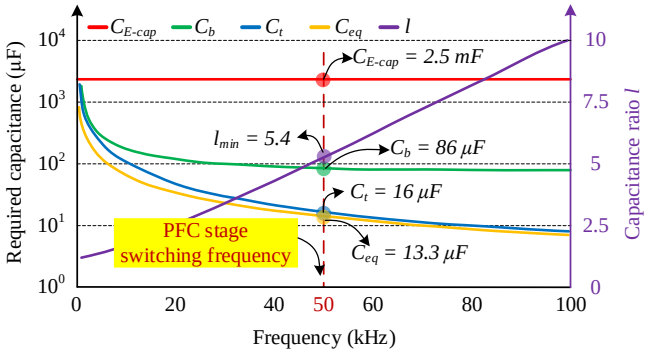


Fig. 5. Required capacitance calculated at $\Delta V_{Link,sw}$ = 8V.

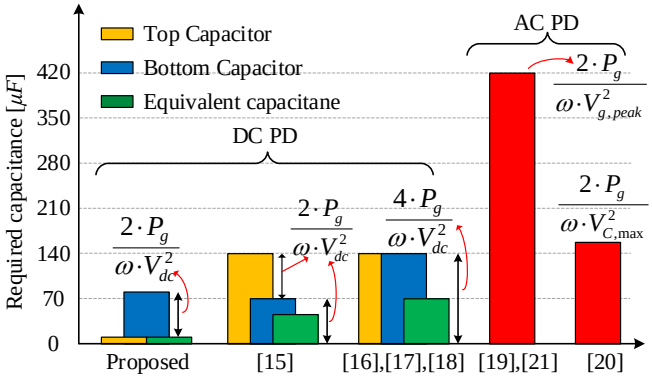


Fig. 6. Capacitance comparisons between the proposed approach and other counterparts

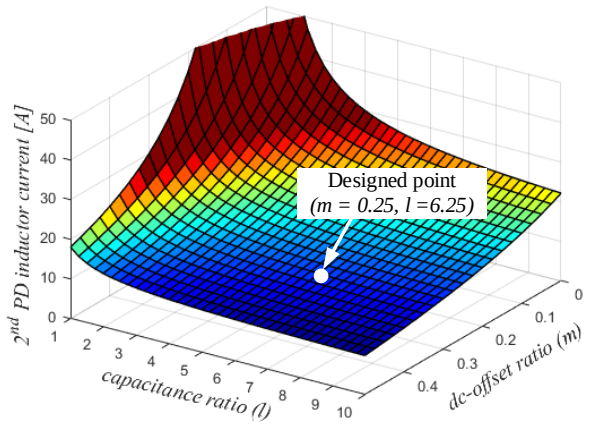


Fig. 7. PD inductor current as a function of *m* and *l*.

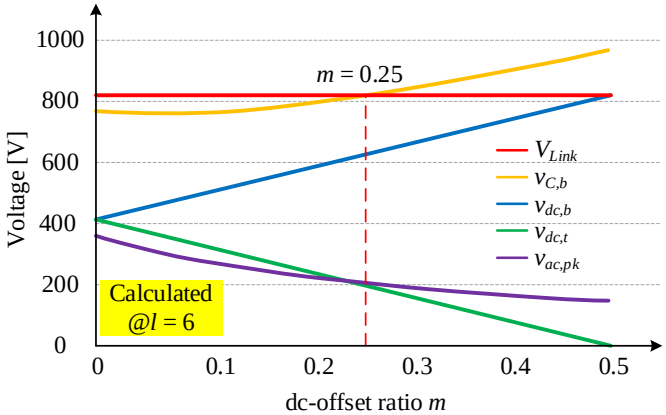


Fig. 8. Decoupling capacitor voltages as a function of *m*

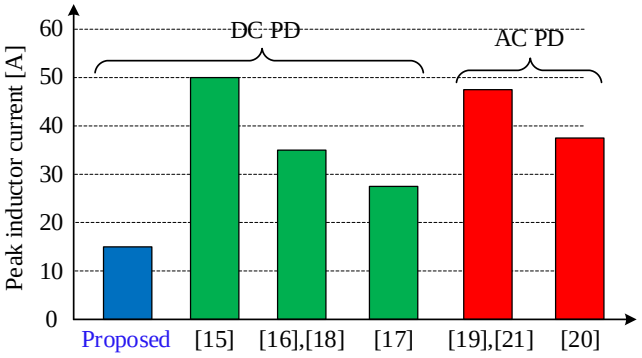


Fig. 9. Decoupling inductor current comparison

worst case in this paper, while ac voltage rating depends on *m*. Lower value of m leads to higher ac voltage rating and vice versa. Since film capacitor is used for decoupling purpose, the dc voltage rating of which is usually several times higher than its ac voltage rating. Fig. 8 shows the dc and ac components of the decoupling capacitors. In this paper, considering the availability and margins, the actual value of decoupling capacitors used for experiment are C_{top} = 15uF and C_{bot} = 100uF, l = 6.25. The dc-link voltage is design maximum at 820V, thus film capacitor BLH505K901A062 with ac voltage rating of 230V_{rms} is selected considering its low-profile benefit. Therefore, *m* can be theoretically designed between 0.05 to 0.25 considering 10% margin for ac voltage rating. However, in practical *m* is designed at its maximum possible value of 0.25 to minimize the self-created power and inductor current, as seen in Fig. 4.

The comparisons of the decoupling inductor current (peak) between the proposed method and other counterparts are shown in Fig. 9. It can be observed that, the proposed method has lowest inductor current due to lower top capacitance value. The unbalance strategy in [15] has another disadvantage is that its inductor current is very high due to higher top capacitance value.

III. Modelling and Control Algorithm

This section describes the proposed control algorithm for the system including PFC stage and HSC-PD circuit. A small-signal model of HSC-PD will be presented, after that, the implementation of two parallel controllers is explained to realize the best compromise between the PFC stage and the PD circuit.

1) *Modeling HSC-PD circuit*

HSC-PD circuit in Fig. 2 can be considered as a buck converter with input voltage and output voltage are V_{Link} and $v_{C,b}$, respectively. Hence, the voltage across top capacitor $v_{C,t}$ will be naturally obtained as a result of these two input and output voltages. Top switch S_t is the main switch of the converter, and its duty cycle is controlled to generate the desired output voltage, while the bottom switch S_b is switched complementarily with S_t. The converter operates under continuous conduction mode. The average model of HSC-PD with current and voltage is defined as:

$$\begin{cases} \bar{v}_{cp}(t) = d(t)\cdot \bar{v}_{ap}(t) \\ \bar{i}_a(t) = d(t)\cdot \bar{i}_c(t) \end{cases} \tag{17}$$

The average voltage and current are functions of duty cycle '*d*' and termed as the averaged PWM switch model. The linearization of PWM switch model and ignoring second-order terms will result in the small signal PWM switch model under CCM as:

$$\begin{cases} V_{cp} + \hat{v}_{cp}(t) = D\cdot V_{ap} + \hat{d}(t)\cdot V_{ap} + D\cdot \hat{v}_{ap}(t) \\ I_a + \hat{i}_a(t) = D\cdot I_c + \hat{d}(t)\cdot I_c + D\cdot \hat{i}_c(t) \end{cases} \tag{18}$$

The small signal circuit model of the HSC-PD circuit is therefore obtained, as shown in Fig. 10, which is used for the design and development of the controller. The transfer function for duty cycle-to-inductor current (19) and duty cycle-to-output voltage (20) is obtained by considering $\hat{v}_{Link}(s)$ = 0. Here, the output voltage is the ac ripple component in the output dc voltage of HSC-PD circuit. The duty cycle to output voltage transfer function of HSC-PD circuit is similar to [16] and capacitor voltage possessing the same ac component.

$$G_{PDi}(s) = \frac{\hat{i}_{Lpd}(s)}{\hat{d}_{pd}(s)} = \frac{(l+1)\cdot C_t \cdot V_{Link}\cdot s}{L_{pd}\cdot(l+1)\cdot C_t \cdot s^2 + 1} \tag{19}$$

$$G_{PDv}(s) = \frac{\hat{v}_{ac(n)}(s)}{\hat{d}_{pd}(s)} = \frac{V_{Link}}{L_{pd}\cdot(l+1)\cdot C_{top}\cdot s^2 + 1} \tag{20}$$

From (19) and (20), current-to-output voltage transfer function of HSC-PD circuit is obtained as

$$G_{PDiv}(s) = \frac{\hat{v}_{ac(n)}(s)}{\hat{i}_{Lpd}(s)} = \frac{1}{s\cdot(l+1)\cdot C_t} \tag{21}$$

2) *Proposed control algorithm*

PI-controller is the most commonly used for the dc reference regulation without steady-state error in synchronously rotating dq frame. PR controller are employed for the reference tracking in stationary frame αβ [28]**.** The PI controller in synchronously rotating dq frame is equivalent to the PR controller in stationary αβ frame [29], however, this holds true mainly for the fundamental frequency components. Considering this, the PR controller requires lesser computation burden as there is no transformation required. PI- controller is capable of tracking the dc reference corresponding to the

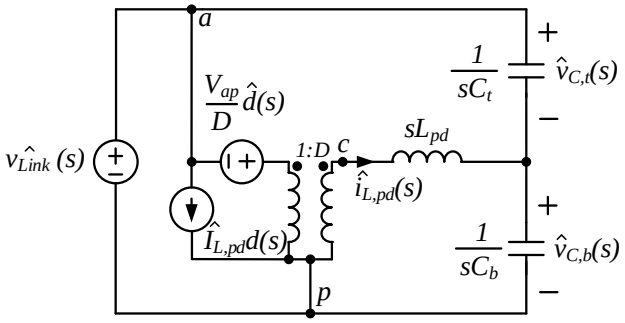


Fig. 10. Small signal model of HSC-PD circuit

fundamental freuqncy only. Therefore, the PR controller is required in the feedback control loop for multi-frequency control considering the double-line frequency and fourth line frequency compensation.

The proposed control loop in Fig.11 is the amalgamation of PFC-stage controller and PD controller offering multifrequency compensation with an additional duty-based feedforward control. The top part of the control structure is the PFC stage consisting of a PI-based outer voltage control loop followed by co-ordinate transformation and a PI-based inner-current control loop in a stationary frame. The bottom part of the control structure consists of the PR-based multifrequency control in the rotating synchronous frame and duty-based feedforward control in the inner current control loop. The top and bottom controller structure is employed as an independent parallel control loop with the same bandwidth response for the inner current control loop.

The PFC stage controller responsible for the regulation of dc-link voltage. The dc voltage error fed to PI controller of the outer voltage control loop providing the equivalent dc current. After the co-ordinate transformation, the ac grid current error passed through the PI controller of the inner current control loop to generate reference duty cycle for the switches.

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{22}$$

The design of the PFC-stage controller must be in accordance with the HSC-PD controller to achieve the optimized performance of the system. The proposed active power decoupling control technique is intended to reduce the equivalent capacitance. However, the value of capacitance and ripple in the voltage are correlated. Reduction in dc capacitance leads to an increase in the voltage fluctuation at the dc-bus. It is crucial during the transients under load change and change in input power. Therefore, the outer voltage loop of PFC is required to have a higher bandwidth compared to the conventional PFC scheme to regulate dc-link voltage faster through current reference. Considering the above-mentioned issue and criteria, the cut-off frequency of the inner current loop is chosen to be $f_{c\_inner} = \frac{f_{sw}}{10}$ and the cut-off frequency of the outer voltage loop is chosen to be at least 2 times of grid frequency $f_{c\_outer} \geq f_{grid} * 2$. In [17] and [18] the outer voltage loop cut-off frequency is between 200-300Hz, and higher capacitance values are used. The lower capacitance values used in this paper and the outer voltage control loop is designed with slightly higher bandwidth to accommodate that effect. The frequency response using the bode plot is demonstrated in Fig. 12 for the PFC controller including both the voltage control loop as well as the current control loop. As mentioned above, the cut-off frequency for the outer voltage control loop is $f_{c\_outer} = 370Hz$ with 90^0 phase margins. The inner current control loop is designed with cut-off frequency of 7 kHz and 75^0 phase margins.

The multi-frequency decoupling control is implemented with unequal dc offset for the designed HSC-PD circuit having an unequal capacitor. PR controller had been the choice of controller for the multi-frequency control as it possesses the infinite gain at the desired frequency that provides the zero steady-state error. The PR controller transfer function is given by (23) with a damping constant near the resonance frequency for system stability. PR-controller is used to compensate for the multi-frequency harmonic components specially double-line and four-line frequency components in the capacitor voltage. The multi-even-harmonic component is generated using current reference for the inductor in PD circuit.

$$G_{PR}(s) = K_p + \frac{2 \cdot K_r \cdot \omega_c \cdot s}{s^2 + 2 \cdot s \cdot \omega_c + \omega_o^2} \tag{23}$$

Nevertheless, the implementation of the PR controller in the digital environment is an issue because of the programming complexity for a real experimental system. The implementation of the PR controllers on the digital processor requires dicretization and two times delay corresponding to the discretization of the transfer function. The PR-controller is implemented using the second-order generalized integrator (SOGI) in the digital environment [30] possesses complex

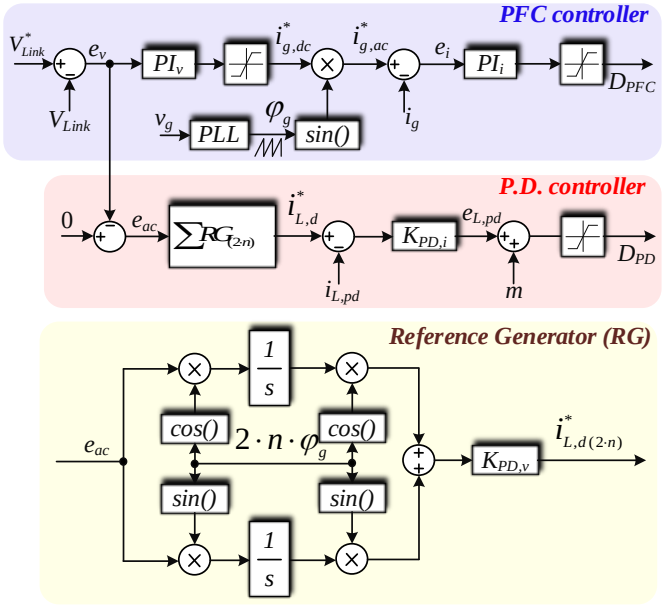


Fig. 11. Block diagram of the proposed control method

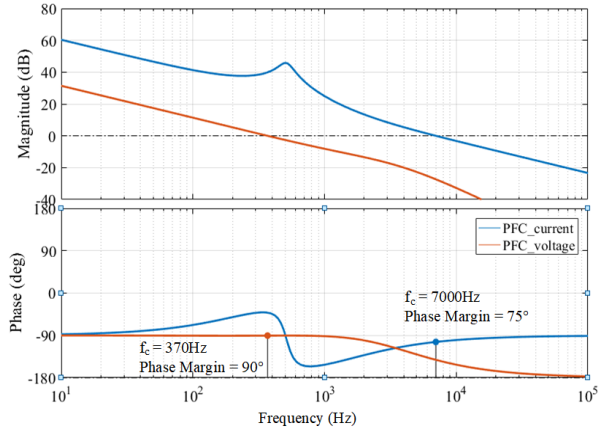


Fig. 12. Bode plot of dual-loop control of the PFC circuit

structure and delay. The discretization method significantly impacts the Stability and performance of the PR controller [31]. Therefore, needed a special attention to avoid instability by restraining the actual performace of PR. The frequency response is comparatively not good compared to the integral control action of the PI-controller.

In this paper, the co-ordinate transformation $\alpha\beta/dq$ is proposed in Fig.11 to change n-order-line-frequency (n=2,4,6,..) to DC signal for the implementation of the PR controller. The integral control action is employed to generate equivalent d-axis and q-axis signals and further pass through dq/αβ transformation with infinite DC gain instead of limit gain in [28]. The implementation of the integral control action is simpler and ultimately results in the reduced DSP memory utilization and calculation weights, consequently, making it cost-effective as digital processor cost depends on memory and computing capability. The unbalanced $\alpha\beta/dq$ transformation [32] is used instead of conventional $\alpha\beta/dq$ transformation for easier implementation. The conventional $\alpha\beta/dq$ need 90° delay to α input signal to generate β axis signal through OGM - Orthogonal (imaginary) term generation method. The difference is unbalanced $\alpha\beta/dq$ transformation has a half gain and a negative term that have no significance.

The outer voltage loop of HSC-PD should have to be designed with larger bandwidth as compared to PFC stage outer voltage loop. The outer voltage loop bandwidth of the HSC-PD circuit has a dominant effect on the system performance. The smaller bandwidth compared to the PFC stage lead to a very high voltage overshoot at dc-link. Furthermore, the bandwidth similar to the PFC stage has a better response considering overshoot at dc-link, however, leads to an oscillation in dc voltage and grid current. This ultimately results in the system unstability. Therefore, the larger outer voltage

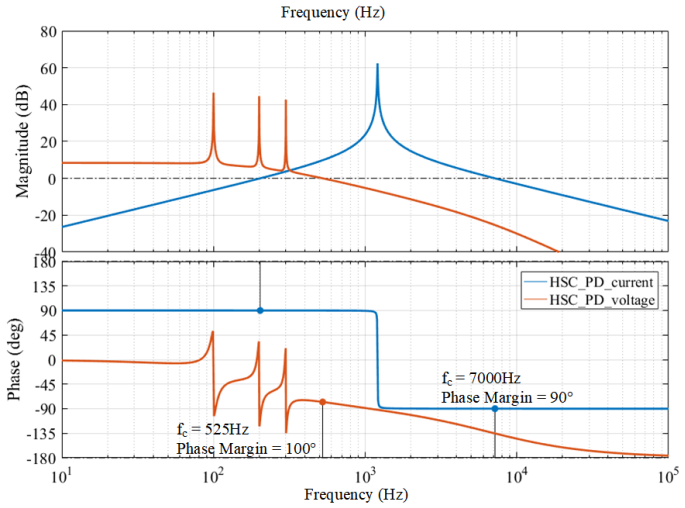
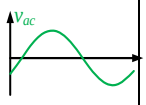
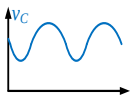
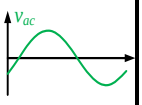
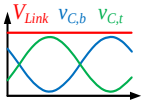
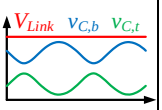
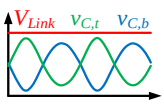
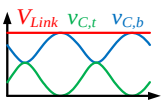


Fig. 13. Frequency response of HSC-PD circuit.

loop bandwidth of the HSC-PD circuit is desirable to achieve a faster response with a minimized overshoot at dc-link voltage. The inner current loop of HSC-PD should have a cut-off frequency at $f_{c\_inner} = \frac{f_{sw}}{10}$ and resonant gain should be tuned to have lower response than the PFC stage but still get enough gain to attenuate ripple on DC-Link. The frequency response of HSC-PD circuit in Fig.13 is investigated using bode-plot for current control loop as well as voltage control loop. The current control loop has a cut-off frequency of 7000Hz and 90^0 phase margins. The voltage control loop has three resonant frequencies to compensate the double-line (100Hz), fourth line (200Hz) and sixth (300Hz) frequency harmonics with cut off frequency of 525Hz and 100^0 phase margins. The higher cut-off frequency of outer voltage. Finally, the overall comparison

TABLE I
COMPARISONS OF THE PROPOSED HSC-PD WITH OTHER COUNTERPARTS

AC Decoupling			DC Decoupling			
[19]	[20]	[21]	[16],[18]	[17]	[15]	**Proposed**
						
$C_{pd} = \frac{2 \cdot P_g}{\omega \cdot V_{g,peak}^2}$	$C_{pd} = \frac{2 \cdot P_g}{\omega \cdot \left(\frac{2}{3} \cdot V_{Link}\right)^2}$	$C_{pd} = \frac{2 \cdot P_g}{\omega \cdot V_{g,peak}^2}$	$C_{eq} = \frac{2 \cdot P_g}{\omega \cdot V_{Link}^2}$	$C_{eq} = \frac{2 \cdot P_g}{\omega \cdot V_{Link}^2}$	$C_{eq} = \frac{2 \cdot P_g}{\omega \cdot V_{Link}^2}$	$C_{eq} = \frac{P_g \cdot D}{V_{Link} \cdot \Delta V_{Link,sw} \cdot f_s}$
			$C_{bot} = C_{top} = \frac{4 \cdot P_g}{\omega \cdot V_{Link}^2}$	$C_{bot} = C_{top} = \frac{4 \cdot P_g}{\omega \cdot V_{Link}^2}$	$C_{bot} < C_{top}$	$C_{bot} \gg C_{top}$
					$C_{top} - C_{bot} = \frac{2 \cdot P_g}{\omega \cdot V_{Link}^2}$	$C_{bot} - C_{top} = \frac{2 \cdot P_g}{\omega \cdot V_{Link}^2}$
Open loop PR, SVPWM	Close loop PR	Close loop	Open loop [16] Close loop [18] PR-50Hz	Close loop Multi - PR DC-offset	Close loop Multi-PR	Close loop Proposed multi- unbalanced αβ/dq DC-offset

of the proposed HSC-PD with other counterparts is shown in Table I.

IV. Experimental Results

The experimental results of the 7.4kW interleaved totem-pole PFC with HSC-PD in Fig.14 are demonstrated in this section to verify the above analysis and System design parameters summarized in Table II. The grid current, grid voltage, dc-link voltage, and decoupling inductor current at full load condition are shown in Fig. 15(a). Grid current and voltage are controlled in-phase with measured power factor of 0.9986. THD of the grid current is low of 3.6% due to interleaved approach even though each inductor current has a significantly higher THD of 5%, as shown in Fig. 15(b).

1) Decoupling capacitor and inductor performance

The decoupling capacitor voltages measured at half and full loads are shown in Fig. 16. The voltages across decoupling capacitor are fluctuating with the same frequency but 180° phase-shift. Dc-offset votlages of the bottom and top capacitors are set to 25% and 75% of the V_{Link}, resepctively, resulting in m = 0.25. DC-link voltage is flat with low ripple of 12.6V at full load meaning that the PD circuit functions well with low

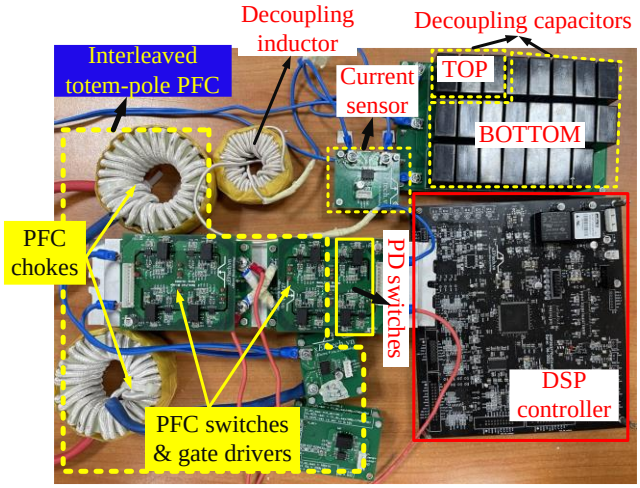
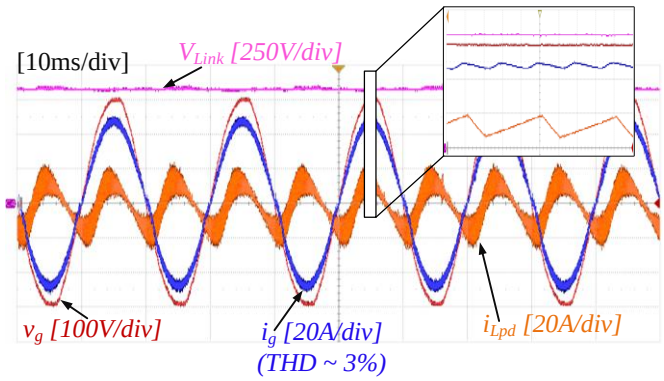


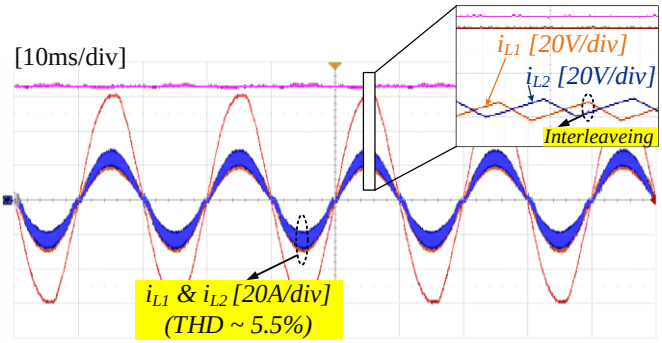
Fig. 14. Experimental prototype of the 7.4kW interleaved boost PFC and HSC-PD.

Table II
Designed Parameters of The Proposed Converter

Items	Values
Power rating	7.4 kW
Dc-link voltage, V_{Link}	820 V_{dc}
Grid voltage, v_g	220 V_{rms}
Switching frequency of PFC circuit	50 kHz
Switching frequency of PD circuit	50 kHz
Input inductors, L_1, L_2	500 µH
Decoupling inductor, L_{pd}	250 µH
Decoupling bottom capacitor, C_b	100 µF
Decoupling top capacitor, C_t	15 µF

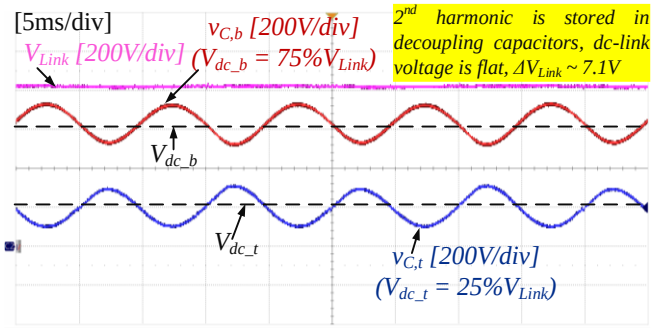


(a)

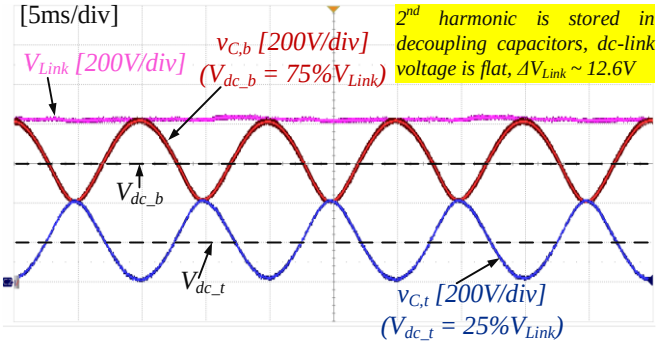


(b)

Fig. 15. Experimental results of the PFC circuit: (a) Grid current with low THD and high PFC is achieved at rated dc-link voltage, and the double-line frequency appears at the decoupling inductor current; (b) interleaved approach is achieved at the input currents.



(a)



(b)

Fig. 16. Decoupling capacitor voltage: (a) 50% of load; (b) full load

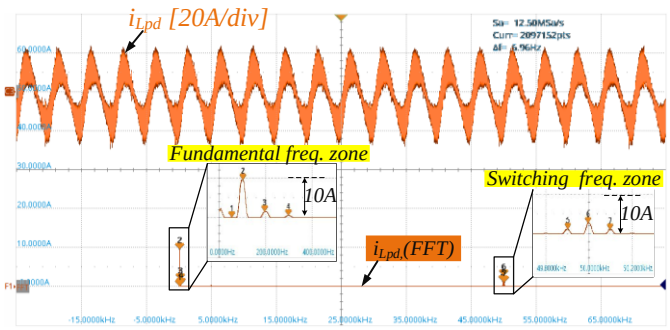


Fig. 17. Decoupling inductor current and its FFT analysis.

dc-link capacitance, and the 2nd harmonic is almost cancelled in both cases 50% and 100% of load. The ac components of the decoupling capacitors voltage at 50% of load has lower magnetude than that of the 100% of load.

The FFT analysis of the decoupling inductor current is shown in Fig. 17. There are two different harmonics zones; the fundermantal frequency zone around 50Hz, and the other harmonic zone is at around swtiching frequency of 50kHz. It can be seen from Fig. 17 that, the amplitude of 2nd harmonic is dominant over other components, verified the theoretical analysis, as shown in Fig. 4.

A step load changes from half to full load is shown in Fig. 18. In general, the transient of HSC-PD capacitors and inductor is smooth. The dc-link voltage drops within a short period of time at the transient because it is regulated by conventional dual-loop controller of the totem-pole PFC circuit without any effort to support the fast transient in addition to low equivalent dc-link capacitance and non-ideal grid in our facility. However, it worth to mention that fast dynamic response is not typically a critical requirement in OBC application since the battery voltage or battery current changes very gradually over an extended charging period. Therefore, the design in this paper does not specifically target this performance aspect.

The method based on conventional PR-controller in [15] and the proposed methods are both implemented on a DSP TMS320F28377D microprocessor, and the experimental comparison of the computation times for the two methods is shown in Fig.19. The results clearly highlight the computational efficiency of the proposed method, which outperforms the conventional approach with a faster calculation time of 389ns.

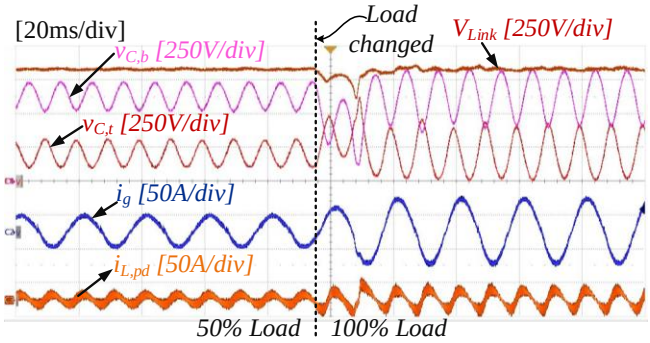


Fig. 18. Transient response of the step load changed from 50% to 100% of load.

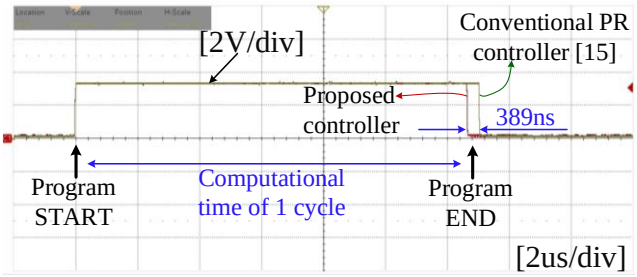


Fig. 19. Computation times for the practical implementation of both the conventional and proposed methods on a DSP TMS320F28377D.

2) Comparisons between the proposed HSC-PD and conventional E-cap method

The measured efficiency of the conventional totem pole PFC with E-cap and the proposed abroad with HSC-PD is shown in Fig. 20, full-load efficiency drops about 0.5% with PD due to additional losses of the HSC-PD circuit. The dropped efficiency is more significant under light load condition because the additional switching loss and core loss of the HSC-PD circuit are more dominant other conduction losses. It is however worth to mention that, in OBC applications the

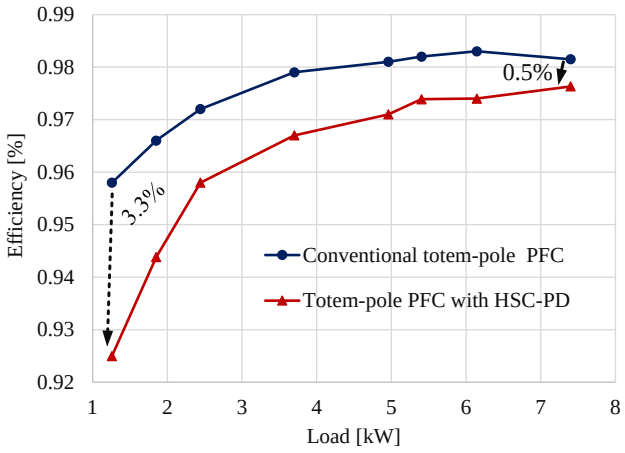


Fig. 20. Measured efficiency of the totem-pole PFC with and without PD circuit.

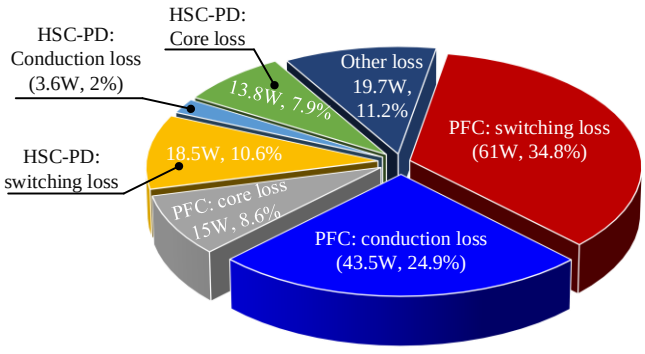


Fig. 21. Loss distribution of the Interleaved Totem-pole PFC with HSC-PD at V_g = 220V, V_{Link} = 820V, P_o = 7.4kW, f_s = 50kHz.

TABLE III
SELECTED DEVICES FOR HSC-PD AND CONVENTIONAL E-CAP METHOD

Component	HSC-PD	E-cap
Capacitor	23x BLH505K901A062	148x 450BXW68MEFR18X25
Switch	2x NTHL040N120SC1	
Gate driver IC Power supply	2x UCC5320SCD 2x PDS2-S12-S24-M-TR	
Core	1x CH400060	

converter operates under heavy load most of the time during one charging cycle.

The loss distribution of the converter at the full load is shown in Fig. 21. Due to hard-switching condition, switching loss of main switches of the interleaved totem-pole PFC is the most dominant loss. The HSC-PD contributes 20.5% to the total loss of the converter at full-load condition. Within the HSC-PD, the switching loss and inductor core loss dominant over the conduction loss due to low current rating of the decoupling circuit.

Furthermore, with the selected components are presented in Table III, total cost and volume of the proposed HSC-PD are

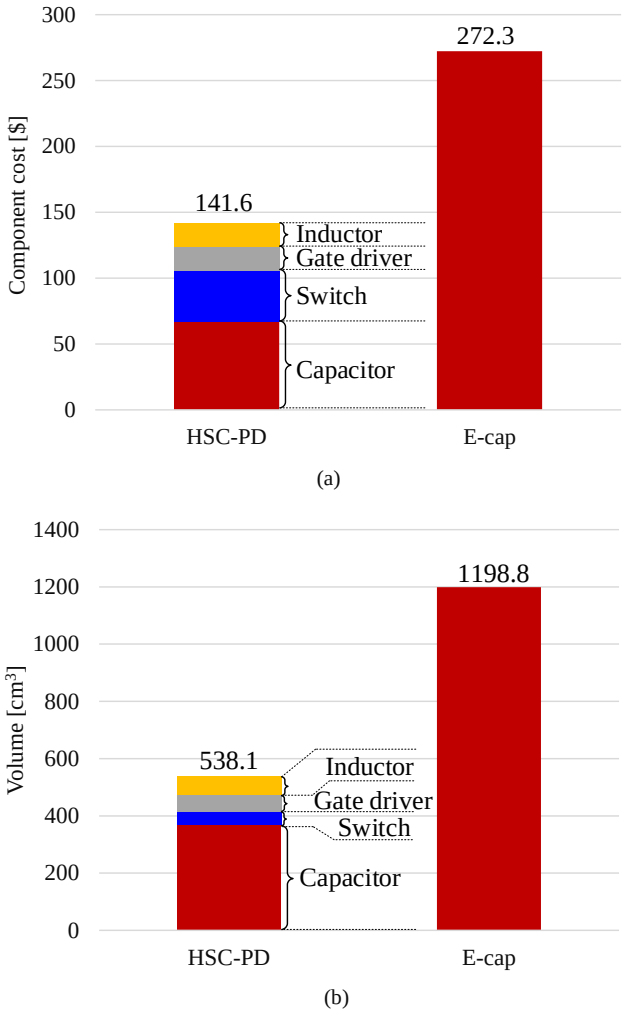


Fig. 22. Cost and volume comparison between the proposed HSC-PD and E-cap: (a) cost; (b) volume. (Cost is based on digikey.com accessed Jan. 2023)

1.9 and 2.2 times lower than that of the conventional E-cap method, respectively, as demonstrated in Fig. 22. Therefore, while acknowledging a marginal reduction in efficiency, the substantial cost and volume savings, complemented by improved reliability, underscore the advantageous trade-off of our proposed HSC-PD approach. This underlines the HSC-PD's potential as a viable alternative to traditional methods, paving the way for more compact and cost-effective OBC.

3) Inrush current and precharge resistor

In OBC application, precharge circuit, which typically consits of one relay and one precharge resistor, is usually used at the input side to limit the inrush current when the OBC is connected to the grid, as seen in Fig. 23(a). The equivalent circuit of the converter when OBC is connected to the grid without and with precharge resistor is shown in Fig. 23(b) and Fig. 23(c), respectively. Assumming grid voltage is fixed, the rating of precharge resistor is mostly based on dc-link capacitance so that the higher dc-link capacitance the higher power needed of the precharge resistor. Therefore, in case of

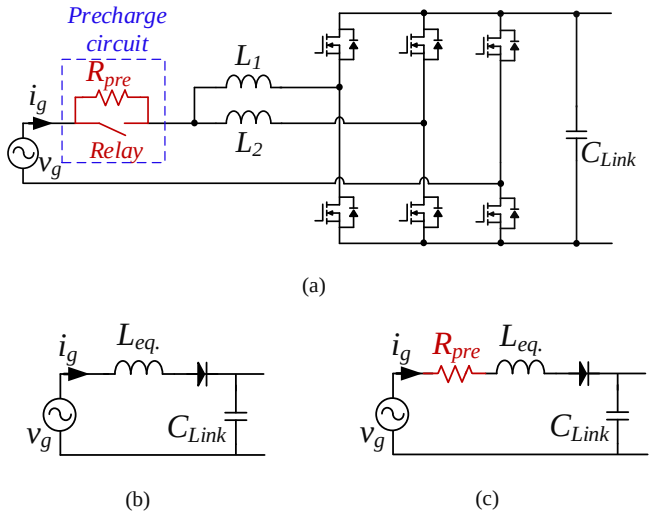


Fig. 23. Precharge circuit and equivalent circuit of AC/DC converter during start-up: (a) interleaved totem-pole PFC with precharge circuit; (b) equivalent PFC circuit during start-up without precharge resistor; (c) equivalent PFC circuit during start-up with precharge resistor.

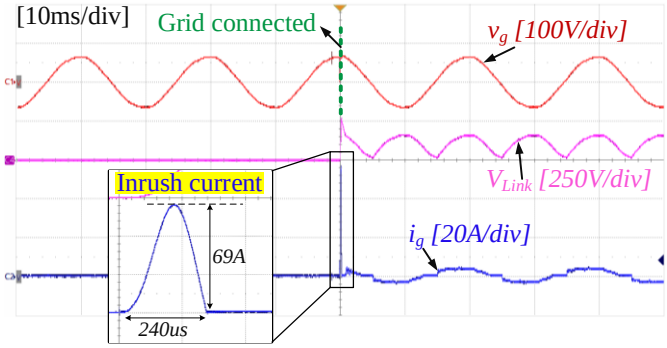


Fig. 24. Experimental waveforms of the inrush current when connecting the HSC-PD based PFC circuit with low dc-link capacitance to the grid without precharge resistor.

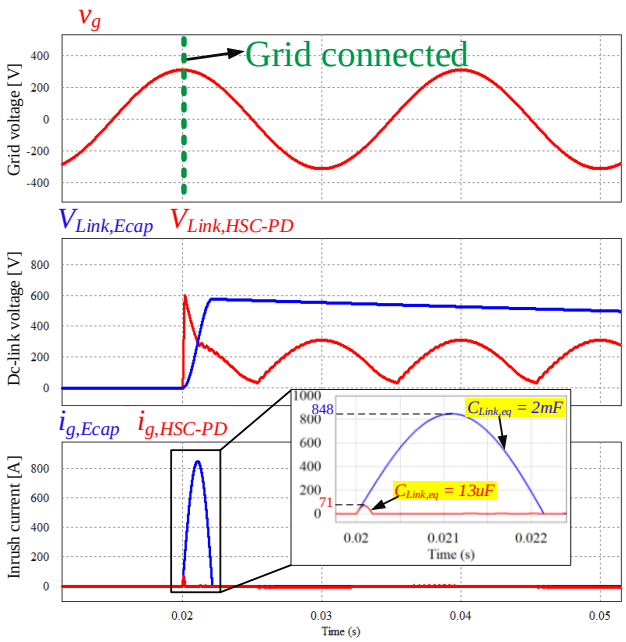


Fig. 25. Inrush currents comparison between conventional PFC with large E-cap and proposed HSC-PD based PFC with low capacitance F-cap.

using PD circuit, the precharge resistor can be significantly reduced compared to that of the conventional rectifier with large E-cap, reducing volume and cost.

Fig. 24 shows the input inrush current of the totempole PFC using HSC-PD circuit. The inrush current is within the acceptable magnetute and short interval due to small dc-link capacitance. The experiment with conventional totempole using large dc-link capaciance with E-cap could not be performed without prechage circuit due to safety issue. However, the simulation results of the inrush current in two cases are shown in Fig. 25. It can be seen that the conventional rectifier with large dc-link capacitor has significantly larger inrush current compared to that of the proposed converter.

VI. Conclusions

In this paper, a new method for designing and controlling a Half-bridge Split Capacitor based Power Decoupling circuit (HSC-PD) is presented with the dominant of bottom capacitor over the top one. The proposed design approach is demonstrated to have the following addvantage over the previous works:

1) Smaller capacitance value of each decoupling capacitors
2) Smaller equivalent dc-link capcitance
3) Reducing the required ac voltage rating of the film capacitor, which is critical in high voltage applications such as 800V OBC due to the low availability and costly of the high ac voltage rating film capacitor.
4) Smaller decoupling inductor current

Moreover, the small signal model of the HSC-PD is presented, and the modified the feedback control of the HSC-PD is proposed based on the co-ordinate transformation αβ/dq, which reduces the memory utilization and calculation effort of the DSP microcontroller compared to the conventional PR implementation. In addition, the effect of dc-link capacitance to precharge resistor power rating is investigated, showing the additional advantage of proposed method. Finally, experimental results of the 7.4kW 820V interleaved totem-pole PFC with HSC-PD are given to demonstrate the superiorities of the proposed method.

While our proposed HSC-PD scheme presents several significant advantages, it does come with its own unique set of challenges. These include a marginal decrease in efficiency due to the incorporation of additional circuit elements, increased complexity in PCB and control design, potential limitations for applications requiring prolonged hold-up times due to low dc-link capacitance value, and meticulous selection requirements for capacitors, especially considering their current rating due to low capacitance of the top capacitor. These issues offer ample opportunities for further refinement and optimization in future research.

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Tuyen Dinh Nguyen (*Senior Member, IEEE*) was born in Binh Dinh, Vietnam, in 1982. He received the B.S. degree in electrical engineering from the Ho Chi Minh City University of Technology, Ho Chi Minh City, Vietnam, in 2004, and the Ph.D. degree from the University of Ulsan, Ulsan, South Korea, in 2012. He is currently an Associate Professor at the Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology, Vietnam National University. His research interests include power electronics converter, power electronics system integration, its industrial applications such as renewable energy and electric vehicle.

Long H. B. Nguyen received the B.S. degrees in Electrical Engineering in 2022 from HCMC University of Technology (Bach Khoa University), Ho Chi Minh City, Vietnam, where He is currently working toward the M.S. degree in Power Electronics. Since 2022, He has been a Power Electronics Engineer with xEVtech Co. Ltd., Ba Ria – Vung Tau, Vietnam. His research interests include PFC converter topologies, Power Decoupling algorithm, EV chargers.

Dong Tran received the B.S. degrees in Electrical Engineering in 2022 from HCMC University of Technology (Bach Khoa University), Ho Chi Minh City, Vietnam. Since 2022, He has been a Power Electronics Engineer with xEVtech Co. Ltd., Ba Ria – Vung Tau, Vietnam. His research interests include PFC converter topologies, Power Decoupling algorithm, EV chargers.

Ravi Nath Tripathi (*Senior Member, IEEE*) received a B.Tech degree in Electrical and Electronics Engineering from Graphic Era Institute of Technology (presently Graphic Era Deemed to be University), Dehradun, India, in 2011 and M.tech degree from Delhi Technological University, Delhi, India in 2013. He received his PhD degree from Kyushu Institute of Technology, Fukuoka, Japan in 2017 and after that worked as a post-doctoral researcher on the NEDO project from 2017-2020 at Next Generation Power Electronics Research Center, Kyushu Institute of Technology. He joined the Kyoto University of Advanced Science, Kyoto, Japan in 2020 as an assistant professor and currently working as an assistant professor at the Kyushu Institute of Technology. His research

interest is gate driving and system control for power semiconductor devices, power converter system development and control, renewable energy systems and virtual prototyping.

Hai N. Tran (M'21) received the B.S. and M.S. degrees in Electrical Engineering from HCMC University of Technology (Bach Khoa University), Ho Chi Minh city, Vietnam, in 2014 and 2016, respectively, the Ph.D. degree from Seoul National University of Science and Technology (SeoulTech), Seoul, Korea, in 2021. Since April 2021, He has been a Postdoctoral Researcher with the Nagamori Institute of Actuators, Kyoto University of Advanced Science, Kyoto, Japan. He is a founder of xEVtech Co. Ltd., Ba Ria – Vung Tau, Vietnam. His research interests include active snubber circuit, soft switching converter topologies, medium voltage, EV chargers, and magnetic design.
Dr. Tran received the 2022 *IEEE Transactions on Power Electronics* (TPEL) Prize Paper Award.