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Review

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Review

Paralleling of IGBT Power Semiconductor Devices and Reliability Issues

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Abstract: Paralleling of power semiconductor devices is inevitable considering their widespread application and exploitation in the extended horizon of these applications. However, paralleling of power semiconductor devices is prone to severe unbalancing corresponding to the non-idealities of device parameters, which leads to non-identical dynamic and static characteristics of the power devices, as well as the operating conditions and aging. Therefore, the currents are generally non-uniform and cause the derating of the system. This paper discusses and analyzes issues associated with the paralleling of IGBT power devices, which can evoke serious reliability issues. Furthermore, the paper examines the techniques and methodologies that have been proposed to reduce the issue of current unbalancing of parallel-connected power devices.

Keywords: power semiconductor device; paralleling; current unbalancing; reliability

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1. Introduction

The Si-IGBT is one of the extensively developed and commercially mature power devices that has been used in various high-power applications [1]. With the advent of wide-band gap (WBG) devices, power device technology received a major boost in terms of fast switching and extended thermal capability. The operations of power devices are constrained by voltage blocking and current-carrying capability, which consequently limit the power-handling capability of devices and power electronic systems [2]. The applications in industrial motor drives, energy–wind power generation converters, solar photovoltaic power generation converters, and automobiles require power semiconductor modules within the 1200/1700 V class [3]. Si-IGBT and WBG SiC-MOSFET devices are the major players for the 1200/1700 V class power devices and modules. Based on the market trend and surveys, the Si-IGBT is expected to play a major role in the industrial motor and home appliance segment, and the SiC-MOSFET is expected to play a major role in automotive and energy segments [4,5]. However, the corresponding application segments require high-current power modules that exceed the limit of the maximum current rating of a single chip. The power device chip sizes are constrained by several factors that ultimately limit the rating of a single chip. A single Si-IGBT chip for the maximum voltage capability of 1200/1700 V is limited by the current rating of approximately 200 A [4,6]. Furthermore, applications of the medium voltage class, i.e., 3.3 kV, 4.5 kV, and 6.5 kV, for high-power industrial drives, have similar current limitation constraints [7–9].

The paralleling of Si-IGBT chips/discrete devices is inevitable and extensively used for high-current applications, as shown in Figure 1, to realize the required current rating corresponding to the specific voltage class of the devices. Furthermore, paralleling provides compelling advantages: better performance-to-cost and cost-per-ampere ratios, flexible connection and operation, better thermal distribution, and high-power density [9–12]. The paralleling can be realized by different methods: paralleling of chips/discrete devices,

paralleling of half bridges/arms/legs, and paralleling of the modules [11,13]. The major problem and concern associated with the paralleling of power semiconductor devices is the current imbalance behavior due to non-idealities and system asymmetry factors [14,15]. The current imbalance behavior also varies corresponding to the paralleling technique and system configuration, which affects the asymmetry factors. The unbalancing can provoke major concerns, such as system derating and thermal derating due to non-uniform current sharing, which, in turn, may lead to stability, reliability, and failure issues of the devices, as well as the system [14,16].

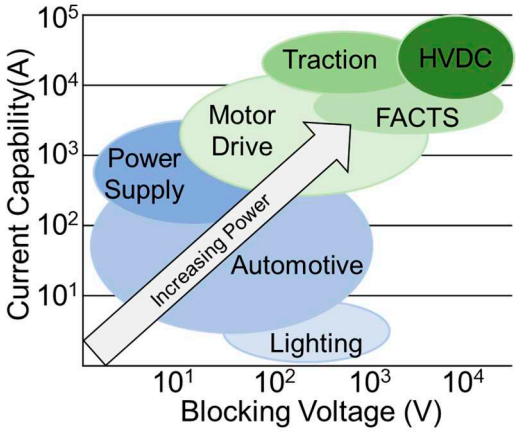

Figure 1. Current capability requirement corresponding to blocking voltage for application of power semiconductor devices [10].

The current imbalance is categorized as static and dynamic current unbalancing. The static and dynamic behavior of paralleled IGBTs was discussed in [17] in 1990. The non-idealities and asymmetry affecting the static unbalancing are the on-state voltage ($V_{CE,sat}$)/on-state resistance ($R_{ds,on}$), gate-emitter voltage (V_{GE}), junction temperature (T_j), and total loop resistance. The non-idealities and asymmetry affecting the dynamic unbalancing are threshold voltage ($V_{G,th}$), gate signal propagation delay ($t_{d,on}$; $t_{d,off}$), rise time and fall time of the gate signal (t_r; t_f), gate resistance (R_G), device parasitic capacitances, total power loop inductance, and gate loop inductance [18–21].

One rudimental means of minimizing unbalancing is the selection of the appropriate devices by ensuring the identical device parameters and other technical passive techniques [9,12,16]. However, this is just a preliminary step for the parallel power device system design and development because of the variable operating condition and environment, as well as the aging of the components. Different gate-driving strategies are implemented for parallel-connected power devices, which can be largely categorized as passive and active, to minimize the current imbalance. Passive techniques have the advantage of easy and low-cost implementation and may improve the current imbalance. However, optimizing the current sharing among the parallel-connected power devices is not possible. The active techniques provide improved current unbalancing to realize homogenous and optimized sharing by manipulating the gate signal corresponding to device performance and characteristics. However, the active control techniques address the implementation complexity and cost. The techniques for current balancing for parallel-connected devices are summarized as follows:

1. Device matching: Ensuring close matching of device parameters, such as $R_{ds,on}$ and $V_{G,th}$, helps promote current sharing among parallel devices. Devices with similar characteristics are selected and grouped together to minimize differences in their current-carrying capabilities.
2. Symmetric system layout: In general, many device manufacturers provide application notes for the paralleling of the power devices in the design and adoption of the symmetric system layout to minimize the connection impedances in the system

layout. This is also crucial concerning overall system stability, and symmetric system layout is vital because it ensures the appropriate gate-driving loop and power circuit loop design.

3. Passive control: Device matching and symmetric system layout techniques are also a kind of passive control method; however, this method does not employ any additional components in the parallel-connected power device system. In passive control techniques, passive components, such as common mode choke or differential mode choke, are used with the parallel-connected device system to minimize the current imbalance.
4. Active control: The active control technique monitors the parallel devices to maintain equal current sharing. In general, these circuits sense the individual device parameters to estimate the current unbalancing, and correspondingly regulate the gate signal to minimize the current imbalance and achieve homogenous current sharing.

Furthermore, an appropriate gate-driving system is required for parallel-connected power devices when employing the appropriate current-balancing technique. The fundamental categorization of gate-driving techniques shown in Figure 2 is the common gate driver (CGD) and individual gate driver (IGD) [14,16]. In the common gate-driving technique, the parallel-connected power devices are driven by a single gate-driving unit, and in the individual gate-driving technique, the power devices are driven by a corresponding separate gate drive unit (GDU) Figure 2. The gate-driving techniques possess their own advantages and disadvantages based on the GDU configuration, such as common emitters or separate emitters, and common auxiliary emitters or separate auxiliary emitters.

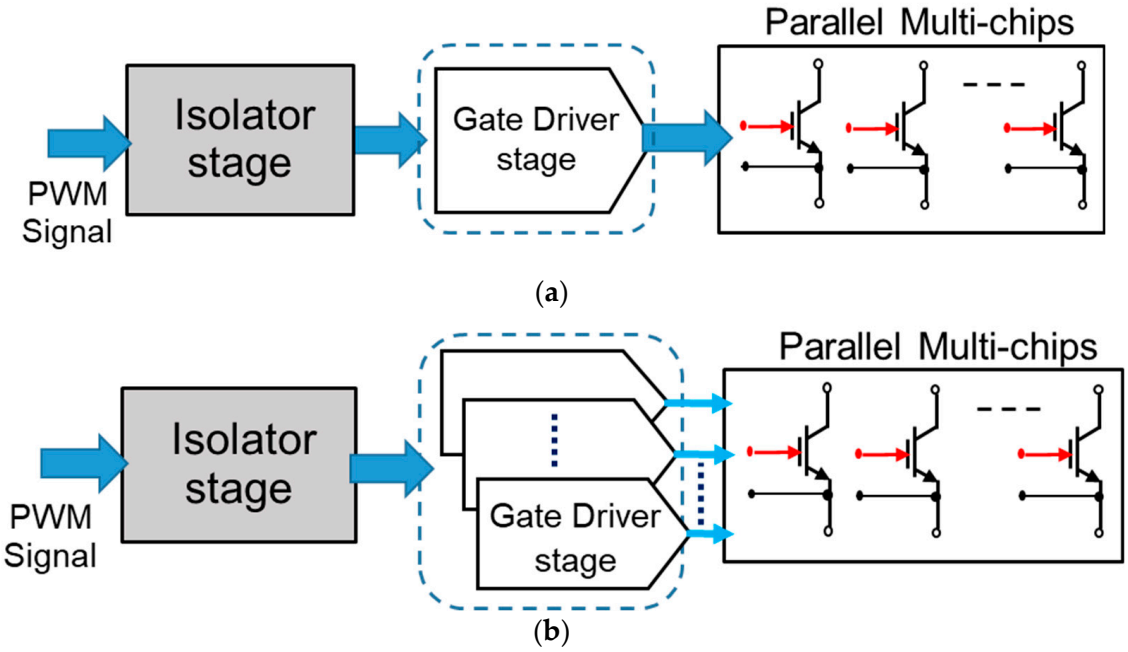

Figure 2. Gate-driving technique for parallel-connected power devices: (**a**) common gate driving (**b**) individual gate driving.

This paper discusses and investigates the gate-driving techniques implemented for parallel-connected power semiconductor devices. Further, it examines the study of the influence of parameters on the current imbalance of the devices in terms of device physics. Furthermore, the gate-driving techniques that have been used for the parallel-connected IGBT power devices are investigated and discussed considering passive and active current-balancing techniques that have been implemented to achieve improved/optimized current balancing. The paper is configured as follows: Section 2 presents the investigation into and study of the influence of system parameters on parallel-connected IGBT power devices. Section 3 examines the gate-driving techniques with active and passive current-balancing techniques, and Section 4 provides the inference in the form of a discussion.

2. Influence of System Parameters

The components of a parallel-connected system have direct, indirect, and cumulative influences on its performance, such as dynamic current sharing, static current sharing, unwanted junction temperature swing of the devices, oscillations, and frequent operation in the safe operating area (SOA) limit region. The system components influencing parallel-connected power devices are represented in Figure 3. The parallel-connected device system encompasses the device parasitic parameters, GDU parameters, and connection layout parameters, consisting of stray inductances and resistances. A schematic circuit diagram of a single device and gate-driving unit is represented in Figure 4.

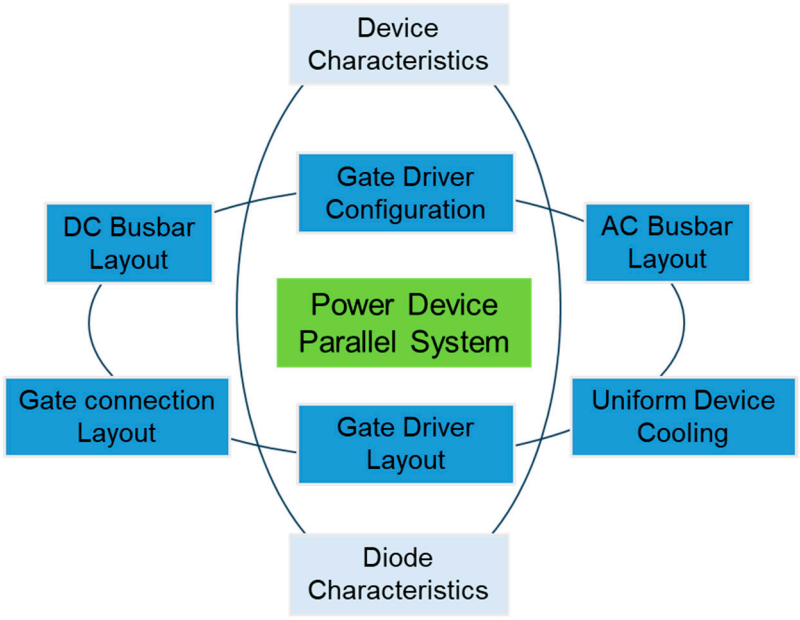

Figure 3. System components influencing the performance of parallel-connected power semiconductor devices [14,15,22,23].

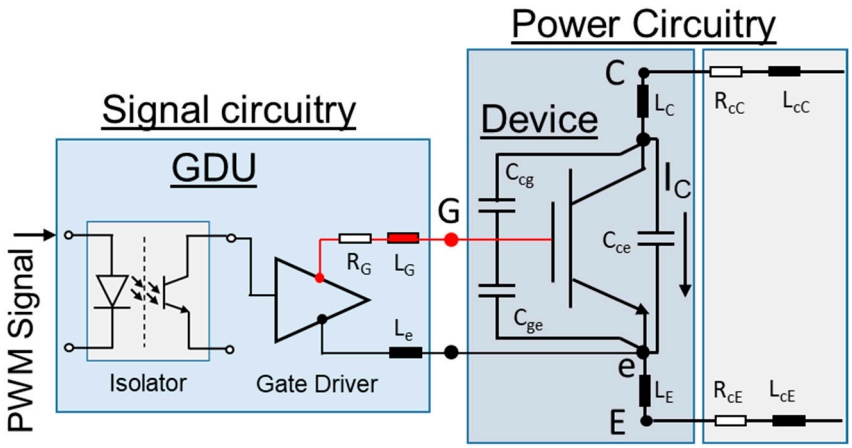

Figure 4. Schematic diagram of an IGBT and gate-driving system including the device parasitic, stray inductance, and capacitance of the connection layout.

2.1. Device Parameters

In this subsection, the co-relations of the device parameters are discussed corresponding to dynamic current unbalancing and static current unbalancing. The transfer characteristics of the device are as follows: the collector current (I_C) relates to V_{GE}, which is associated with the dynamic current balancing considering threshold voltage. The fundamental reason for the difference in device characteristics regarding the device parameters is

the fabrication process, in which it is extremely difficult to eliminate variation at different steps. The gate oxide layer thickness affects $V_{G,th}$, and a thicker oxide layer ultimately results in a higher $V_{G,th}$ for the conduction [24]. In addition, similar to the gate oxide thickness, the p-base doping concentration influences $V_{G,th}$ and an increase in doping ultimately increases the $V_{G,th}$ required for conduction [24]. Threshold voltage affects the dynamic current sharing during turn-on and does not have a significant role during turn-off considering the difference between the negative gate drive voltage and $V_{G,th}$ [25]. The device with lower $V_{G,th}$ turns on earlier, resulting in current imbalance.

The switching characteristic of the device is related to the capacitances formed between the gate and the insulating silicon oxide layer [26]. The gate-emitter capacitance and Miller capacitance of IGBT devices mainly impact the dynamic current imbalance in parallel [27]. The equivalent input capacitance comprising the gate-emitter capacitance affects the turn-on delay; a lower input capacitance means the device turns on faster and results in current imbalance. The common gate resistance in a parallel-connected IGBT system results in the limit of the increase in V_{GE} for slower IGBTs in the Miller region, thereby resulting in current imbalance [27].

Similarly, the output characteristic, also termed the static characteristic of the device, provides the relation between the device current and on-state voltage, i.e., collector current (I_C) and $V_{CE\ (sat)}$, respectively, for an IGBT. The gate oxide thickness and p-base doping also influence $V_{CE\ (sat)}$; higher gate oxide thickness and p-base doping concentration results in increased $V_{CE\ (sat)}$, and consequently higher $R_{ds,on}$ for the corresponding IGBT device and less static current under the paralleled device operation [24]. Furthermore, the forward voltage (V_F) of the diode and $V_{CE\ (sat)}$ in combination as a device parameter impacts the current sharing of the parallel-connected devices [25].

The effect of the device parameters, rate of change in the current (di/dt) and voltage (dv/dt), is discussed in [25] considering their major impact during turn-off. The device having higher di/dt will have an overshoot in current during turn-on, and during turn-off the IGBT having higher dv/dt reaches the dc-link voltage earlier than in the counterpart IGBT, thus leading to the high current overshoot in the counterpart IGBT. In [25], a selection criterion for IGBT device parameters is proposed considering di/dt and dv/dt.

2.2. Gate-Driving Parameters

The gate-driving layout determines the gate current path, and an asymmetric gate-driving layout results in parallel-connected power devices due to the asymmetric gate current path [9]. The gate-driving parameters in conjunction with the gate-driving layout affect the gate resistance (R_G), gate loop emitter inductance (L_e), gate-emitter voltage (V_{GE}), gate signal propagation delay ($t_{d,on}$; $t_{d,off}$), and rise time and fall time of gate signal (t_r; t_f), consequently leading to current imbalances among the parallel-connected power devices [19].

One of the vital parameters of gate driving is R_G, which governs multiple factors. The use of individual gate resistances is recommended to reduce the potential of oscillations and the effect of the Miller region [16,27,28]. The effect of unequal R_G on the current imbalance is demonstrated in [29] considering the different cases of R_G and demonstrating the linear unbalance rate corresponding to increase in variation between R_G. However, there is a sudden non-linear increase in current imbalance after resistance difference higher than 30%. The gate resistor selection is discussed in [27,30], which mentions its effect on the following parameters: turn-on and turn-off times, switching losses, dv/dt across the collector-emitter, di/dt, and EMI due to switching. An increase in R_G increases turn-on and turn-off times, and consequently decreases dv/dt, di/dt, and EMI, but increases switching losses.

The current imbalance during turn-off is discussed in [31] considering a change in R_G for a parallel-connected IGBT device operating with equal R_G. Although parallel-connected devices operate with equal gate resistance, an increase in gate resistance results in a significant change in current imbalance during turn-off. This is due to the change in the turn-off delay time difference corresponding to an increase in R_G.

The current imbalance during turn-off due to unequal R_G, $t_{d,off}$, and L_e was demonstrated in [8] using TCAD simulation for parallel-connected IGBT devices. The unequal R_G results in a significant current imbalance. Further, $t_{d,off}$ and L_e produce significant current imbalance. In [8], the impact of the unequal R_G demonstrated during turn-on results in a severe current unbalance; however, the impact of the unequal L_e demonstrated during turn-on does not produce a significant current imbalance.

The current mismatch phenomenon during turn-off is mentioned in [32] corresponding to fulfillment of three conditions, given as follows: the individual gate resistances are used for the parallel-connected field-stop IGBTs, V_{GE} values are near $V_{G,th}$, and IGBT reaches the field-stop layer before reaching the DC link voltage, in addition to the occurrence of a self-turn-off process and parasitic turn-on effect before reaching the DC link voltage. The DC link influence is mentioned in [26], in which the current redistribution during turn-off stops as soon as the voltage across the collector-emitter (V_{CE}) regains the DC link voltage. A similar kind of mechanism was also described for a single IGBT case as a negative gate capacitance effect in [25].

The reason for the turn-off current imbalance due to gate-driving parameters is the occurrence of the distinctive V_{CE} slope and current redistribution among the paralleled IGBT devices [8,19,31]. The current imbalance phenomenon during turn-off corresponding to unequal V_{CE} for parallel-connected devices is discussed extensively in [26]. During turn-off of the devices, V_{GE} reaches the Miller plateau and V_{CE} rises significantly. However, different slopes, together with unequal stray collector inductance (L_C) and/or emitter inductance (L_E), lead to the current redistribution between the parallel-connected power devices [8,19]. This results in a serious cumulative effect as the redistribution of current affects the V_{GE} of IGBTs, which further leads to a combined cumulative effect, resulting in a change in V_{CE} slopes [19].

V_{GE} impacts are discussed for dynamic current unbalancing and static current unbalancing in [11,14]. The difference in V_{GE} of the parallel-connected devices results in the unequal static current sharing [11] and unequal dynamic current sharing during turn-on [14]. The difference of 0.5 V for V_{GE} is used in [14] to demonstrate the effect during turn-on; however, there is no significant impact on current sharing during turn-off.

2.3. System Layout and Interconnections

The stray inductance and resistance due to the load connection layout and parallel device interconnection layout can cause severe current imbalance. The stray emitter and collector inductance, (L_E, L_{cE}) and (L_C, L_{cC}), respectively, are almost unaffected by the frequency; however, the stray resistance (R_{cC}, R_{cE}) significantly increases corresponding to frequency due to the skin and proximity effects occurring in the conductors [33]. Therefore, the stray resistance and inductance have a dominant effect on current imbalance during dynamic current sharing among the parallel-connected power devices. Furthermore, the stray resistance impacts the current imbalance during static current sharing. It is mentioned that the significant changes in R_{cC}, R_{cE} have a major impact on current imbalance during switching turn-on and, as a result, at higher operating frequencies, the total power loss increases significantly [33].

The effect of L_E and L_C is thoroughly investigated in [8,26] during dynamic current sharing. The current unbalancing demonstrated for two parallel-connected devices considering unequal L_E and L_C is examined in [8]; a non-identical current slope during turn-on is observed because of the unequal displacement current through gate oxide. The difference in L_C has a significantly dominant effect compared to L_E during turn-on; however, differences in unequal L_E and L_C are not mentioned quantitatively in [8]. In [19], the current unbalancing is demonstrated due to the difference in L_C during turn-off, and it is mentioned that the unequal L_E values have the same impact on the current redistribution. However, the study in [26] also includes the busbar inductance and unequal R_G condition.

In [31], the impact of L_E is elucidated considering the influence on the gate current path with equal R_G during turn-off; an increase in L_E consequently increases $t_{d,off}$. The

effect of L_C is also demonstrated and $t_{d,off}$ increases corresponding to the increase in L_C, and a current redistribution occurs as mentioned in [19]. However, as discussed in [31], current redistribution, and consequently current imbalance, is improved with the higher L_C value because of the slower current redistribution.

In [25], three different gate-driving strategies (shown in Figure 5) are compared considering a common gate driver with a common emitter, an individual gate driver with independent driving, and an individual gate driver with a common auxiliary emitter for turn-on and turn-off conditions. This results in a different gate-driving layout. This demonstrates that a single driver/common emitter has almost the same performance as individual gate driving with an auxiliary common emitter and individual gate driving with independent driving, which lead to static current unbalance. The effect of a common auxiliary emitter considering $L_e >> L_E$ is also demonstrated in [31], which confirms that a common auxiliary emitter configuration helps improve the current imbalance compared to a common emitter configuration. This demonstrates that a single gate driver with a common auxiliary emitter has better current balancing during turn-off compared to the common gate driver with a common mode inductance. Commutation path inductance (L_S) is also discussed in [31], which demonstrates the effect on the current redistribution phenomenon. This paper mentioned that there is no influence of an increase in L_S (changed from 10 nH to 90 nH) on current redistribution; however, it impacts the voltage during turn-off and results in voltage overshoot.

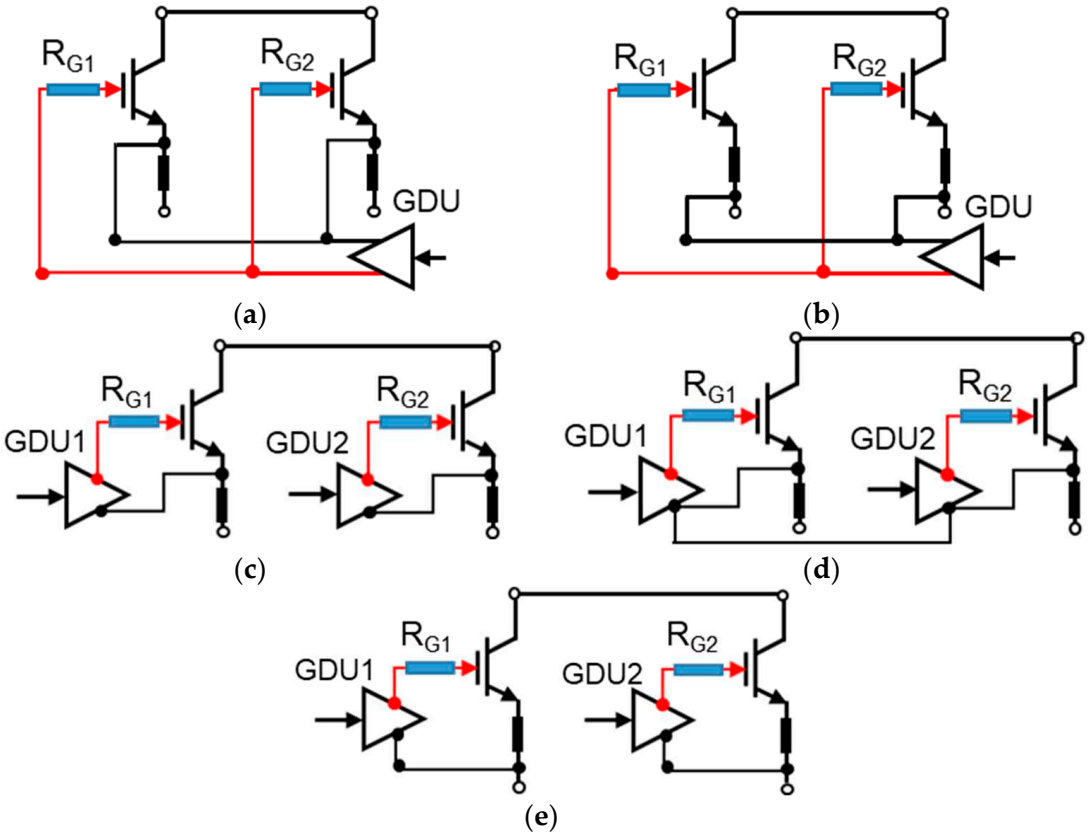

Figure 5. Layout configuration of the gate driver for parallel devices: (**a**) common auxiliary emitter CGD; (**b**) common emitter CGD; (**c**) independent auxiliary emitter IGD; (**d**) common auxiliary emitter IGD; (**e**) common emitter IGD.

The system parameters for the parallel-connected IGBT devices considering co-relation factors of device characteristics, such as transfer characteristics, output characteristics, and switching characteristics, are summarized in Table 1. The summary of related references corresponding to system parameters is also given in Table 1.

Table 1. Summary of parallel-connected IGBT system parameters.

System Parameters	Co-Relating Factors	References
Threshold voltage ($V_{G,th}$)	Gate oxide thickness, transfer characteristics, dynamic current sharing	[11,14,24]
On-state saturation voltage ($V_{CE,sat}$)/on-state resistance ($R_{DS,on}$)	Gate oxide thickness, p-base doping, output characteristic, static current sharing, dynamic current sharing	[11,14,24,25]
Parasitic capacitances	Input capacitance, output capacitance, switching characteristics, Miller region, dynamic current sharing, current redistribution phenomenon	[26,27,32]
Rate of change in current (di/dt) and voltage (dv/dt)	Switching characteristics, dynamic current sharing	[25]
Gate resistance (R_G)	Switching characteristics, dynamic current sharing, current redistribution phenomenon	[8,9,16,28–31]
Gate loop emitter inductance (L_e)	Switching characteristics, dynamic current sharing	[8,18–21]
Gate-emitter voltage (V_{GE})	static current sharing	[18–21,26,31]
Gate signal propagation delay ($t_{d,on}$; $t_{d,off}$)	Switching characteristics, dynamic current sharing	[8,18–21]
Stray emitter and collector inductance (L_E, L_{cE}) and (L_C, L_{cC})	Switching characteristics, dynamic current sharing, current redistribution phenomenon	[25,26,31,33]
Stray resistance (R_{cC}, R_{cE})	Switching characteristics, dynamic as well as static current sharing	[33]
Commutation path inductance (L_S)	Dynamic current sharing	[31]

3. Gate-Driving Techniques

Active and passive methods, as shown in Figure 6, are adopted to minimize the current unbalancing or optimize the current sharing amongst the parallel-connected power devices. This is required considering the maximum junction temperature of a particular chip to retain thermal stability and avoid thermal runway, and to ensure the operation of the parallel-connected devices within SOA corresponding to the SOA limit of the devices. In a parallel-connected system, if a device frequently experiences a higher temperature swing and operation near the SOA limit, the device will experience accelerated aging and lifetime issues [16].

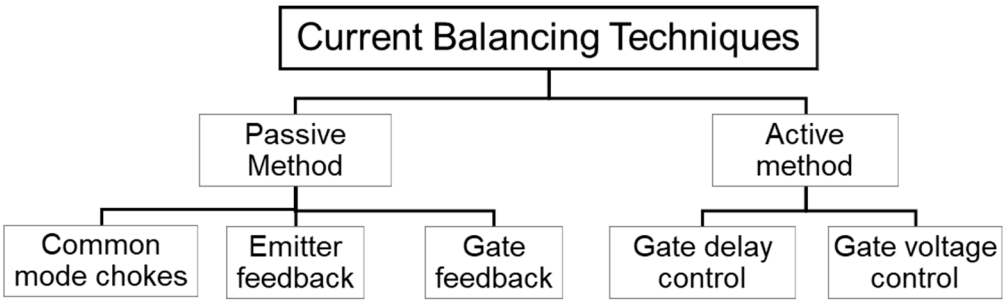

Figure 6. Current-balancing techniques of the parallel-connected IGBT power devices.

One conventional approach to achieving the operating criterion considering thermal stability and the SOA limit is derating the chips/power modules [16]. This method is the easiest and does not require sophisticated or complex gate-driving techniques. In many cases, the device manufacturers provide the application note for an analytical explanation of the derating factors regarding the parallel-connected modules. The application notes [22,23,34–36] of different manufacturers have detailed information regarding the paralleling requirement and derating factors. However, derating the chips/modules is not a current-balancing technique; therefore, the parallel system capability cannot be exploited in terms of system performance, system stability, or cost. The analysis of derating factors is a critical and

tedious procedure in the evaluation of the appropriate derating factor considering static sharing, dynamic sharing, thermal stability, and the SOA limit based on various influential factors and parameters [37].

3.1. Gate-Driving Topologies for Parallel-Connected Power Devices

A general gate-driving strategy is discussed in [9] in a study of the impact of corresponding gate-driving strategies on the paralleling of IGBT devices. The gate-driving strategies are categorized as direct gate driving, isolated gate driving, passive adapter board driving, and active adapter board driving. A schematic diagram of gate-driving techniques discussed in [9] is represented in Figure 7. As summarized in [9], direct gate driving, and passive adaptor board driving are low-cost and low complexity implementations and are highly sensitive to layout/wire length and emitter loop current. Active adapter boards have a low cost with medium complexity for implementation, have better emitter loop current performance, and are less sensitive to layout/wire length. Finally, the isolated driver has high cost and complexity, is less sensitive to layout/wire length, and is best for emitter loop current response.

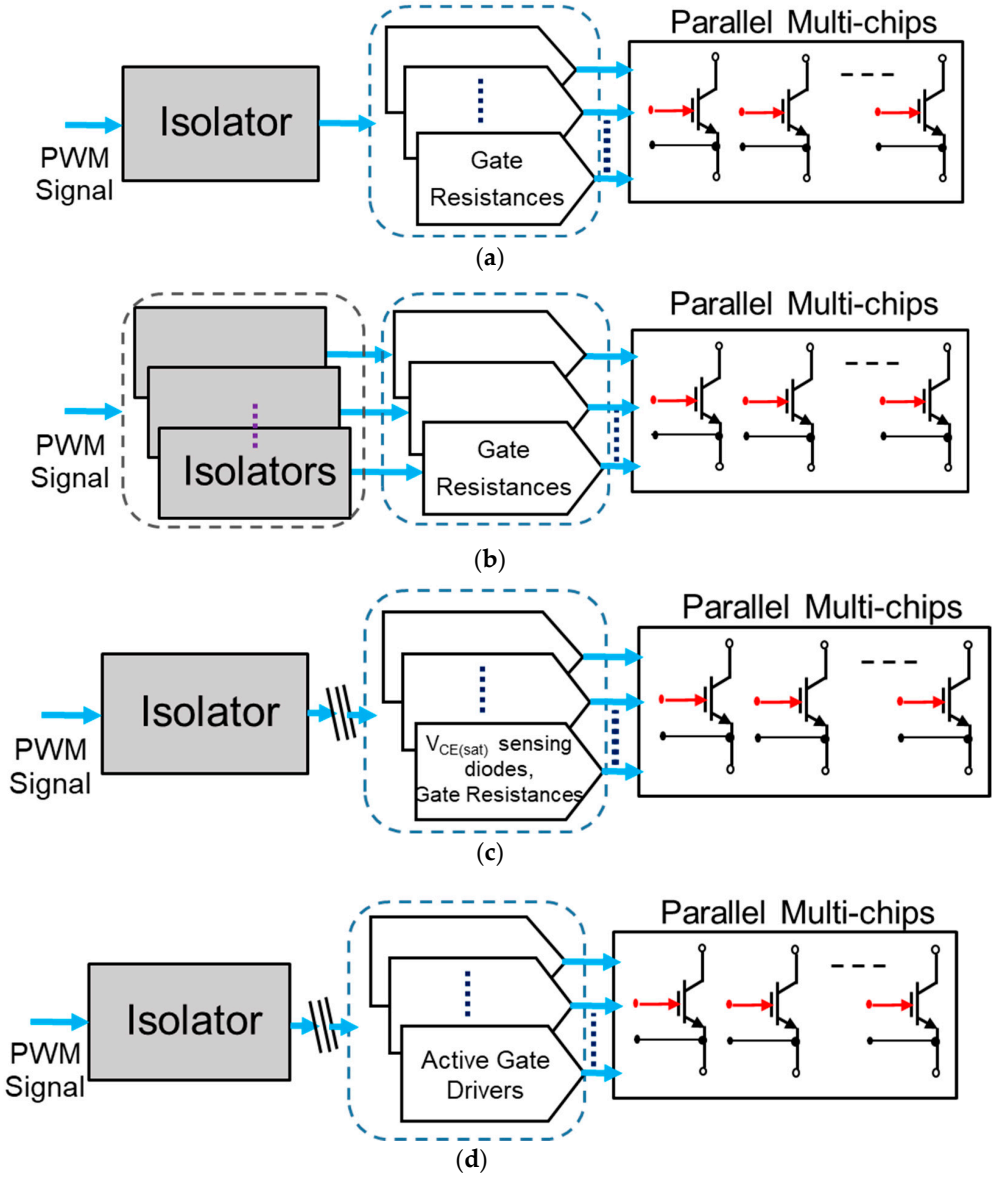

Figure 7. Gate-driving topologies for parallel devices: (**a**) direct gate driving; (**b**) isolated direct gate driving; (**c**) passive adapter board driving; (**d**) active adapter board driving.

3.2. Passive Gate-Driving Technique for Current Imbalance

Passive gate-driving techniques are a lucrative option to achieve improved current sharing for parallel-connected power devices. A detailed investigation and study were performed in [8] considering the current imbalance cause and effect, as well as the impact of passive measures on the corresponding current imbalances. The passive measure technique is categorized in three parts, as shown in Figure 8: the common mode choke technique (without feedback), emitter feedback, and gate current feedback technique.

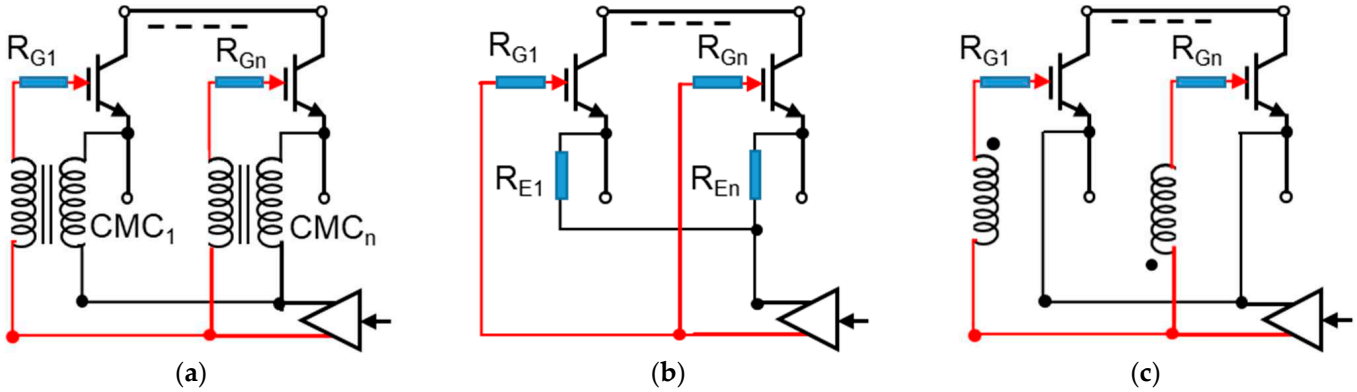

Figure 8. Schematic diagram of passive gate-driving technique for parallel-connected power devices: (**a**) common mode chokes; (**b**) emitter feedback through common auxiliary emitter; and (**c**) gate current feedback using differential mode chokes.

3.2.1. Common Mode Chokes

The common mode chokes are investigated in [9] using passive adapter board gate driving and the CGD technique under the conditions of an asymmetric gate drive length and asymmetric busbar configuration. The common mode choke significantly worsens the dynamic current imbalance for an asymmetric gate drive length. However, the common mode choke improves the dynamic current imbalance for an asymmetric busbar configuration.

The impact of common mode (CM) chokes on the CGD technique is discussed in [14], and is described as a patented technology from ABB. The current sharing is demonstrated for the two parallel-connected devices considering unequal L_E values. A similar test condition without CM chokes results in current imbalance during turn-on and during static current sharing; there is almost no impact during turn-off. The inclusion of CM chokes eliminates the current unbalancing during turn-on and in static conditions.

3.2.2. Emitter Feedback

The effect of emitter feedback caused by the emitter inductance through a common auxiliary emitter is investigated in [9] using passive adapter board gate driving under the conditions of an asymmetric gate drive length and asymmetric busbar configuration. The emitter feedback provides improved dynamic current sharing with an asymmetric gate drive length, as well as an asymmetric busbar configuration. However, emitter feedback is less effective in the case of the asymmetric busbar configuration compared to an asymmetric gate drive length.

Similar emitter feedback is investigated in detail in [8] considering the difference in gate resistors, the difference in turn-off delay times, the difference in gate inductances, and the combined effect of the difference in emitter inductance and the difference in turn-off delay times during turn-off for two parallel-connected power devices with a CGD configuration. This also considers the difference in turn-off delay times due to gate-emitter capacitance (C_{GE}) and due to $V_{G,th}$. The emitter feedback technique can reduce current imbalances for all the test conditions.

Furthermore, emitter feedback is investigated for turn-on conditions considering the difference in gate resistors, C_{GE}, $V_{G,th}$, L_e, L_E, and L_C. The current imbalance is improved

for the turn-on condition for all the cases except the difference in the emitter inductance condition. The current imbalance worsens in the case of the difference in the emitter inductance condition for the emitter feedback.

3.2.3. Differential Choke-Based Gate Feedback

The effect of differential choke-based gate feedback is assessed in [8]. This considers the turn-off case with a difference in turn-off delay times, a difference in gate inductances, and the combined effect of a difference in emitter inductance and a difference in turn-off delay times; a difference in the turn-off delay times due to C_{GE} and $V_{G,th}$; and the turn-on case with a difference in gate resistors, C_{GE}, $V_{G,th}$, L_e, L_E, and L_C. In the turn-off case, the gate feedback method can reduce current imbalances, except the difference in turn-off delay times due to C_{GE}, and the current imbalance worsens for the case of C_{GE}. In the case of turn-on, the current imbalance is reduced for the difference in gate resistors and gate inductances; however, the current imbalance almost remains the same for L_E and $V_{G,th}$; the current imbalance worsens for the case of L_C and C_{GE}.

The comparative performance of the passive gate driving techniques is summarized in Table 2. The performance is summarized considering the study and investigation discussed in [8,9,14].

Table 2. Comparison of common mode chokes, emitter, and gate feedbacks passive methods.

Imbalance Parameters	Transient	Common Mode Chokes	Emitter Feedback	Gate Feedback
Asymmetric Gate drive length (L_G)	on	Increased	Reduced	Reduced
	off	Increased	Reduced	Reduced
Asymmetric bus bar length (L_S)	on	Reduced	Reduced	
	off	Reduced	No change	
Gate Resistance (R_G)	on	Increased	Reduced	Reduced
	off	Increased	Reduced	Reduced
Threshold voltage ($V_{G,th}$)	on		Reduced	No change
	off		Reduced	Reduced
Gate-emitter capacitance (C_{GE})	on		Reduced	Increased
	off		Reduced	Increased
Emitter Inductance (L_E)	on	Reduced	increased	No change
	off		reduced	

3.3. Active Gate-Driving Control Techniques

The active gate-driving control techniques are employed to minimize the current imbalance and/or to achieve optimized current sharing, as shown in Figure 9 for parallel collected devices/modules. The current-balancing techniques are classified in [38] as derating, active gate control, and impedance balancing. Further, active gate-driving control is categorized as gate delay control and the average current method. The derating method is a means of maintaining the thermal stability and SOA operation of the parallel-connected chips/modules by reducing the rated operating limit of the chips/modules; this method is not capable of providing current balancing or improving current imbalance. The active gate control method can be an appropriate solution; however, implementation complexity is an associated issue. The active gate control methods are summarized in Figure 8 using a schematic representation of the techniques.

3.3.1. Gate Delay Control

The gate delay control technique is presented in [39] for the dynamic current balancing during turn-on and turn-off. The results are demonstrated for four parallel connected

IGBT devices through gate delay control, which achieves improved current sharing. The operating principle is presented for the gate delay control based on calculation of the current error using central signal processing or a master–slave control method.

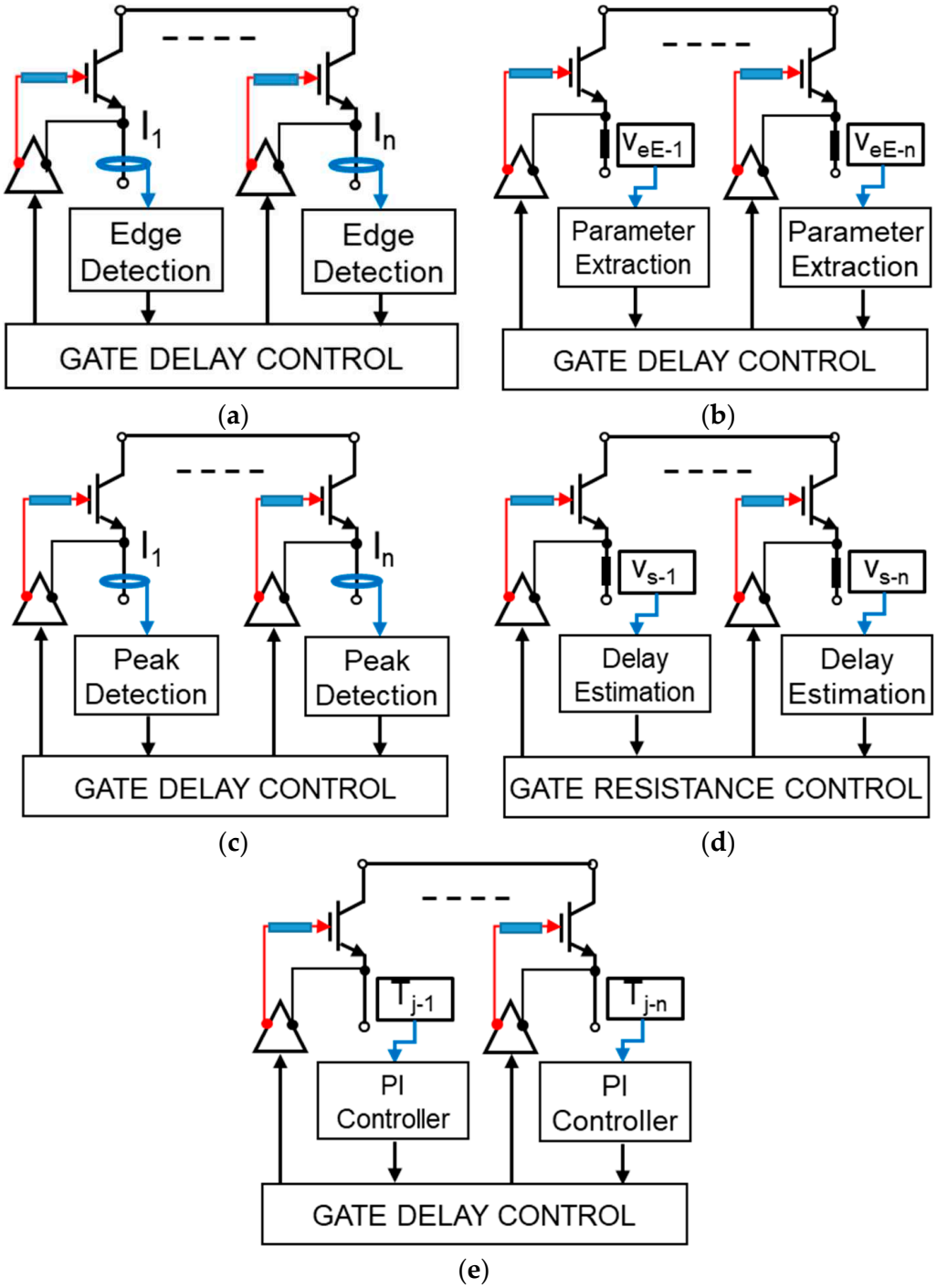

Figure 9. Schematic diagram of active gate-driving control techniques for dynamic current balancing of parallel−connected power devices: (**a**) current edge detection; (**b**) auxiliary emitter and emitter voltage measurement; (**c**) current peak detection; (**d**) TSEP-based junction temperature measurement; (**e**) gate voltage and delay control using dynamic gate resistance.

The active gate delay control is proposed and discussed in [40] based on the edge detection of currents with peak current monitoring of parallel-connected power devices. The rise-and-fall time controller is based on the detected rising and falling edges, and gate

signals are manipulated to provide the required delay and to achieve current balancing. A distributed non-centralized control is presented in [41] based on the edge detection technique presented in [40]; to implement the distributed non-centralized control, the master–slave technique and daisy chain technique are used to determine the appropriate delay of the gate signals and are finally experimentally evaluated for four parallel-connected IGBT power devices.

The delay time compensation principle is presented in [42–45] considering the voltage measurement between the emitter and auxiliary emitter (V_{eE}). The measurement of V_{eE} corresponding to individual devices connected in parallel is further used for the extraction of delay time information. This delay time information is further used for the compensation algorithm to determine the appropriate delay time for the gate signal corresponding to individual devices and generation of the manipulated gate signal. The method is examined for the two parallel-connected power devices in [42] to achieve active current balancing and evaluated for the three parallel-connected devices; in addition, the half bridge inverter configuration is examined in [45]. This demonstrates the balanced current sharing during turn-off after employing this technique, and improved current imbalance during turn-on as well.

The dynamic current peak detection-based active delay compensation method is presented in [46]. The peak current of the parallel-connected devices is detected, and active gate delay compensation control is demonstrated for two IGBT devices using fully digital feedback control in FPGA. The efficacy of the method is demonstrated for four parallel connected IGBT devices in [47] with a current imbalance limit to achieve current optimization. Further, this dynamic peak current detection implementation is demonstrated using a PCB Rogowski current sensor in [48]. This approach is suitable for system miniaturization considering the characteristic of the PCB Rogowski current sensor, providing current measurement in the form of peak overshoots for parallel-connected power devices. The appropriateness of this method is demonstrated for four parallel connected IGBT devices, and current measurement accuracy is verified using a Pearson current probe.

Another active gate delay control technique is presented in [49] using the junction temperature measurement of the power devices. The online junction temperature of corresponding devices is measured using the thermo-sensitive electric parameter (TSEP) method, which is integrated with a gate-driving unit to estimate the junction temperature of the individual devices. The internal gate resistance is a TSEP considering its dependence on the chip temperature. However, an accurate calibration mechanism is required to translate the voltage measurement across the internal gate resistor into temperature estimation and based on the temperature estimation of the devices, gate signals are manipulated to incorporate an appropriate delay and to equalize the junction temperature of the parallel-connected devices.

3.3.2. Gate Voltage Control

A gate voltage control method is mentioned in [39] for the static current balancing of the parallel IGBT devices considering the negative temperature coefficient. The appropriate adjustment of the gate voltage can provide improved static current sharing. The method of gate voltage control based on the current averaging method is presented in [50] and balanced static current sharing is demonstrated for two parallel connected IGBTs. Furthermore, the gate voltage control method based on the current average calculation and current cross-reference is presented in [12], and results are demonstrated for two independent parallel-connected transistors and for the boost converter implementation.

The device current slope can be controlled via dynamic gate-emitter voltage control of the corresponding device [51] and dynamic current balancing can be realized. The dynamic adjustment of V_{GE} can be realized through dynamic R_G control. The dynamic R_G control is presented and implemented in [52,53] for parallel-connected IGBTs to realize dynamic V_{GE} adjustment. Furthermore, turn-on and turn-off delay time parameters can also be controlled by dynamic resistance control.

4. Discussion

The various components that influence the performance of the parallel-connected power device system are summarized in Figure 3. The power semiconductor device characteristics, diode characteristics, gate driver configuration, and gate driver layout are one set of influences, and DC busbar layout, AC busbar layout, gate connection layout, and device cooling are another set, which, in combination, can cause severe issues in terms of reliability, thermal stability/thermal runaway, unwanted oscillations, and violation of safe operating area (SOA) operation.

4.1. Influence of Parameters and Passive Gate Control

The influence of parameters is thoroughly studied and investigated in Section 2. The turn-on and turn-off phenomena are significantly different for the IGBT devices; therefore, the effects of parameters and gate control techniques may possess unique impacts. The case of different emitter inductances for dynamic current imbalance is improved during turn-off via the passive gate control technique of emitter feedback; however, the current imbalance worsens during turn-on. Similarly, emitter feedback for an asymmetric feedback busbar length can improve current imbalance during turn-on but has no impact during turn-off. This ultimately implies that a single perfect solution is not possible using the passive gate control technique; however, emitter feedback can still be the preferred choice considering its impact on a higher number of parameters that influence unbalancing compared to other passive gate control techniques. The passive feedback methods discussed in Section 3.2 can mainly improve or minimize the current imbalance rather than realizing current balancing or optimized current sharing under most of the unbalanced conditions.

The condition and criterion for a single IGBT are discussed in [54] using a proposed signal flow graph model that can be vital for parallel-connected IGBT system design. It establishes a relationship between critical parameters: emitter inductance, gate inductance, collector inductance, and gate resistance. If emitter inductance is zero, the critical gate resistance required increases with the increase in gate inductance. Furthermore, if gate inductance is constant, critical gate resistance decreases as emitter inductance increases.

The circuit stability depends on the emitter inductance, and a small emitter inductance destabilizes the circuit, considering that an increase in emitter inductance is preferable to an increase in collector inductance, which can minimize the possibility of oscillation; gate inductance should be as small as possible to minimize the oscillation [54]. The effect of emitter inductance in [31] for turn-off provides confirmation considering 0 nH, 5 nH, 10 nH, 15 nH, and 20 nH cases, and demonstrates that the current redistribution phenomenon is almost absent for the 20 nH case compared to the 0 nH case, which has dominant current redistribution due to the self-turn-off of the IGBT. Therefore, the design criteria in [54] would be significant, as the emitter inductance, gate inductance, collector inductance, and gate resistance are the crucial parameters for current imbalance, as well as system oscillation. Nevertheless, these criteria must be exploited for parallel system design, which requires overall system parameter design optimization.

The influence of the device parameters considering the IGBT, as well as the anti-parallel diode, is analyzed in [55] for paralleling of specific types of module packages. This study targets the most influential parameters for the parallel-connected system and defines the relationship for reverse recovery energy (ΔE_{recov}) with the forward voltage of the diode (ΔV_F), turn-on energy (ΔE_{on}) with the forward voltage of the diode (ΔV_F) and threshold voltage ($V_{G,th}$), and turn-off energy (ΔE_{off}) with the collector-emitter voltage ($\Delta V_{CE,sat}$) and turn-off delay time (Δt_{dvoff}). This demonstrates that the linear relation between current unbalancing corresponding to Δt_{dvoff} has an effect during turn-off, a dominant $V_{G,th}$ effect during turn-on, a dominant V_F effect during reverse recovery and turn-on, and a $V_{CE,sat}$ dominant effect during turn-off, which can lead to different slopes of V_{CE} during turn-off, and ultimately lead to current redistribution phenonmenon. The relationships are mathematically defined as:

$$\Delta E_{recov} = f(\Delta V_F)$$
$$\Delta E_{on} = f(\Delta V_F, \Delta V_P)$$
$$\Delta E_{on} = f\left(\Delta V_{CE}, \Delta t_{dvoff}\right)$$

4.2. Gate-Driving Techniques and Active Gate Control

The gate-driving methods discussed in Section 3.1 and active current-balancing technique discussed in Section 3.3 for parallel-connected power semiconductor devices are summarized in Figures 9 and 10. The gate-driving technique is categorized fundamentally as direct driving, common gate driving, or individual gate driving. The simplest way of driving parallel-connected power devices is via direct gate driving, which is subcategorized into separate gate resistance, isolated separate gate resistance, and passive adapter board driving. Further, common gate driving and individual gate driving (which is a kind of active adapter board driving) are subdivided into separate auxiliary emitter driving and common auxiliary emitter driving. The individual gate driver can also be subcategorized as isolated gate driving. The common auxiliary emitter provides an additional possibility to incorporate the passive emitter feedback technique.

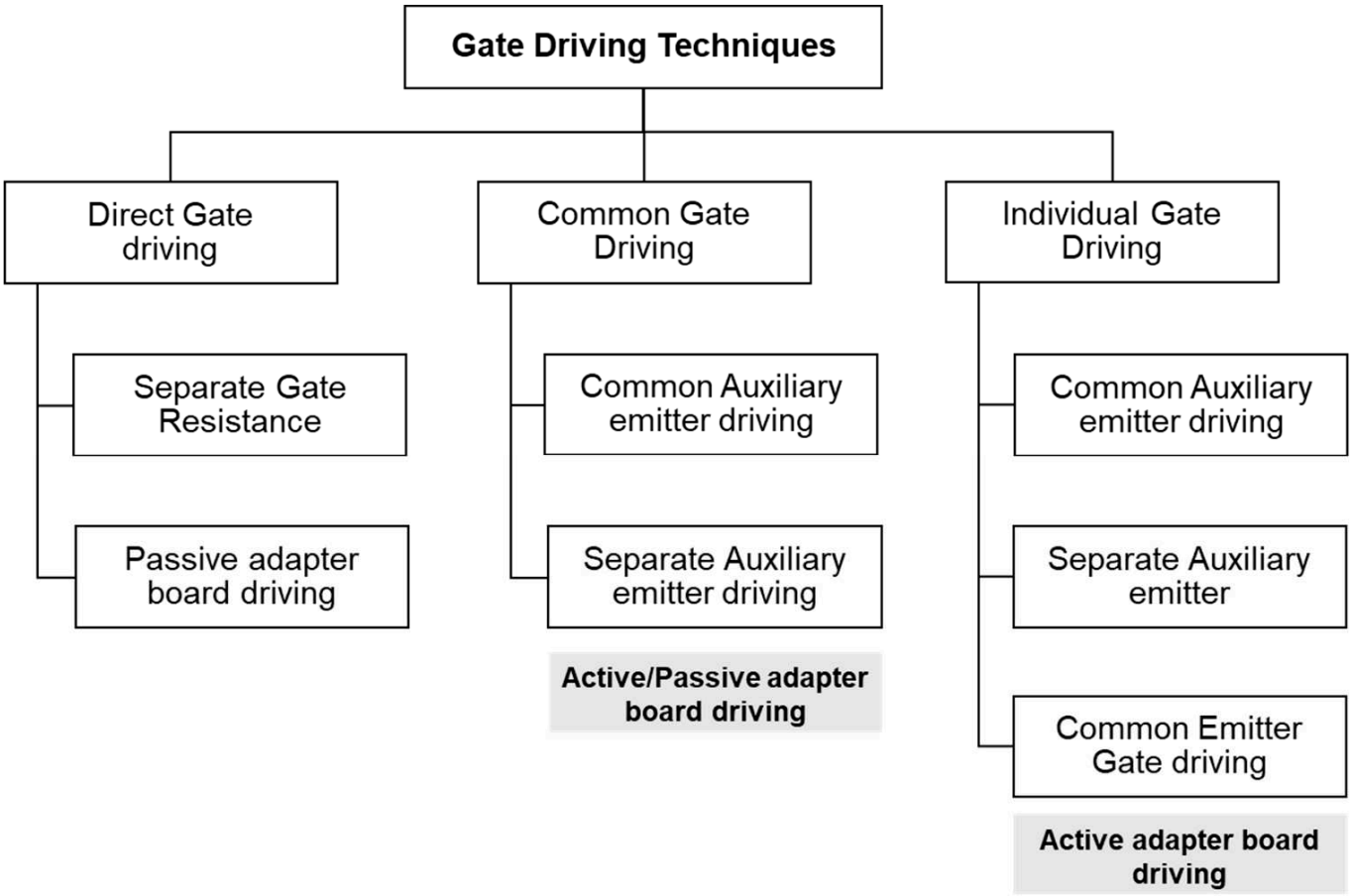

Figure 10. Gate-driving techniques for parallel-connected power devices.

The active gate control current-balancing techniques are mainly realized using the individual gate-driving method to assist corresponding power devices with gate signal adjustment capabilities. Most of the active gate controls employ the delay adjustment technique, which is the simplest to implement; however, computation and decisions for gate delay can be complex depending on the implementation methodology. In addition, the individual gate-driving implementation is costly compared to other approaches as it

requires separate active gate drivers for each device. Isolated individual gate-driving is the costliest means of implementation but provides maximum flexibility for independent adjustment. The gate voltage control technique provides static current balancing, and dynamic gate voltage control has the capability to adjust the device current slope as well as the gate delay. Dynamic gate voltage control has higher complexity compared to other techniques considering the computation and determination of the pattern for the selection of dynamic gate resistance for the implementation.

4.3. Reliability, Derating, and Stability Factors

The current imbalance in the parallel-connected system enforces the SOA operational and thermal operational limits considering the system reliability. The worst-case scenario of the maximum possible current imbalance must be considered to determine the derating factors corresponding to SOA. Furthermore, the maximum junction temperature operation of a single chip should be considered to determine the thermal derating. The complexity of these factors increases with the increased number of parallel modules/discrete devices/chips. Derating criteria are discussed in [55] based on the relationship's dominant parameter's impact on current balancing to achieve operation within the SOA limit.

Current imbalance impacts the junction temperature and, considering this, the reliability of parallel-connected switches is discussed in [56] using the Markov-based reliability model. The mean time to failure criterion is considered to analyze the failure possibility under different current sharing and operating conditions. The operating conditions are parallel-connected switches with redundant operation and parallel-connected switches with modular operation. Furthermore, the short-circuit performance and reliability of parallel-connected devices is indispensable; it is discussed for the parallel SiC MOSFET and Si-IGBT in [57]. The performance is studied considering different device parameters, and non-identical $V_{G,th}$ parameter variation is the dominant factor under the short-circuit condition.

The derating factor for SOA operation and the thermal operation limit are mentioned in [14]. The cooling of the devices is another aspect, and homogenous cooling of the paralleled device/module system is a critical factor to realize homogenous sharing of the current and to maintain the junction temperature within the operating limit, as well as to ensure it is closely matched. It has been mentioned that the current imbalance can be up to 50% due to $t_{d,off}$ and t_{dvoff} during turn-off; therefore, to achieve operation within SOA, the turn-off current must be reduced by 50%. Further, the switching losses and on-state losses must be critically analyzed corresponding to the unequal current sharing to achieve thermal stability by employing thermal derating based on the junction temperature profile. This factor can be more critical for the full-load operating conditions and high-switching-frequency operations.

The paralleling problems are discussed in [16], which mentions the stability considerations as part of the fundamentals for the parallel-connected IGBT system. The system stability depends on the generated power loss and dissipated power losses; that is, the rate of generated power loss should be less than or equal to the dissipative power, i.e., $(\partial P_G/\partial T) \leq (\partial P_D/\partial T)$. This is important to achieve a stable and settled junction temperature corresponding to an increase in generated power losses. This must be satisfied for a single device, as well as an overall paralleled system, to realize and maintain system stability, along with individual device stability, to avoid thermal runway and violation of SOA operation. Furthermore, it is also worth noting that frequent operation with high temperature swings and operation near the SOA limit can cause accelerated aging and lifetime reduction.

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