A Low Area-Overhead and Low Delay Triple-Node-Upset Self-Recoverable Design Based on Stacked Transistors

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Abstract—**With the aggressive decrease of the feature size of transistors, single event triple-node-upset (TNU) induced by charge sharing has become a significant reliability problem. A TNU self-recovery latch called LORD-TNU based on N-type stacked transistors is proposed in this paper. It has a smaller number of transistors and a lower delay than four existing TNU self-recovery latches. Simulation results show that compared with four existing TNU hardened latches, the proposed LORD-TNU latch reduces area overhead by 49.76%, power consumption by 56.07%, delay by 40.17%, and the power-delay-product (PDP) by 72.56% on average, respectively. PVT and Monte Carlo results show that the proposed LORD-TNU latch remains stable with the variation in process corner, supply voltage, and temperature.**

Index Terms—**Circuit reliability, radiation hardening, single-event-upset, stacked transistors, triple-node-upset.**

I. INTRODUCTION

WITH the rapid development of integrated circuits (ICs), the feature size of transistors continues to decrease, and parasitic capacitances and power supply voltages of the circuit decrease sharply [1]. Therefore, ICs become more susceptible to soft errors caused by the incidence of high-energy particles such as neutrons, protons, heavy ions, and so on [2]. When a sensitive node inside a circuit is struck by high-energy particles, the charge it carries is collected by the sensitive node [3]. When the charge surpasses the critical charge of the node, the logical value of the node experiences an upset, leading to a single-event upset (SEU) [4]. If charges are collected by a single sensitive node in a latch, causing the logic value of a single node to upset, it is called an single-node-upset (SNU). However, in recent years, researchers have discovered that high-energy particles can also induce a multiple-node-upset (MNU) due to charge sharing [5], including a double-node-upset (DNU) or even a triple-node-unset (TNU) [6]-[7]. In safety-critical applications (particularly in the harsh radiation environment), TNUs have emerged as a serious concern for circuit designers and manufacturers working with advanced CMOS technology [8]-[10].

Currently, radiation-hardening-by-design (RHBD) is the most effective technique for addressing TNUs [17]-[24]. The RHBD technique is widely adopted without altering the design flow. Some common hardened elements are shown in Fig. 1. From Fig. 1(a) to Fig. 1(f), they are dual-input inverter [11], source-drain cross-coupled element (CCE) [24], Schmitt Trigger (ST) [12], C-Element (CE) [13], input-split C-Element (CPN) [20], and Dual-Interlocked-storage-Cell (DICE) [14]. Using the CE as an example to illustrate its working principle, the output value is the inverse of the input value when the two inputs are identical. However, when the two inputs differ, the output value enters a high-impedance state, temporarily maintaining the original logic value unchanged.

Various hardened latches [21]-[24] designed to recover TNUs have been introduced, enhancing their reliability against MNUs. These latches still encounter certain limitations. The LRLPT latch [21] has high power consumption and high delay due to the formation of multiple feedback loops during the transparent period. The LCTNUCR latch [22] has a large quantity of area overhead because of the use of multiple four-input CEs. The TNURL latch [23] also causes a large area overhead due to the use of multiple SIM structures. The LCTNURL latch [24] achieves the TNU self-recovery and also results in a very high overhead. Due to these problems, the proposed LORD-TNU latch in this paper can achieve TNU self-recovery using a smaller number of transistors than the existing four TNU self-recovery latches. Its delay is relatively low due to the high-speed path.

The rest of the paper is organized as follows. Section II introduces the radiation upset mechanism and the existing latch structures. The proposed latch is introduced in section III. Section IV performs simulation results of the proposed latch. Summarizes are drawn in Section V.

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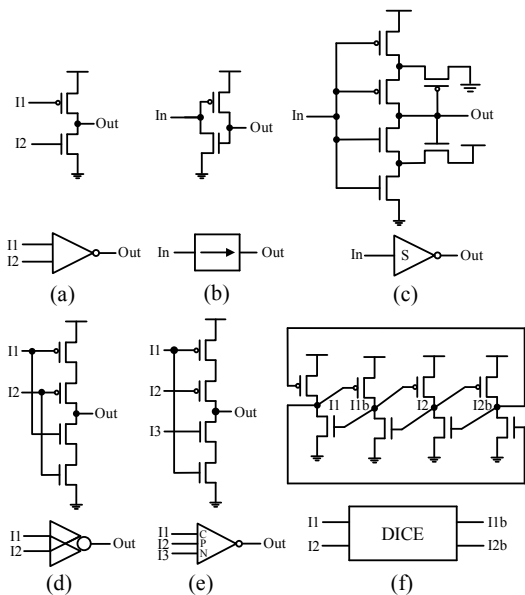
Fig. 1. The common hardened elements. (a) Dual-input inverter. (b) Source-drain cross-coupled element (CCE). (c) Schmitt-Trigger (ST). (d) C-Element (CE). (e) Input-split C-Element (CPN). (f) Dual-Interlocked-storage-Cell (DICE).
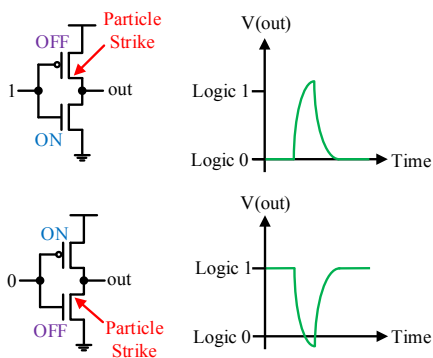

Fig. 2. Upset mechanism by using an inverter.

II. BACKGROUNDS

A. Radiation Upset Mechanism

When the energetic particles hit the sensitive region of the device, additional electron-hole pairs are generated and collected within the depletion layer due to the reverse-biased electric field. These pairs move under the influence of the reverse-biased electric field (electrons are collected only by NMOS, and holes are collected only by PMOS) [15].

Fig. 2 takes an inverter as an example to describe the process of charge collection [3], [15]-[16]. As a result of the existence of the reverse-biased electric field, the polarity of the radiation-induced transient voltage depends on the type of the affected transistor: if the affected transistor is a PMOS in the OFF-state, the storage value of the drain changes from 0 to 1 due to the collection of holes. If the affected transistor is an OFF-state NMOS, the storage value of the drain changes from 1 to 0 because of the collection of electrons.
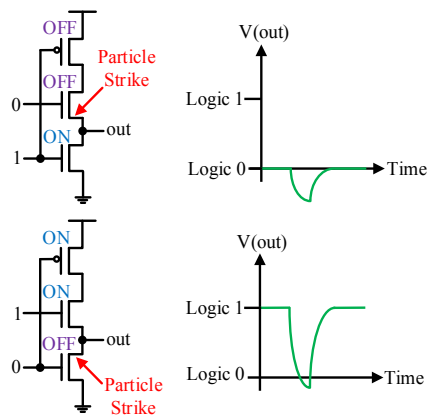

Fig. 3. Upset mechanism by using stacked transistor.

Because of the stacked transistors, the output node is completely isolated from the PMOS transistor, resulting in the output node only collecting negative charges, so only the flip from 1 to 0 is considered. When the output is 1, the flip from 1 to 0 occurs; when the output is 0, similar to having no flip (the output is 0), the voltage becomes negative because the negative charges are gathered. The flip case is illustrated in Fig. 3. This paper proposed a LORD-TNU latch that uses the stacked transistors. The drawback is that the stacked NMOS transistor results in a threshold loss. The sizes of some pull-down transistors must be changed to compensate for this penalty. (i.e., Offering a stronger pull-down driving capability).

B. Previous Works

This part will review existing hardened latches, named HITTSFL [17], TNU-Latch [18], LCTNURL [24], TNUTL [20], LRLPT [21], LCTNUCR [22], TNUHL [19], TNURL [23], as shown in Fig. 4.

The HITTSFL latch, which can tolerate TNU, is shown in Fig. 4(a). The HITTSFL latch consists of three clocked DICEs and an ST. This latch lacks a high-speed transmission path, and this triple-modular redundancy structure based on three clocked DICEs leads to current contention at Qb, resulting in greater delay overhead.

Fig. 4(b) shows the TNU-Latch latch, consisting of seven multi-input CEs and one dual-input CE. The latch delay overhead is substantial since it uses a lot of multi-input CEs, and there is not a transmission path from D to Q.

Fig. 4(c) demonstrates the structure of the LCTNURL latch. It comprises twelve interlocked three-input CEs to form a feedback loop and can achieve the self-recovery of TNU. The power consumption is quite high since there are so many complementary parts, and the area overhead is also somewhat high because so many three-input CEs are being used.

Fig. 4(d) displays the TNUTL latch, consisting of five CPNs and one dual-input CE, and can achieve TNU tolerance. The latch has the benefit of consuming little power and taking up little area, but the downside is that it has a high delay. Although there is a transmission period path from D to Q, the delay during the hold period will be larger because of the multi-stage hold module.
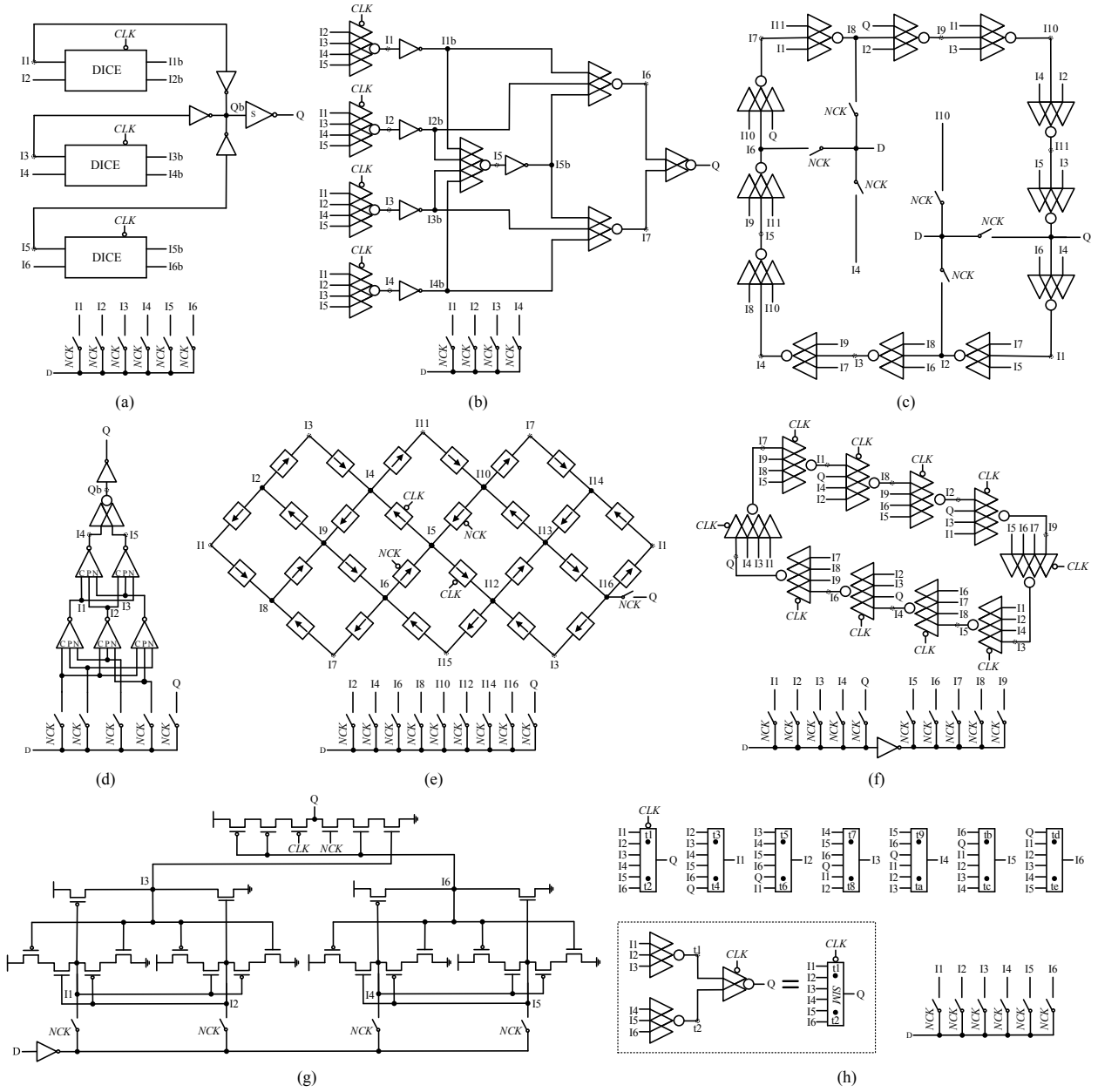
Fig. 4. Existing latches. (a) HITTSFL [17]. (b) TNU-Latch [18]. (c) LCTNURL [24]. (d) TNUTL [20]. (e) LRLPT [21]. (f) LCTNUCR [22]. (g) TNUHL [19]. (h) TNURL [23].

Fig. 4(e) shows the LRLPT latch. It is based on the CCE. The advantage of this element is that the on-state CCE can tolerate the occurrence of SEU at one end and restore the other. Multiple feedback loops cause this latch transparent period power consumption to be serious.

Fig. 4(f) demonstrates the LCTNUCR latch. This latch consists of ten clocked four-input CEs and can achieve TNU self-recovery. The use of multiple four-input CEs costs a large amount of area overhead.

Fig. 4(g) illustrates the TNUHL latch. It consists of two recovery circuits (RCs) and a clocked dual-input CE, which can achieve TNU tolerance. The advantage of the TNUHL

latch is low area and power consumption, but the delay is relatively high owing to the lack of a high-speed transmission path, and the latch cannot tolerate all TNU.

Fig. 4(h) displays the structure of the TNURL latch. The TNURL latch is composed of seven soft error intercept modules that provide feedback to each other. Each module includes two three-input CEs and one dual-input CE (one of which is a clocked CE). Consequently, the self-recoverability of the TNU latch relies on the associated overhead cost.

Due to all the problems of the high area and delay in these existing latches, a TNU self-recovery LORD-TNU latch that uses the stacked transistors is proposed in the next section.
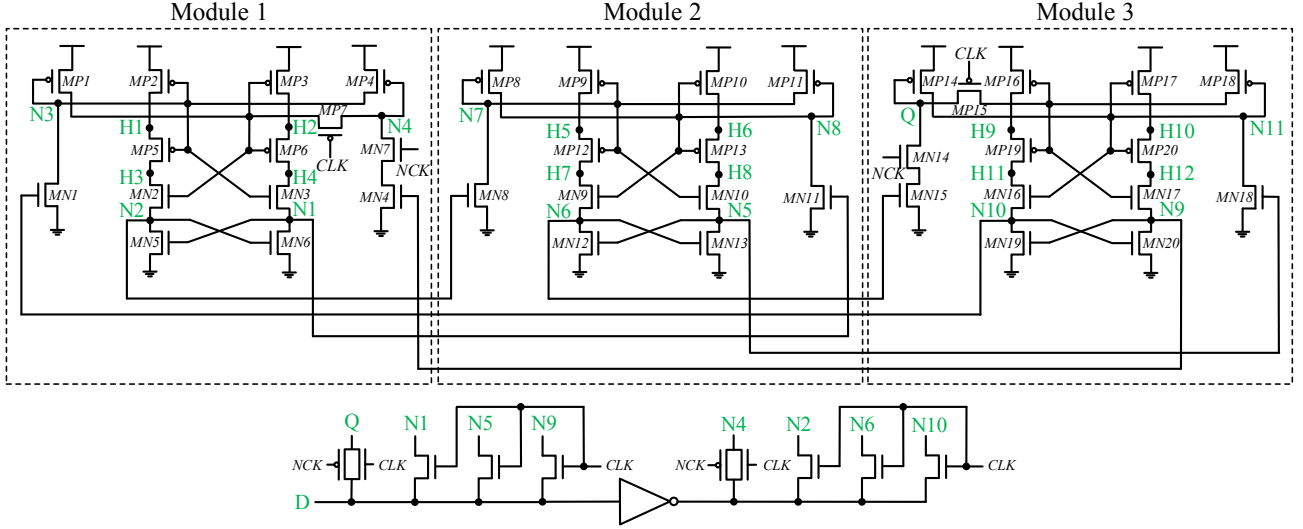
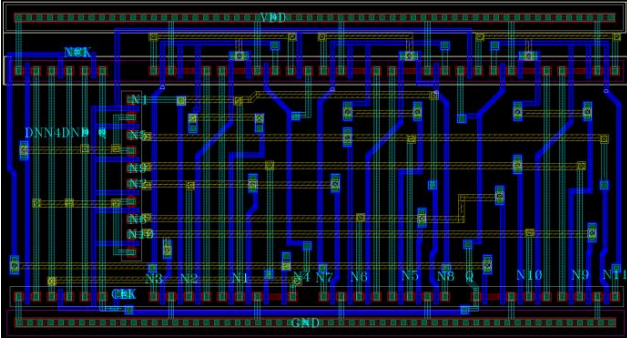Fig. 5. Schematic of the proposed LORD-TNU latch.

Fig. 6. Layout of the proposed LORD-TNU latch.

III. PROPOSED LATCH DESIGN

The proposed LORD-TNU latch shown in Fig. 5, consists of three identical modules (except for the clocked element). Fig. 6 shows the layout of the proposed LORD-TNU latch. To form a feedback loop for latching values during the hold period, the three modules are redundant to each other. D supplies values directly to the nodes N1, N5, and N9, and to nodes N2, N6, and N10 through the inverter. Nodes Q and N4 are derived through the transmission gate. The purpose of adding clocked elements to the first and third modules is to avoid the formation of a feedback loop during the transparent period. These clocked elements reduce power consumption. The schematic diagram of the clocked element to break a feedback loop is shown in Fig. 7 under D = 0 in transparent and hold mode. The case when D = 1 is equivalent to that when D = 0. Thus, there is no need for repetition.

The latch operates in transparent mode when CLK = 1, and NCK = 0. At this time, the transmission gates are turned ON, the clocked elements are turned OFF, and Q is directly driven by D. Consequently, the value of the nodes N1, N5, N9 is 0, and the value of the nodes N2, N6, N10 is 1 when D = 0. Nodes Q and N4 are directly driven by the transmission gate

with values of 0 and 1, respectively. MN6, MN13, and MN20 turn ON to strongly pull-down nodes N1, N5, and N9 to logic 0. MN1 and MN8 are turned ON. The ON-state of MN8 will pull down nodes N7 to logic 0. Nodes N7 and Q drive MP8 and MP14 to turn ON. The ON-state of MP8 and MP14 will pull nodes N8 and N11 up to 1. At this point, all nodes are initialized, and the situation at D = 0 is similar to D = 1 and will not be repeated so that the circuit can operate normally during the transparent period.

The latch operates in hold mode when CLK = 0, and NCK = 1. Currently, the transmission gates are turned OFF, and the clocked elements of module 1 and module 3 are turned ON. Module 1 (MP3, MP6, MN3, MP7, MP4, MN7, MN4), module 2 (MP10, MP13, MN10, MP11, MN11), and model 3 (MP17, MP20, MN17, MP18, MN18) are in the ON-state, forming a feedback loop for latching values. The feedback loop drives the output Q.

In the following, memory 0 is used as an example to describe the flipping case of the node. Due to the characteristics of the stacked transistors, internal nodes N2, N3, N4, N6, N7, N8, N10, N11 and the output node Q are considered. For high-impedance nodes, H1 = H3 = N2 = H5 = H7 = N6 = H9 = H11 = N10 = 1 (The corresponding transistors are in the ON-state), so H2, H4, H6, H8, H10, H12 must be considered.

First, for the case of SNU, the following four cases are considered because of the symmetrical structure of the latch.

SNU-Case 1: When node N2 is affected, the value of node N2 is flipped to 0, MN6 and MN8 are temporarily turned OFF, and other nodes are unaffected. Because MP2, MP5, and MN2 are in the ON-state, the value of node N2 can be restored.

SNU-Case 2: When the value of node N3 is flipped to 1, MP1, MP2, and MP5 are temporarily turned OFF, and MN3 is temporarily turned ON. Because node N10 is in the correct value and MN1 is in the ON-state, node N3 can be restored by node N10 driving MN1.
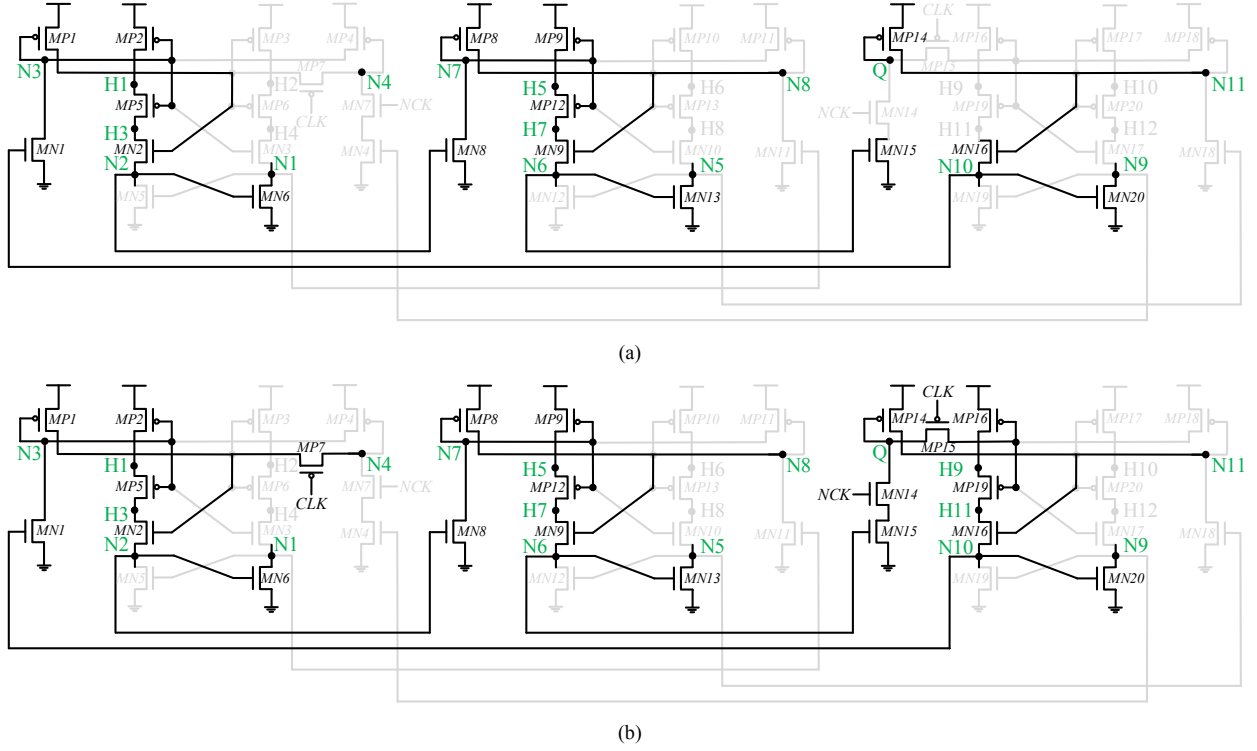
Fig. 7. Avoiding the formation process of feedback loops. (a) D = 0 in transparent mode. (b) D = 0 in hold mode.

SNU-Case 3: When the affected node is N4, its value is flipped from 1 to 0, MP3, MP4, and MP6 are temporarily turned ON, MN2 is temporarily turned OFF, and other nodes are unaffected. However, node N3 is unaffected because the transistor size of MN1 is large (provides a stronger pull-down capability), node N3 drives MP1 ON, and node N4 is restored.

SNU-Case 4: When the high-impedance node H2 (H4) is the affected node, Q has a correct latched value because the induced charge does not diffuse to other nodes. The other values are still correct.

Next, for the DNU case, consideration is given to the following two cases due to the symmetrical structure of the latch.

DNU-Case 1: When the flipped node pair comes about in the same module.

(a) When the node pair <N2, N3> is affected, the value of node N2 is flipped to 0, and node N3 is flipped to 1. MN3 is temporarily turned ON, MP1, MP2, MP5, MN6, and MN8 are temporarily turned OFF, and other nodes are unaffected. Node N10 drives MN1 to maintain the correct value of node N3, and node N3 drives MP1, MP2, and MP5 to turn ON. The wrong node value of node N2 is restored. The recovery principle of <N2, N4> is the same as that of <N2, N3>.

(b) When a double node upset occurs on N3 and N4, the value of node N3 is flipped from 0 to 1, and the value of node N4 is flipped from 1 to 0. MP1, MP2, MP5, and MN2 are temporarily turned OFF, and MP3, MP4, MP6, and MN3 are temporarily turned ON, resulting in

competition. Since node N10 is correct and MN1 is ON-state and has a large size, node N3 can be restored, and then node N3 drives MP1 to restore node N4.

(c) When the affected high-impedance node pair is <H2, H4>, Q can provide the latched 0 value because the shared charge does not flow to other nodes.

(d) When the high-impedance and internal nodes are affected, this situation is the same as (c) above.

DNU-Case 2: When the flipped node pair arises in the different modules. It is similar to an SNU, and because the above SNU cases can be recovered, it will not be discussed again. The examples of flips are shown in the simulation figure below.

Finally, consider the following three cases of TNU. Because the flipping between the internal node and the high-impedance node and the flipping of the high-impedance node does not affect the value stored in Q, the following TNU will not discuss the high-impedance node.

TNU-Case 1: When the flipped node sequence takes place in the same module, this is also the most serious case. For example, the node sequence <N2, N3, N4> is flipped, Nodes N2 and N4 are flipped from 1 to 0, and node N3 is flipped from 0 to 1. MP1, MP2, MP5, MN2, MN6, and MN8 are turned OFF temporarily, MP3, MP4, MP6, and MN3 are turned ON temporarily, causing node N1 to flip, which leads to MN11 turn ON, node N8 is flipped, and node N7 is also reversed (MN8 is OFF-state). Node N5 is in a competitive state, and if N5 is flipped, it will affect N11 to flip because N6 is the correct value, and MN15 has a large size. Node Q will not flip, and then Q can restore N11. The correct value of

node N10 will always drive MN1 ON because the transistor size of MN1 is larger. It will pull down node N3 node to 0. Thus, node N3 is restored, node N3 drives MP1 ON, node N4 is also restored after MP1 is ON-state, MP2, MP5, and MN2 are also restored to ON-state, node N2 can also be restored, restored node N2 will make MN6 and MN8 ON, thus restore nodes N1 and N7, node N8 is restored by node N7 drive MP8, so all nodes can be restored.

TNU-Case 2: When the flipped node sequence occurs in two different modules. For example, the node sequence is <N6, N8, Q>. Nodes N6 and N8 are flipped from 1 to 0, and node Q is flipped from 0 to 1. MN9, MN13, MN15, MP14, MP16, and MP19 are temporarily turned OFF, while MP10, MP11, MP13, and MN17 are temporarily turned ON. None of the other nodes are affected. Node N7 is unaffected because the transistor size of MN8 is large, node N7 drives MP8 ON, and node N8 is restored. Node N8 drives MN9 ON, and since MP9 and MP12 are ON-state, N6 can be restored. Next, the correct value of node N6 drives MN15 ON, so node Q can be restored. All nodes can restore correct value.

TNU-Case 3: When the flipped node sequence happens in three different modules. The instances of flips are illustrated in the simulation figure below. This is similar to an SNU, and given that the preceding SNU instances are recoverable, there is no need to discuss them again.

From the above discussion, the LORD-TNU latch proposed in this paper can achieve the self-recovery of TNU, and the discussion is greatly reduced on account of the symmetry of the latch structure. Next, simulation experiments are used to validate the above discussions.

IV. SIMULATION RESULTS

To verify the fault tolerance and robustness of the proposed LORD-TNU latch, the HSPICE simulation tool is used to simulate fault injection in the 32nm PTM (Predictive Technology Model) process. The temperature is 25°C, the power supply voltage is 0.9V, the clock frequency is 500MHz, and the driving capability of the transmission gates is simultaneously enhanced. The same conditions are used for all comparison experiments. For fault injection, the double exponential current source model [25] in (1) is used to simulate, and the rise time (τ_1) and fall time (τ_2) of the pulse are set to 0.1ps and 3ps, respectively.

$$I_{inj}(t) = \frac{Q_{inj}}{\tau_1 - \tau_2}\left(e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}}\right) \qquad (1)$$

Where Q_{inj} represents the charge collected by time t, I_{inj} represents the injected current pulse, and τ_1 and τ_2 illustrate the aggregation time constant and the particle trajectory establishment time constant [26].

Fig. 8 left side (0 ~ 7ns) displays the simulation results without fault injection, demonstrating that the proposed latch works properly.

The simulation results of single-node fault injection in the latch are shown in Fig. 8 right side (7 ~ 16ns). When D = 0, the fault injection time considering nodes N2, N3, N4, and Q
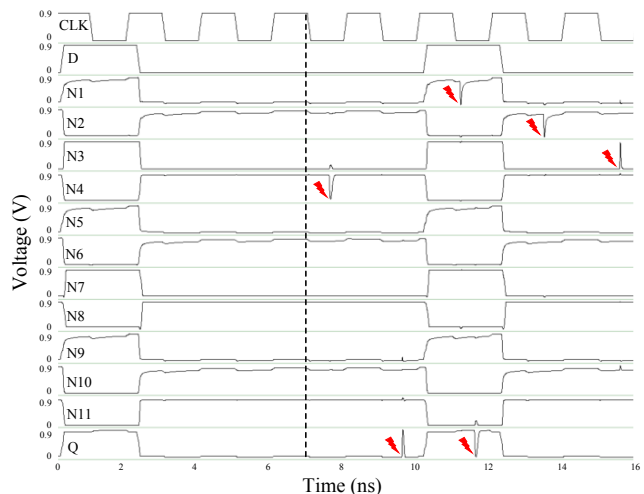

Fig. 8. Simulation waveforms for error-free injection and SNU cases.

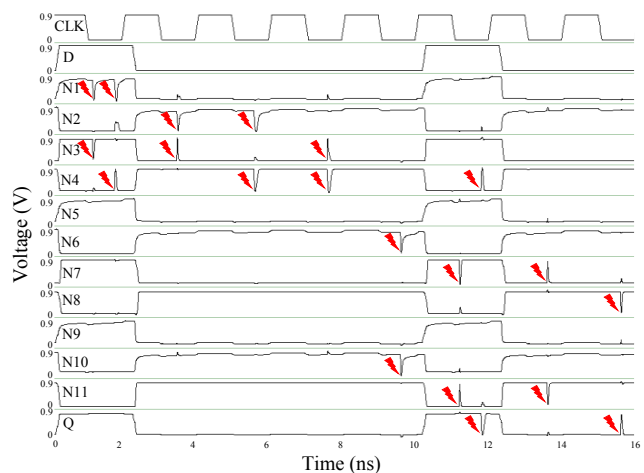
Fig. 9. Simulation waveforms for DNU cases.

are 13.5ns, 15.6ns, 7.6ns, and 9.6ns, respectively. Similarly, when D = 1, considering nodes N1 and Q, the fault injection time is 11.2ns and 11.6ns, respectively. The simulation results indicate that the proposed LORD-TNU latch can achieve SNU self-recovery.

The simulation results of latch double-node fault injection are presented in Fig. 9. In the previous section, it was established that when D = 0, the fault injection times for node pairs <N2, N3>, <N2, N4>, <N3, N4>, <N6, N10>, <N7, N11>, and <N8, Q> are 3.5ns, 5.6ns, 7.6ns, 9.6ns, 13.6ns, and 15.6ns, respectively. When D = 1, the fault injection times for node pairs <N1, N3>, <N1, N4>, <N7, N11>, and <N4, Q> are 1.2ns, 1.8ns, 11.2ns, and 11.8ns, respectively. The simulation results demonstrate the ability of the proposed latch to achieve self-recovery of DNU.

The simulation results of latch triple-node fault injection are provided in Fig. 10. When D = 0, the node sequences <N2, N3, N4>, <N6, N7, N10>, <N6, N8, Q>, <N7, N8, N11>, <N2, N6, N10>, and <N3, N8, Q> are considered for fault injection at times 3.3ns, 5.5ns, 7.6ns, 9.6ns, 13.5ns, and 15.2ns, respectively. When D = 1, the node sequences <N1,

TABLE I
RELIABILITY OF LATCHES FOR TNU AND OVERHEAD COMPARISON OF LATCHES

| Latch	Ref.	TNU Tol.	TNU Rec.	Transistor Numbers	Power (μW)	T_{Setup} (ps)	T_{Hold} (ps)	T_{DQ} (ps)	T_{CQ} (ps)	$T_{AVG.}$ (ps)	PDP (aJ)
HITTSFL	[17]	√	×	60	0.42	11.44	5.37	44.37	37.78	41.08	17.25
TNU-Latch	[18]	√	×	82	0.46	16.42	6.40	126.23	119.14	122.69	56.44
TNUHL	[19]	√	×	38	0.35	35.26	-3.50	46.06	20.63	33.35	11.67
TNUTL	[20]	√	×	36	0.44	11.15	5.26	41.67	41.41	41.54	18.28
LRLPT	[21]	√	√	80	3.27	42.37	2.28	31.22	26.65	28.94	94.63
LCTNUCR	[22]	√	√	122	0.63	30.52	5.85	39.92	38.99	39.46	24.86
TNURL	[23]	√	√	128	1.24	52.47	15.05	23.90	20.70	22.30	27.65
LCTNURL	[24]	√	√	84	0.87	39.15	11.14	32.36	25.85	29.11	25.33
LORD-TNU	Proposed	√	√	52	0.66	25.43	2.38	20.11	15.73	17.92	11.83
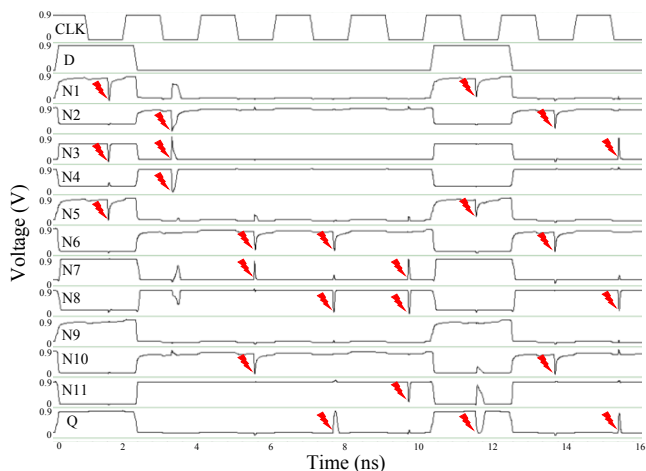
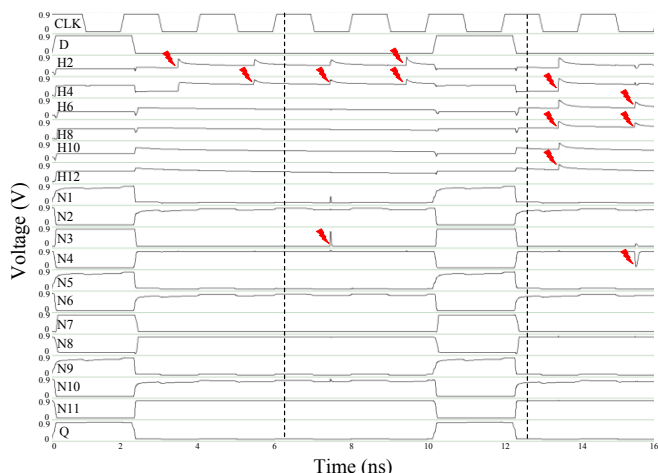Fig. 10. Simulation waveforms for TNU cases.

Fig. 11. Simulation waveforms for SNU, DNU, and TNU cases with high-impedance nodes.

N3, N5> and <N1, N5, Q> are considered. Fault injection is performed at 1.6ns and 11.4ns, respectively. The simulation results illustrate the efficacy of the proposed latch in accomplishing self-recovery of DNU.

The fault injection with high-impedance nodes is shown in Fig. 11. The single-node fault injection considers nodes H2 and H4, and the time of fault injection is 3.5ns and 5.5ns. The double-node fault injection considers the node pairs <N3, H4> and <H2, H4>, and the fault injection time is 9.5ns and 13.5ns. The triple-node fault injection node sequences <H4, H8, H12> and <H6, H8, N4> are considered. Fault injection is performed at 13.5ns and 15.5ns. The simulation results illustrate the efficacy of the proposed latch in accomplishing self-recovery of SNU, DNU, and TNU cases with high-impedance nodes.

The results of reliability and overhead comparison are shown in Table I (The term "Tol." represents the Tolerant, and "Rec." represents the Recovery). Columns 3 and 4 indicate that the LRLPT, LCTNUCR, TNURL, and LCTNURL latches exhibit the equivalent level of fault tolerance to the proposed LORD-TNU latch. For a more precise comparison between latches of the same type, Fig. 12 depicts their comparative overheads. It includes delay, area (number of transistors), and power consumption. As seen in Fig. 12, the overhead of the proposed LORD-TNU latch is superior in all aspects except the power of LCTNUCR.

The number of transistors used by each latch is listed in column 5 of the table. TNURL latch has the greatest number of transistors due to multiple interception modules. LCTNUCR latch also has a relatively large number of transistors owing to the use of multiple clocked four-input CEs. The proposed LORD-TNU latch has the lowest transistor count amongst latches of the TNU self-recovery.

The average power was calculated over a 20ns duration when the latch is error-free in column 6. On account of the formation of multiple feedback loops during the transparent period, LRLPT has the highest power consumption. The power consumption of the proposed LORD-TNU latch is lower than other latches.
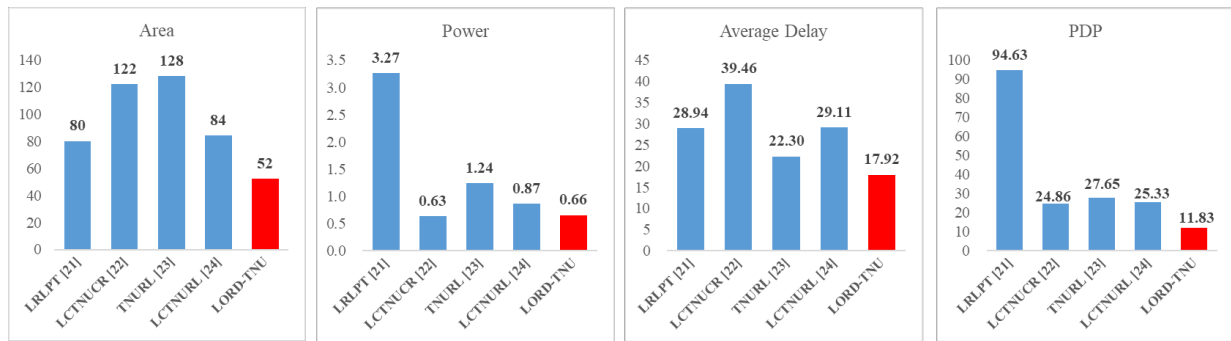
Fig. 12. Comparison of latch overhead of the same type.

Columns 7 and 8 show the setup and hold times. Since setup and hold times are crucial parameters for clocked storage elements, both are measured at the trailing edge of the clock. [18]. The TNUHL latch measured hold delay in column 6 is negative because there is an inverter before the first transmission gate. It introduces a time delay greater than the transmission gate opening or closing delay. The proposed LORD-TNU latch has the fourth shortest setup time, behind only HITTSFL, TNU-Latch, and TNUTL latch, and has the second shortest hold time, behind only LRLPT.

Columns 9, 10, and 11 demonstrate the delay overhead of the latch. Column 9 refers to the delay time of the latch from D to Q. TNU-Latch owes to the lack of a high-speed path, and the delay is relatively high. Compared with other latches, the proposed LORD-TNU latch has the lowest delay overhead. Column 10 is the delay time from CLK to Q, and the proposed LORD-TNU latch is also the lowest. Column 11 is the average delay from D to Q and CLK to Q, and the formula is shown in (2). The proposed latch is also the lowest.

The formula for calculating the PDP [27], [28] of the 12 columns is shown in (3). Being able to display the characteristics of the power consumption and delay of the display circuit, the PDP of the proposed latch is also lower.

$$T_{AVG.} = (T_{DQ} + T_{CQ}) / 2 \qquad (2)$$

$$PDP = Power * T_{AVG.} \qquad (3)$$

To intuitively observe the relative changes in these structural overheads, TABLE II compares the relative overheads of LORD-TNU latches and contrast latches, where Δ and Δ average values are calculated as shown in (4) and (5) [29]. If the value is positive, the LORD-TNU latch is not as effective as another latch. A negative value indicates that the LORD-TNU latch is superior to the comparison latch. TABLE II makes it abundantly evident that only the LCTNUCR latch power consumption is less than the proposed latch.

$$\Delta = \frac{(The\ proposed - The\ existing)}{The\ existing} \times 100\% \qquad (4)$$

$$\Delta\ Average = \frac{(The\ proposed - Average)}{Average} \times 100\% \qquad (5)$$

TABLE II
COMPARISON OF THE RELATIVE OVERHEAD OF LATCHES

Latch	ΔArea	ΔPower (μW)	$\Delta T_{AVG.}$ (ps)	ΔPDP (aJ)
LRLPT [21]	-35.00%	-79.82%	-38.08%	-87.50%
LCTNUCR [22]	-57.38%	4.76%	-54.59%	-52.41%
TNURL [23]	-59.38%	-46.77%	-19.64%	-57.22%
LCTNURL [24]	-38.10%	-24.14%	-38.44%	-53.30%
Average	-49.76%	-56.07%	-40.17%	-72.56%

As semiconductor technology rapidly develops, the transistor feature size continues to shrink, making the latch variation with process, voltage, and temperature (PVT) more obvious. To ensure that the latch operates correctly under corresponding PVT fluctuations, it needs to be analyzed and evaluated, so the effects of different PVT on delay and power consumption are analyzed by the HSPICE tool.

Fig. 13 shows the fluctuation of latch power consumption and delay under the change of supply voltage, temperature, and threshold voltage (other subfigures in Fig. 13 share the legend of Fig. 13(a)). From Fig. 13(a) and (b), the power consumption increases and the delay decreases with the increase of the power supply voltage. The power consumption of the LORD-TNU latch varies greatly with the voltage, but the delay changes little and is at the lowest value.

The effect of temperature change on latch power consumption and delay is shown in Fig. 13(c) and (d). As temperature increases, power consumption decreases while delay increases. Under the temperature fluctuation of -40 ~ 120°C, the power consumption and delay of the LORD-TNU latch fluctuate little and are stable, and the delay is at the lowest value.

The effect of the threshold voltage change on the latch power consumption and delay is shown in Fig. 13(e) and (f). When the threshold voltage is increased, the power consumption goes down, and the delay goes up. When the threshold voltage fluctuates from 0.01 to 0.08V, the power consumption of the LORD-TNU latch fluctuates greatly, but the delay tends to be stable and at the lowest value.
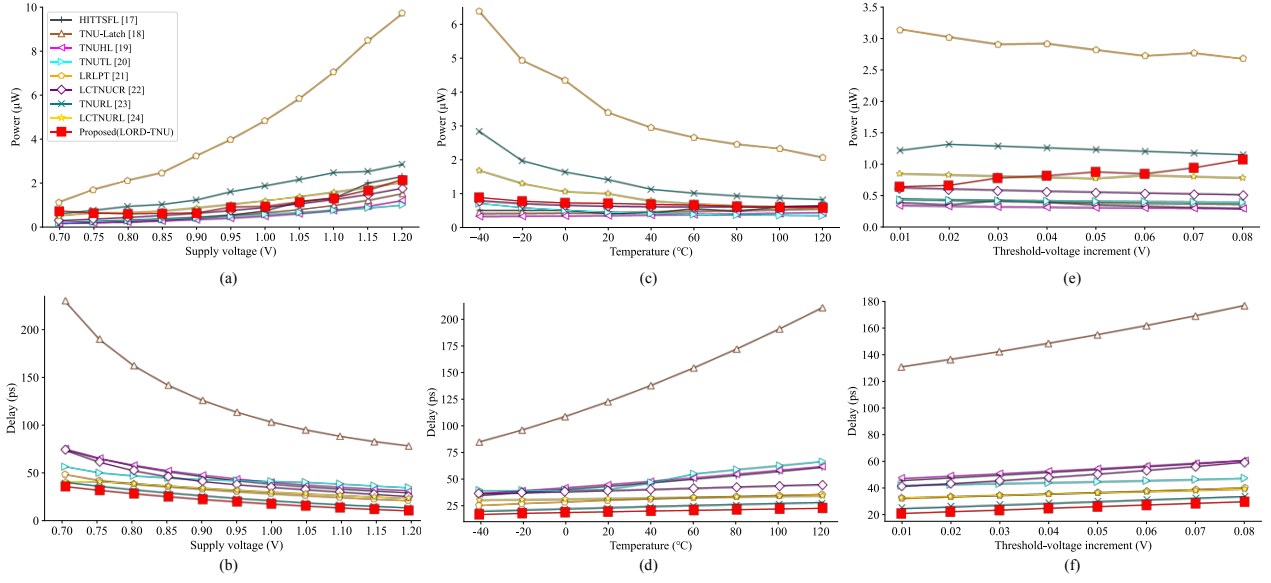
Fig. 13. The simulation of PVT variation. (a) and (b) The variation of power and delay at different voltages. (c) and (d) The variation of power and delay at different temperatures. (e) and (f) The variation of power and delay at different threshold voltages.
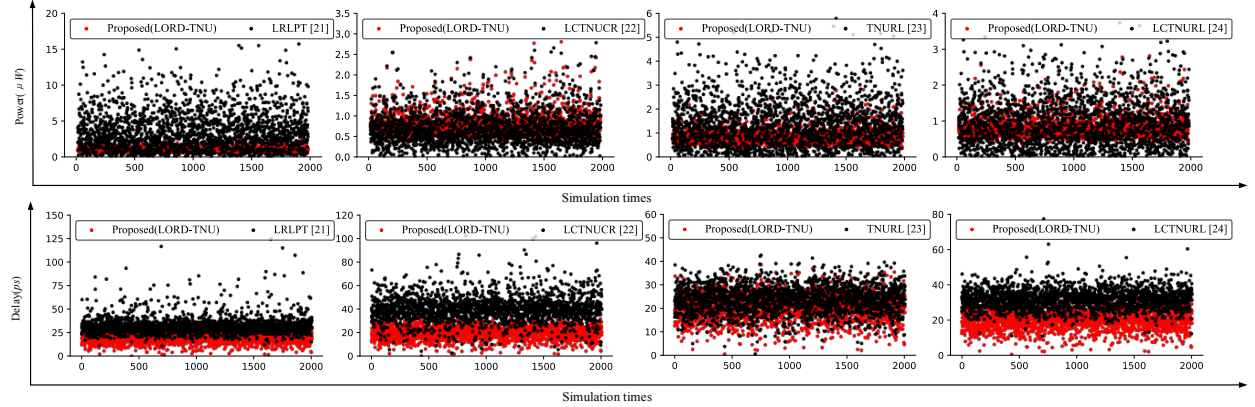

Fig. 14. Monte Carlo simulation results on the delay and power.

Fig. 14 shows the power consumption and delay results of the Monte Carlo simulation. The simulations are based on 2000 samples, using a ±20% Gaussian distribution sweeping supply voltage, changing at the ±3σ level. In addition, a ±10% Gaussian distribution is used to change the threshold voltage at ±3σ level. At the same time, the temperature shows absolute Gaussian distribution, the variation range at ±3σ level, and the fluctuation range is -40 ~ 120℃. Compared with four existing similar hardened structures, the degree of delay data dispersion is similar (data is relatively concentrated), so the above latch is less sensitive to PVT. Because the power consumption of LRLPT, LCTNURL, and TNURL latches varies substantially, they are susceptible to PVT fluctuations. Since LORD-TNU and LCTNUCR power consumption statistics exhibit little volatility, PVT changes have little effect on them. In summary, whether delay or power consumption, LORD-TNU features lower or comparable sensitivity to PVT variations than the other compared latches.

In order to assess the circuit sensitivity to process variations more intuitively, Table III provides the standard deviation (σ) and average deviation (AD) to evaluate the dispersion of delay and power consumption for five latches under different process conditions. σ and AD values are calculated as shown in (6) and (7).

$$\sigma = \sqrt{\frac{\Sigma(X_i - \bar{X})^2}{N}} \qquad (6)$$

$$AD = \frac{\Sigma|X_i - \bar{X}|}{N} \qquad (7)$$

Among them, N is the number of simulations, which is 2000, X_i represents the i-th simulation value, and $\bar{X}$ is the average value.

Compared to four existing latches of the same type, the

TABLE III
EXPERIMENTAL RESULTS FOR STANDARD DEVIATION (σ) AND AVERAGE DEVIATION (*AD*)

Latch	Ref.	Power		Delay	
		σ	AD	σ	AD
LRLPT	[21]	2.76	2.15	15.97	7.32
LCTNUCR	[22]	0.42	0.31	11.12	8.00
TNURL	[23]	0.97	0.76	19.19	5.04
LCTNURL	[24]	0.67	0.52	7.95	4.72
LORD-TNU	proposed	0.29	0.20	5.58	4.39

Proposed LORD-TNU latch has the lowest value among the comparison latches, indicating that process variations have a relatively minor impact on LORD-TNU.

V. CONCLUSION

This paper proposes a novel radiation-hardened latch to recover TNUs. The simulation results show that the design of the proposed LORD-TNU can achieve the self-recovery of TNUs according to the triple-modular redundancy and stacked transistors. Verification has been performed to confirm the robustness and low cost of the LORD-TNU latch. Compared to four existing TNU hardened latches, the proposed LORD-TNU reduces area overhead by 49.76%, power consumption by 56.07%, delay overhead by 40.17%, and the PDP by 72.56% on average, respectively. PVT and Monte Carlo analyses demonstrate the better stability of LORD-TNU latch.

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