A single-electron stochastic associative processing circuit robust to random background-charge effects and its structure using nanocrystal floating-gate transistors

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Abstract. A new single-electron circuit using the unique features of single-electron devices is proposed based on a basic strategy and circuit architecture for achieving large-scale integration. A unit circuit consisting of a single-electron transistor and a capacitor operates as an exclusive-NOR gate by the Coulomb blockade effect, and its transient behavior is stochastic due to electron-tunneling events. Using this unit circuit, a stochastic associative processing circuit is proposed based on a new information-processing principle where the association probability depends on the similarity between the input and reference data. This circuit can be constructed by using a silicon nanocrystal floating-gate structure in which dots are regularly arranged on a gate electrode of an MOSFET. The simulation results of a simple digit pattern association demonstrate the successful stochastic operation. The background-charge effects on the proposed circuit are analyzed and simulated, and it is shown that the circuit is much more robust to such effects than the conventional single-electron logic circuits.

1. Introduction

Recently, a large number of theoretical and experimental studies of single-electron devices have been carried out [1, 2, 3], and various circuits using these devices have been proposed. Some circuits are based on the idea of replacing conventional CMOS devices with single-electron transistors (SETs), as shown in figure 1 [4, 5]. These circuits are expected to operate as binary logic gates in which a binary state is represented by the presence or absence of a single electron or a few electrons in isolated islands.

However, in order to construct CMOS-like digital integrated circuits using SETs, there are several serious difficulties related to the features of SETs: (i) The operation of SET circuits is not deterministic because electron transport is based on single-electron tunneling events that randomly occur with a tunneling probability. Because of this property, the gate delay time fluctuates significantly, and a sufficiently low error rate is not attained at a high clock frequency. Thus, this stochastic property degrades the operational speed and reliability. (ii) The effects of charges randomly induced on isolated islands surrounded by tunnel junctions, which are referred to as random background-charge effects, are a very serious problem for correct circuit operation [3]. Random background charges are mainly induced by defects and/or impurities located within the oxide barriers [4], and these defects cannot be entirely removed with the present technology. Although the amounts of charge induced on an island are usually large, an excess over $\pm e/2$ is compensated for by electrons tunneling to or from other islands, where e is the elementary charge. Therefore, background charges distribute over a range of $[-e/2, e/2]$ with a uniform probability. However, it has been estimated that the background charge margins in CMOS-like logic circuits are much smaller than $|e/2|$, typically $0.03e$ [5, 6]. Even if future technology makes it so that almost no islands have any background charge, even a few background charges may cause fatal errors in the operation of a whole circuit in multi-stage logic circuits. In small-scale circuits, this problem can be solved by individual biasing for each island [7], but this solution cannot be used for large-scale integrated (LSI) circuits.

Thus, in order to construct practical SET LSI circuits, we have explored new circuits and systems based on new information-processing principles different from conventional digital logic systems. It is very important to invent new systems that use unique properties of quantum devices. We propose here a strategy for achieving SET LSI circuits and present an example of such systems.

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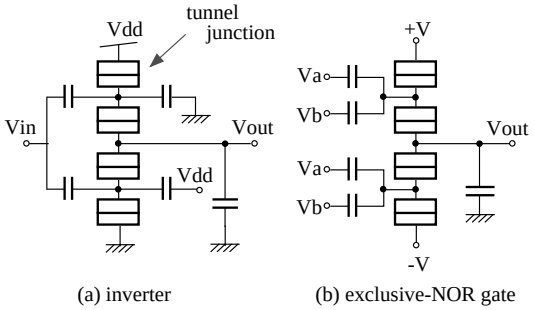

Figure 1. Conventional CMOS-like SET logic circuits.

In this context and in relation to difficulty (i), there have been some proposals of new circuits which positively utilize the stochastic property of single-electron devices. One such proposal involves a Boltzmann machine circuit [8]. The Boltzmann machine is an information-processing model using a statistical mechanics system in which each element behaves stochastically. However, because in this case the output capacitance of each element must be small enough to represent a binary state with a single electron, integrated circuit design is difficult.

We have already proposed another system utilizing the stochastic property referred to as stochastic associative memory [9]. In this paper, we propose and analyze a new circuit for constructing this system. Since the proposed circuit has a simple circuit configuration, it is more robust against random background-charge effects than the CMOS-like SET circuits.

This paper is organized as follows: Section 2 presents a strategy for achieving SET LSI circuits. Section 3 proposes a unit circuit used in a dynamic operation mode. Section 4 describes a stochastic associative processing circuit and its structure using silicon nanocrystal floating-gate MOSFETs. We confirm the basic function of a stochastic association by simulating digit pattern association. In section 5, the random background-charge effects in this circuit are analyzed. Finally, we present our conclusions in section 6.

All simulations described in this paper were performed by a Monte Carlo single-electron circuit simulator developed according to the model presented in [10, 11]. The simulation algorithm is briefly described in Appendix.

2. Strategy for achieving SET LSI

Single-electron devices should be used for massively parallel processing with a vast number of devices because of their large packing density and ultra-low power dissipation. Parallel processing compensated for the low operation speed. Adopting a few logic stages, a small fanout, and regularity or repeatability in the circuit architecture, the reliability in circuit operation is improved and the background-charge effects are reduced.

Ultra-small CMOS devices should also be used for multi-stage logic circuits, while single-electron devices should be used for simple functional circuits with massively parallel processing and few logic stages.

Large output capacitor should be used as an interface between SET and CMOS circuits. The information generated by massively parallel processing in SET circuits is collected and integrated into the output capacitor and is transferred to the CMOS circuits. The gate capacitance of an ultra small CMOS device can be used as such a capacitor.

In order to reduce the sensitivity to background charges, new information-processing concepts and models that can use the information averaging and/or redundant configurations have to be adopted.

3. SET unit circuit

A unit circuit used in dynamic operation mode consists of a SET and a large capacitance C_O, as shown in figure 2(a). The typical capacitance values and other parameters used in the simulation are also shown in figure 2(a) and (b). Here, the maximum number of electrons accumulated in C_O is given by $C_O V_{dd}/e \approx 19$. We also assume that the junction capacitance C_j is of the order of 1 aF and that the operation temperature T is 1 mK, where single-electron devices operate without thermal disturbance.

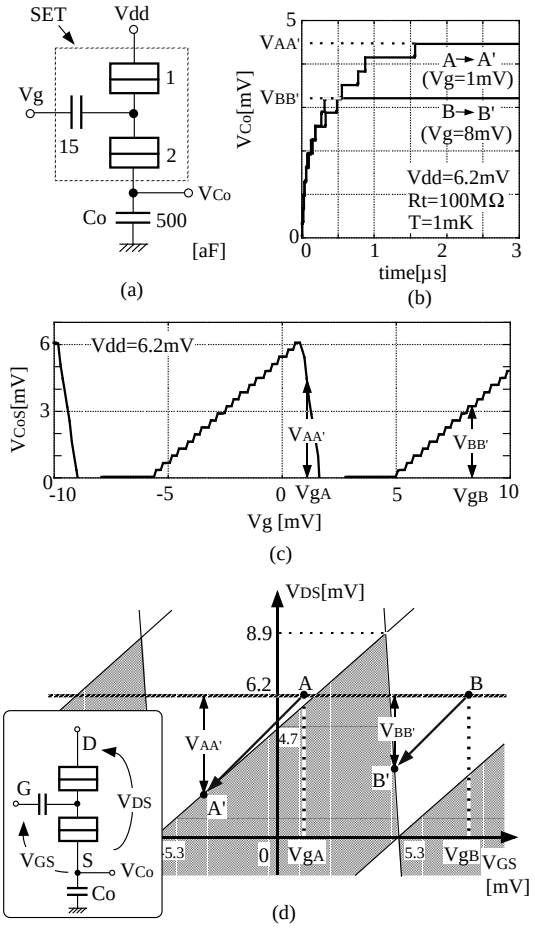

Figure 2. Unit circuit and its characteristics: (a) circuit diagram, (b) transient behavior of V_{Co}, (c) relationship between V_{CoS} and V_g, and (d) Coulomb blockade diagram; shaded areas represent Coulomb blockade regions where no electron flows through SET, while in the non-shaded area electrons flow through SET.

Figure 2(b) shows the transient behavior of output voltage V_{Co}. The output voltage in the steady state, V_{CoS}, depends on the gate voltage V_g. The relationship between V_{CoS} and V_g is non-monotone and periodic, as shown in figure 2(c). This characteristic is derived from the Coulomb blockade oscillation, and can be explained using the Coulomb blockade diagram of a SET [12], as shown in figure 2(d). Let $V_{Co} = 0$ V at the initial state and the unit circuit start to operate from point A or B in figure 2(d). A current flows through the SET, and V_{Co} increases. As V_{Co} increases by ΔV, both voltages $V_{DS} (= V_D - V_{Co})$ and $V_{GS} (= V_G - V_{Co})$ shown in the inset of figure 2(d) decrease by ΔV. Thus, the operation point moves along the line A–A' or B–B', with an angle of -135 degrees from the horizontal axis in the diagram. When the operation point reaches the boundary of the Coulomb blockade regions (point A' or B'), the current stops, and the unit circuit becomes stable. The difference between $V_A (V_B)$ and $V_{A'} (V_{B'})$, that is $V_{AA'} (V_{BB'})$, equals the V_{CoS} in figure 2(c); both of which are also equal to the stable voltages in figure 2(b).

The unit circuit shown in figure 2(a) is identical to half of the conventional CMOS-like SET inverter shown in figure 1(a). Because of the simpler structure, the unit circuit is more robust for random background-charge effects, as described in section 5. However, the unit circuit does not have a current path for discharging C_o in itself. Before operation, we have to reset V_{Co} by using some discharging measure. We propose two methods that enable discharging without changing the unit circuit configuration. One method is to ground V_{dd} and to give a proper bias to the gate (V_g). When the device characteristics fluctuate and/or background charges exist, it may be difficult to determine the proper bias voltage. Scanning the gate voltage is a sure method for guaranteeing the complete discharge of V_{Co}. Another method is to use an ultra-small MOS device connected with C_o in parallel. This method is very effective, especially when many SETs are connected with

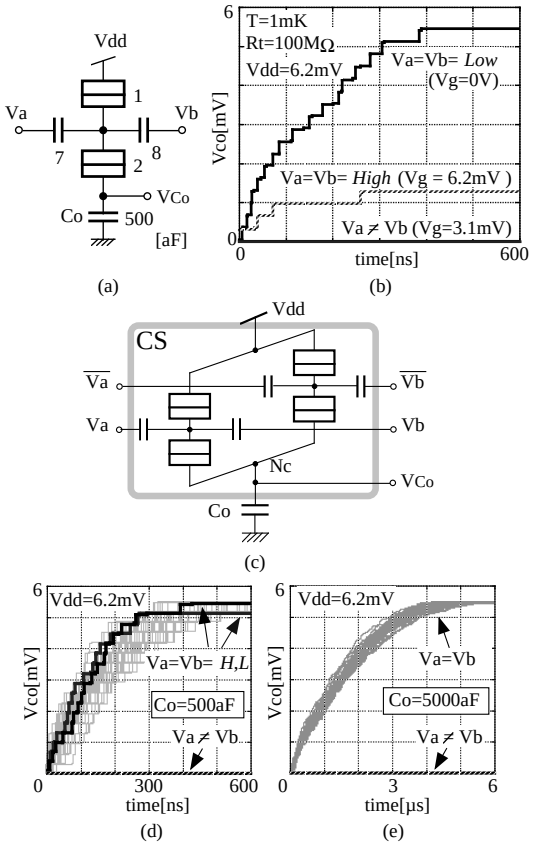

Figure 3. Exclusive-NOR gate using the unit circuit: (a) the gate using a single unit circuit and (b) transient behavior of V_{Co}; (c) the gate using complementary configuration and its stochastic behavior (simulation results of 50 trials): (d) C_O = 500 aF, (e) C_O = 5000 aF.

one output capacitor C_o, as described in section 4.

Using the non-monotone characteristic shown in figure 2(c), an exclusive-NOR (XNOR) gate is obtained with only one unit circuit in which the gate is divided into two input terminals: V_a and V_b, as shown in figure 3(a). The simulation results are shown in figure 3(b). Electrons pass through the SET to the capacitor C_O only when $V_a = V_b = L$ or H, although the output voltages in both cases are not equal. In order to equalize both output voltages, a complementary configuration of SETs (CS) is introduced, as shown in figure 3(c). Figures 3(d) and (e) show the waveforms of V_{Co}, where C_O is 500 aF and 5000 aF, respectively. In both simulations, the operations are repeated fifty times when the same inputs are applied, and all waveforms are represented by the gray lines in the figure. Here, the circuit is initialized with $V_{Co} = 0$ before every operation. Because of the stochastic event in each electron tunneling, the rise time of voltage V_{Co} fluctuates in every operation, even if the same inputs are applied. The fluctuation in figure 3(e) is smaller than that shown in figure 3(d) because the stochastic characteristic is eventually averaged as the number of electrons accumulating in the capacitor increases. Thus, the XNOR gates with larger C_O operate more deterministically, and those with smaller C_O operate more stochastically. Larger C_O obviously leads to a longer circuit-delay time, and a C_O that is too small makes integrated circuit design difficult. The appropriate capacitance value depends on the application.

The co-tunneling effect should be mentioned here. This effect causes a leakage current in the Coulomb blockade region, and thus increases V_{CoS} when $V_a \neq V_b$. However, if the unit circuit is used in a dynamic mode, that means the transient characteristics of the circuit are used, this effect hardly affect the circuit operation.

Although we assumed operation temperature of 1 mK in the simulations, it was verified that the circuit with the same parameters as shown in figure 3(a) can operate properly up to around 3 K. Moreover, it was also verified that the circuit can operate up to around 100 K if the capacitance values except C_o is reduced

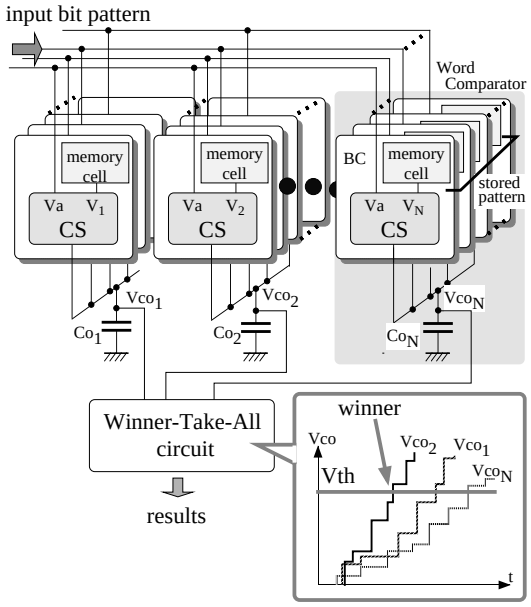

Figure 4. Stochastic associative processing circuit.

to one tenth, where thermal disturbance is used for stochastic operation.

To avoid misunderstanding, it should be noted that the circuits shown in figures 2 and 3 are not logic gates in the usual sense of this term. It is difficult to use them in multi-stage logic circuits because they should be externally reset after each clock cycle; they cannot sustain arbitrary logic levels for long time due to the co-tunneling effect; and their output voltage is lower than the input voltage.

4. Stochastic associative system

4.1. Principles of stochastic association

An associative memory is usually defined as a system that extracts the pattern most similar to the input pattern from the stored reference patterns. When a pattern is represented by a set of binary data, which is referred to as a word, the associative memory compares the input pattern bits with all stored pattern bits. As a simple similarity measure, a Hamming distance is often used, which is defined as the number of the different bits between the two bit patterns. Conventional deterministic associative memory, such as content-addressable memory (CAM) [13] or Hopfield networks [14], always gives the same result for the same input pattern.

In a stochastic associative system, the association probability depends on the similarity between the input and the stored patterns. This system associates not only the stored pattern most similar to the input but also other similar stored patterns. A larger number of repetitive associations gives a more precise order of similarity [9].

4.2. Stochastic associative processing circuit using SET unit circuit

Figure 4 shows a stochastic associative processing circuit architecture using the SET unit circuit. This architecture consists of word comparators and a Winner-Take-All (WTA) circuit. Each word comparator consists of a number of bit comparators (BCs) and evaluates the Hamming distance between the input and each stored pattern with stochastic fluctuation. Because the BC is obviously an XNOR gate, we can construct a stochastic BC by using the unit circuit described in the previous section. Thus, the word comparator is constructed by connecting nodes N_c of the plural CS' shown in figure 3(c) with the common output capacitor C_O. The number of CS' that pass electrons to the capacitor C_O increases as the Hamming distance decreases, resulting in a shorter rise time for the voltage V_{Co}. However, even when the Hamming

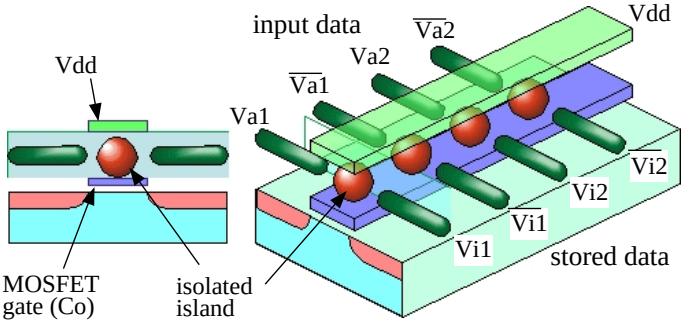

Figure 5. Device structure image of the word comparator.

distance is at its shortest, the output voltage does not always increase rapidly because of the stochastic characteristics in CS' as shown in figure 3(d) or (e).

The WTA circuit selects the word comparator output that reaches the threshold voltage most rapidly, which means that it selects the stored pattern having the shortest Hamming distance. Because the output capacitance C_O is large enough, e.g. 0.5 fF, the input stage of the WTA circuit can be constructed by sub-100nm MOS devices (C_{ox} <1 fF). Thus, we can construct a WTA circuit using CMOS devices, as described in references [15, 16], and we assume that the WTA circuit operates deterministically.

A device structure image of the word comparator is shown in figure 5. Isolated islands of SETs are regularly arranged on a capacitor plate, which corresponds to an electrode of C_O and also a gate electrode of an ultra-small MOS device. This structure will be fabricated as a sophisticated version of silicon nanocrystal floating-gate MOSFETs [17, 18] by using highly-controlled self-assembly processes.

4.3. Simulation results

We confirmed the basic association operation by simulation of a digit pattern association. Each stored pattern consisted of seven segments and represented a digit number of $\{0, 1, \cdots, 9\}$. Because the ON/OFF state of each segment corresponded to a bit data, the stored data consisted of ten vectors, each of which had seven binary elements.

The simulation of the system was performed as follows; (a) Input bit data V_a and stored data V_i $(i = 1, 2, \cdots, 9)$ were supplied to BCs as voltage signals. (b) Operation of the word comparators that consisted of single-electron devices was simulated by the Monte Carlo simulator. (c) Operation of the WTA circuit was simulated as an ideal *black-box* that simply selected a winner from outputs of the word comparators.

Two examples of output-voltage changes in the word comparators when the input pattern was '5' are shown in figure 6(a). Because of the stochastic property, different patterns become winners; one is the pattern most similar to the input pattern '5', and the other a second similar pattern '6'. Figure 6(b) shows the association probabilities of all stored patterns where the input pattern is '5', and figure 6(c) is another simulation result, where the input pattern is not included in the stored patterns. Both simulation results show that the association probability of the stored pattern increases as the Hamming distance from the input pattern decreases.

5. Random background-charge effects

Because of the stochastic feature in our system, background charges fluctuating in time domain hardly affect the associative operation. However, fixed background charges can cause errors in the association probability. In the following, the fixed background-charge effects are analyzed. We assume that background charges are induced on isolated islands (nodes) randomly chosen at a certain rate η; their amounts Q_p distribute over a range of $[-e/2, e/2]$ with a uniform probability, and Q_p remains constant during the operation. It is emphasized again that for conventional CMOS-like SET circuits, if $|Q_p|$ exceeds a certain small value, e.g. $0.03e$ [5], for only one node, the whole circuit does not operate correctly.

The unit circuit used in our stochastic associative processing circuit has only one isolated node. When a background charge is induced at the isolated node, the transient behavior of V_{Co} varies, and the bit

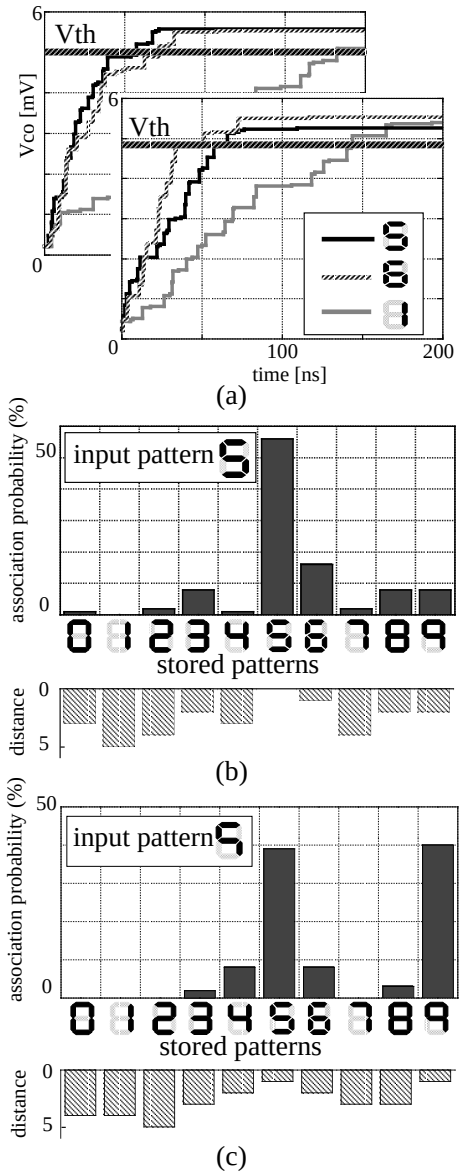

Figure 6. Simulation results: (a) output voltage changes in word comparators, (b),(c) association probabilities for stored patterns, where the association is repeated 100 times.

comparison result inverts if Q_p is $+0.3e$. However, our circuit is less sensitive to the effects than the conventional CMOS-like logic circuits, which can be explained as follows: In CMOS-like logic circuits, as shown in figure 1, two types of SETs that charge and discharge the output capacitance, respectively, must operate complementarily irrespective of background charges. On the other hand, our unit circuit consists of one type of SET that only operates for charging. Discharging operation can be independent of background charges, as described in section 3.

The bit-comparator (XNOR gate) in our circuit has two isolated nodes, as shown in figure 3(c). Because the two SETs operate complementarily, the combinations of the two inputs are either H, H and L, L or H, L and L, H. We name each node in terms of the combination of inputs; i.e., HH, LL, HL, LH. If we assume that the associative memory has M stored data of N bits, then the number of total isolated nodes is $2MN$, and the average number of total background charges induced is $n = 2MN\eta$. Each node of the word comparators is schematically shown in figure 7(a), where word comparators $WC_i, (i = 0, 1, \cdots, M)$ are arranged in order of the Hamming distance to the input data. Here, it is assumed for simplicity that the Hamming distance increases one by one for several upper WC_i's; i.e., i is equal to the Hamming distance

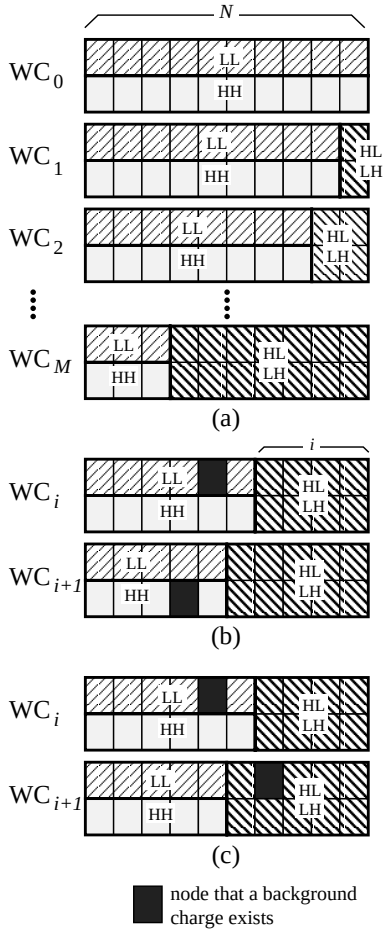

Figure 7. (a) State of each isolated node in word comparators. (b),(c) Two simplest cases where association probability distribution can be changed.

for these WC_i's.

Our associative processing circuit can only associate stored data having a Hamming-distance difference of less than μ from the most similar data by using the stochastic operation. For the simulation condition in the digit pattern association, μ is around 4 to 5 bits, as shown in figure 6. Therefore, the number of stored data concerning association is independent of the total number of stored data M. This is an important point when the robustness of our circuit to the background-charge effects is estimated.

Let us consider the situations in which the associative processing circuit makes a mistake by background charges. According to figure 3(b), when $Q_p = 0$, LL nodes make the largest contribution to current flow, HH nodes make the second contribution, and HL or LH (HL/LH) nodes make no contribution. There are the two simplest cases where the association probability can be changed: (1) A background charge is induced at an LL node of WC_i, and at the same time, another background charge is induced at an HH node of WC_{i+1}, as shown in figure 7(b); (2) A background charge is induced at an LL node of WC_i, and another background charge is induced at an HL/LH node of WC_{i+1}, as shown in figure 7(c). Here, note that $i \leq \mu$.

We simulated background-charge effects at a word comparator when $N = 7$. When a background charge is induced in each LL, HH, or LH node of WC_2 and WC_3, the average time to reach the threshold voltage is shown in figure 8. When $Q_p = 0$, WC_2 obviously reaches the threshold voltage most rapidly. However, if the contribution of the LL node to the current flow becomes smaller than that of the HH or HL node, the associative processing circuit makes a mistake in the estimation of the similarity order. For example, when background charges of an LL node of WC_2 and an HH node of WC_3 are equally $+0.4e$, WC_3 reaches the threshold voltage more rapidly than WC_2. From the calculation results for all cases in which two background

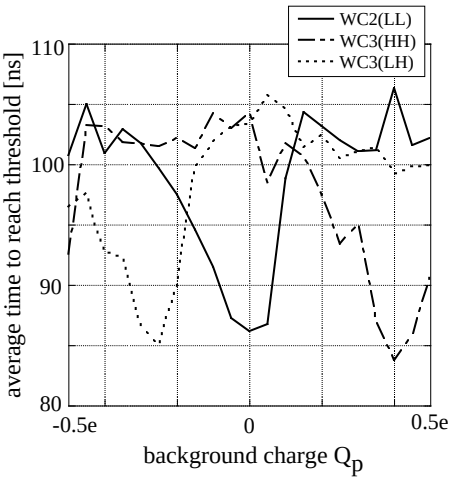

Figure 8. Relationship between background charge amount and average time to reach the threshold voltage (simulation results of 300 trials).

charges are randomly induced at LL and HH or LL and HL/LH nodes, respectively, we found that the probabilities of wrong association for cases (1) and (2) are equally about 0.5.

Since the above two probabilities are equally of the order of unity, and because μ is independent of M, we can roughly estimate the probability P_c that the associative processing circuit leads to correct results irrespective of induced background charges for large-scale circuits. An analytical derivation of probability P_c is very complicated because many cases must be considered. However, the main factor contributing to P_c is the probability that no background charges are induced at LL nodes of WC_i. This is because the ratio of the number of HL/LH nodes to that of HH/LL nodes becomes very small for data having short Hamming distances if $N \gg 1$. Therefore, if $M \gg 1, N \gg 1$, then,

$$\begin{aligned} P_c &\sim \frac{\left(\begin{array}{c} 2MN-N \\ n \end{array} \right)}{\left(\begin{array}{c} 2MN \\ n \end{array} \right)} \\ &= \frac{(2MN-N)!}{(2MN-N-n)!n!} \cdot \frac{(2MN-n)!n!}{2MN!} \\ &= \prod_{k=0}^{n-1} \left(\frac{2MN-N-k}{2MN-k} \right). \end{aligned} \tag{1}$$

If $n \ll 2MN-N$, that is $\eta \ll 1-(1/2M)$, then,

$$\begin{aligned} P_c &\sim \left(\frac{2MN-N}{2MN} \right)^n = \left(1 - \frac{1}{2M} \right)^{2MN\eta} \\ &= \left(1 + \frac{1}{-2M} \right)^{(-2M)(-N\eta)}. \end{aligned} \tag{2}$$

Using the equation for the base of a natural logarithm:

$$\lim_{x \to \pm\infty} \left(1 + \frac{1}{x} \right)^x = \mathrm{e}, \tag{3}$$

one can obtain

$$P_c \sim \mathrm{e}^{-N\eta}. \tag{4}$$

if $N\eta \ll 1$, the associative processing circuit leads to correct results with a high probability. It should be noted that P_c is independent of M, as is intuitively understandable. Figure 9 shows the simulation results for P_c as a function of η when $M = N = 7$. Although this does not necessarily meet the condition $M, N \gg 1$, the

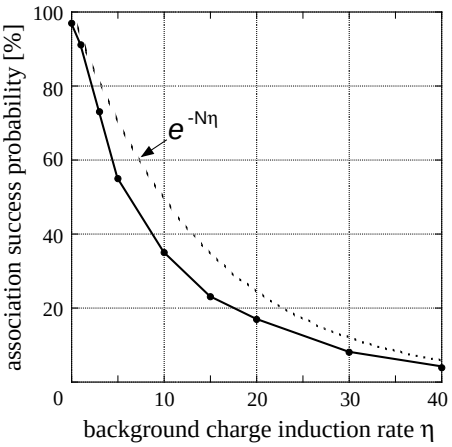

Figure 9. Background charge effect on the association success probability, where $M = N = 7$. Each point was obtained by simulation of 100×100 trials.

simulation results are on the same order as those obtained by using (4), indicating that the above estimation for P_c is valid.

It should also be noted that we can achieve further lowering of background-charge effects if we adopt redundant circuit configurations where plural BCs are used for comparison between the input and each stored data.

6. Conclusion

We have presented a strategy for designing SET LSI circuits. We use single-electron devices for simple functional circuits with few logic stages and CMOS devices for multi-stage logic circuits, and use a large capacitor as an interface for the two devices. On the basis of this strategy, we have proposed a unit circuit operating in a dynamic operation mode and a new stochastic associative processing circuit using the unit circuit. We positively utilize the stochastic property for implementing a new association processing scheme. Stochastic association for digit patterns was successfully demonstrated by a single-electron Monte Carlo simulation.

As for background-charge effects, the stochastic operation in our circuit hides the effects of background charges randomly fluctuating in time domain. On the other hand, for the effects of fixed background charges, we found that the error rate is only dependent on the bit number of the data, and independent of the number of stored data, indicating that our associative processing circuit is very suitable for large-scale associative systems.

Because the single-electron device used for this associative processing circuit can be simple and regular, we expect that a prototype device will be fabricated in the near future.

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Appendix

The Monte Carlo simulation algorithm used in this paper is briefly described as follows [10, 11].

Step 1: Compute the electrostatic energy for the current state.

Step 2: Compute the electrostatic energies for all possible subsequent states that can be reached from the current state by one electron tunneling process.

Step 3: Compute the energy difference ΔE_i between each subsequent state i and the current state.

Step 4: Calculate the following waiting time τ_i for a tunneling process corresponding to each subsequent state:

$$\tau_i = \frac{1}{\Gamma_i} \ln \frac{1}{r}, \tag{5}$$

where r is a uniform random number ($0 < r < 1$), and mean tunneling rate Γ_i is given by the "orthodox" theory:

$$\Gamma_i = \frac{\Delta E_i}{e^2 R_T [1 - \exp(-\Delta E_i / k_B T)]}, \tag{6}$$

where R_T is a tunneling resistance, k_B is the Boltzmann constant, e is the elementary charge, and T is temperature.

Step 5: Select the tunneling event that has the shortest waiting time, and set the corresponding subsequent state as the current state. Then, return to Step 1.

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