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PAPER

A CMOS Spiking Neural Network Circuit with Symmetric/ Asymmetric STDP Function

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SUMMARY In this paper, we propose an analog CMOS circuit which achieves spiking neural networks with spike-timing dependent synaptic plasticity (STDP). In particular, we propose a STDP circuit with symmetric function for the first time, and also we demonstrate associative memory operation in a Hopfield-type feedback network with STDP learning. In our spiking neuron model, analog information expressing processing results is given by the relative timing of spike firing events. It is well known that a biological neuron changes its synaptic weights by STDP, which provides learning rules depending on relative timing between asynchronous spikes. Therefore, STDP can be used for spiking neural systems with learning function. The measurement results of fabricated chips using TSMC 0.25 μm CMOS process technology demonstrate that our spiking neuron circuit can construct feedback networks and update synaptic weights based on relative timing between asynchronous spikes by a symmetric or an asymmetric STDP circuits.

key words: *spiking neuron model, associative memory, spike-timing dependent synaptic plasticity (STDP), LSI implementation*

1. Introduction

A biological neuron receives many electric spike impulses via synapses, and it fires by generating a spike impulse. Recently, the spiking neuron models, which express analog information by the timing of neuronal spike firing, attract a lot of attention with expectation of their higher information processing ability [1], [2]. From the theoretical research of neural network models, it is expected that more advanced neural systems can be developed using the spiking neuron models. Since these models operate asynchronously, it is also expected that spiking neural networks operate faster than the conventional synchronous models.

From the viewpoint of VLSI implementation, spiking neurons output binary values in the voltage or current domain and represent analog values in the time domain. Therefore, spiking neural network systems can easily be connected to the existing digital systems than the conventional analog neural network systems that output analog values in the voltage or current domain. Additionally, when feedback-type networks are constructed using spiking neurons, we have an advantage that unexpected oscillation hardly occurs.

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So far, the spiking neuron models have often been applied to feedforward networks; for example, image data processing using a spiking feedforward network was proposed [3]. However, there have been only a few reports about spiking feedback networks. In order to express analog values by spike timing in feedback networks, spikes expressing the zero values are required. However, a neuron generates no spike unless its internal potential exceeds the threshold, and usually the resting (membrane) potential corresponding to the zero value is below the threshold. Therefore, a simple information representation scheme by spike timing cannot be applied to such feedback networks. To solve this problem we have introduced a global excitatory unit (GEU) or by modulating the resting potential [4], [5]. It has also been demonstrated that our spiking neuron model can be applied to the Hopfield network, which is a typical feedback network model, and that it has a retrieval property as associative memory [4], [5].

It is known that a biological neuron changes its synaptic weights by STDP (Spike-Timing Dependent synaptic Plasticity). STDP provides learning rules based on relative timing between asynchronous spikes. Therefore, STDP can be used effectively for spiking neural systems with learning function. There are two types of STDP function which are characterized by symmetric and asymmetric time windows, as shown in Fig. 1 [6]–[8]. In symmetric STDP, if spikes *pre* and *post* are given simultaneously ($t_{post} - t_{pre} = 0$), the synapse increases its weight ($\Delta V_{wij} > 0$). On the other hand, if spikes are given with a time difference of around t_n, the weight decreases. In contrast, asymmetric-STDP synapses update their weights based on the temporal order of spikes as well as the absolute time difference.

An asymmetric STDP function was realized by analog CMOS circuits and applied to spiking neuron models [9], [10]. In addition, we have proposed a synapse circuit with a

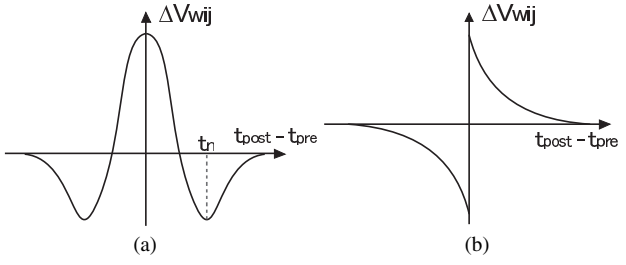

Fig. 1 STDP functions: (a) symmetric and (b) asymmetric.

symmetric STDP function and a Hopfield-type VLSI neural network using it [11], [12].

In this paper, we propose an analog CMOS circuit which achieves spiking neural network with STDP, and show measurement results of fabricated LSI chips using TSMC 0.25 μm process technology [13]. The measurement results demonstrate that the circuits we have designed realize the symmetric/asymmetric STDP functions and spiking feedback network operation with learning by STDP.

2. CMOS Spiking Neural Network Circuit

2.1 Integrate-and-Fire-Type Spiking Neuron

The integrate-and-fire-type (IF) neuron model is shown in Fig. 2, which is a typical spiking neuron model. When a spike pulse is fed into a neuron via a synapse, a post-synaptic potential (PSP) is generated. A neuronal internal potential is determined by the spatiotemporal summation of PSPs generated by the input spikes. There are two types of synapses: excitatory and inhibitory, according to the sign of the synaptic weight w_{ni}.

In the simple IF model, the time courses of PSPs are the same, which we call here a unit PSP, $P(t)$, as a convolutional kernel, and a PSP from neuron i to neuron n, $PSP_{ni}(t)$, is given by the temporal summation of unit PSPs multiplied by the corresponding synaptic weight w_{ni}:

$$PSP_{ni}(t) = \sum_{t_i^{(f)} \in \mathcal{F}_i} w_{ni} P(t - t_i^{(f)}) \tag{1}$$

where $\mathcal{F}_i = \{t_i^{(1)}, \cdots, t_i^{(n)}\}$ is the set of firing times of neuron i. The type and amplitude of a PSP are determined by the sign (positive or negative) and the absolute value of synaptic weight w_{ni}, respectively. Since a PSP is generated by an RC circuit, the unit PSP is given by

$$\begin{aligned} P(t) = P_0\{&(1 - e^{-t/\tau})\mathcal{H}(t)\mathcal{H}(t_p - t) \\ &+ (1 - e^{-t_p/\tau})e^{-(t-t_p)/\tau}\mathcal{H}(t - t_p)\} \end{aligned} \tag{2}$$

where P_0 is a constant, τ is the time constant for decay, t_p is the time span between the time when the unit PSP starts to increase and the time when it has the peak value. The internal potential of neuron n, $V_n(t)$, is given by the spatial summation of $PSP_{ni}(t)$:

$$V_n(t) = \sum_{i \in \Gamma_n} PSP_{ni}(t) \tag{3}$$

where Γ_n is the set of inputs to neuron n. The effect of a PSP is temporary, and $V_n(t)$ returns to the resting potential level after the PSP ceases. When the $V_n(t)$ exceeds the threshold th, a neuron n fires and generates a spike. After firing, a refractory period follows. A generated spike is transmitted to other neurons or the neuron itself with a certain transmission delay time.

In our spiking neuron model, analog information expressing processing results is given by the relative timing of spike firing events. If we use the spike train of a certain neuron #1 as reference spikes, the analog information $x_i^{(f)}$ normalized in [0, 1] is expressed by

$$x_i^{(f)} = \begin{cases} \frac{2\Delta t_{i1}^{(f)}}{T} & (\Delta t_{i1}^{(f)} \le T/2) \\ \frac{2(T - \Delta t_{i1}^{(f)})}{T} & (\Delta t_{i1}^{(f)} > T/2) \end{cases} \tag{4}$$

where $\Delta t_{i1}^{(f)} = |t_i^{(f)} - t_1^{(f)}|$ $(i = 1, 2, 3 \ldots)$, and T is the inter-spike interval at the stable state, as shown in Fig. 3.

Figure 4 shows our CMOS spiking neuron circuit and its timing diagram. The CMOS spiking neuron circuit consists of a synapse part and a neuron part. If spike pulse i_i is fed into the synapse part from other neurons, a PSP control signal (*psp_cont*) is generated by a delay-and-inversion circuit (*D&I*) and a NOR gate. The *D&I* consists of an inverter chain, and their delay time is determined by bias voltages V_{bi}. While *psp_cont* is "High," transconductance amplifier (gm-amp) A turns on and charges or discharges capacitor C in the neuron part. Thus, the terminal voltage of the capacitor, V_n, is changed, and a PSP is generated. The spatiotemporal summation of PSPs by input spikes is performed at this capacitor. The current from the synapse is determined by $V_{w_{ij}}$. The gm-amp A generates a current in proportion to $V_{w_{ij}} - V_{ref}$. When $V_{w_{ij}} - V_{ref} > 0$, the circuit operates as excitatory synapse, and vice versa.

In the neuron part, the internal potential represented by V_n returns to resting potential V_{ini} by leak resistance R_L

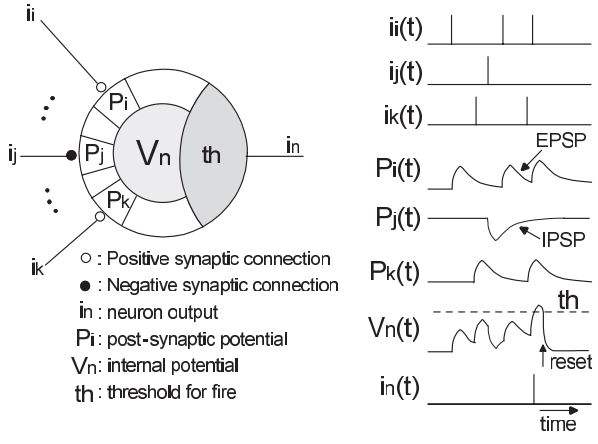

Fig. 2 Integrate-and-fire-type neuron model.

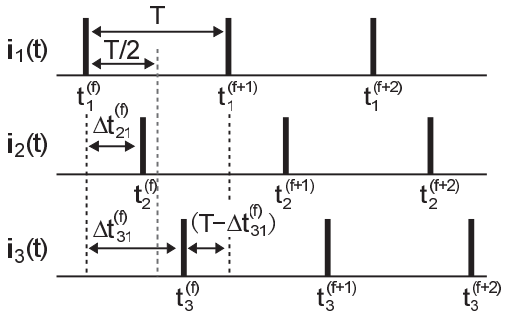

Fig. 3 Information representaion using relative timing of spikes.

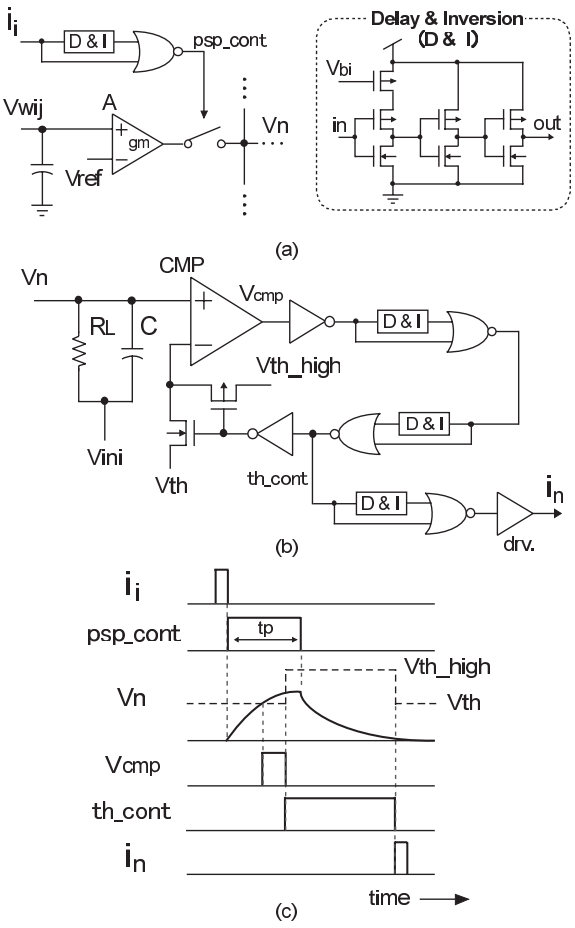

Fig. 4 Spiking neuron circuit: (a) synapse part (PSP generation), (b) neuron part and (c) timing diagram.

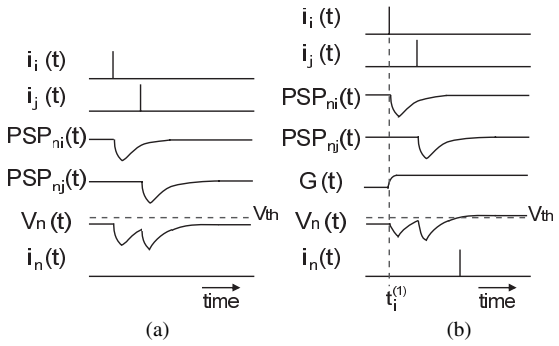

Fig. 5 Examples of input/output spike trains and neuronal internal potentials without (a) and with (b) *GEU*.

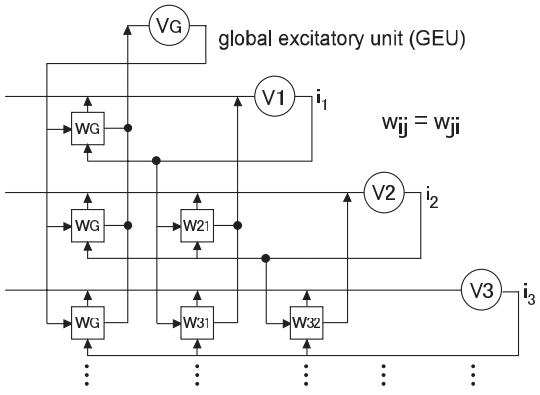

Fig. 6 Spiking feedback network with GEU.

connected in parallel with capacitor C, after charged or discharged by the current sources of the synapse parts. A comparator (*CMP*) compares V_n with threshold voltage V_{th}. If V_n exceeds V_{th}, a spike is generated. At the same time, the threshold voltage increases to generate a refractory period. In this circuits, the transmission delay is equal to the refractory period.

2.2 Spiking Feedback Networks

In the IF neuron model, if V_n does not exceed the threshold as shown in Fig. 5(a), the neuron obviously generates no spikes. However, in order to apply the spiking neuron model to feed-back networks with continuous states, spikes have to be generated pseudo-periodically to express an analog value by spike timing.

To achieve this, one of the authors proposed *negative thresholding* operation and a global excitatory unit (*GEU*) [4]. Figure 6 shows a spiking feedback network model with *GEU*, where all neurons are connected each other. In this network, *GEU* receives spikes from all neurons via excitatory synapses, and it is activated by the earliest input spike. The activated *GEU* gives a continuous-level stimulus to all neurons. Therefore, *GEU* gives the same effect as a decrease in the threshold levels of all neurons. If once *GEU* is activated, even a neuron at the resting state can fire, and a neuron with stronger inhibition generates a spike with later timing as shown in Fig. 5(b).

The neuron and synapse circuits shown in Fig. 4 are also used as the *GEU* circuit and the synapse circuits between *GEU* and neurons, respectively. In order to give a constant effect from *GEU* to all neurons, we use a PSP with a longer pulse width than the whole operation time.

3. CMOS STDP Circuits

3.1 Circuit Principle Generating STDP Functions

A circuit principle that generates STDP functions is shown in Fig. 7. In our STDP circuits, we use a current sampling scheme [14]; the first spike is used as a trigger to generate a nonlinear waveform $V_{NW}(t)$ corresponding to the STDP function shape and the second one is used as a sampling pulse. Because the circuits generate a nonlinear waveform by themselves, asynchoronous operation is achieved. In Fig. 7, gm-amp A updates synaptic weight $V_{w_{ij}}$ in proportion to $V_{NW}(t) - V_{ref}$. Current $i(t)$ is given by $G_m(V_{NW}(t) - V_{ref})$, where G_m is the transconductance. Thus, $\Delta V_{w_{ij}}$ is given by

$$\Delta V_{w_{ij}} = \int_{t_s}^{t_s+\Delta t} G_m(V_{NW}(t) - V_{ref})dt \tag{5}$$

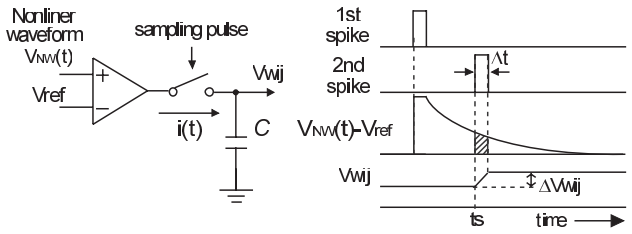

Fig. 7 Circuit principle for STDP generation.

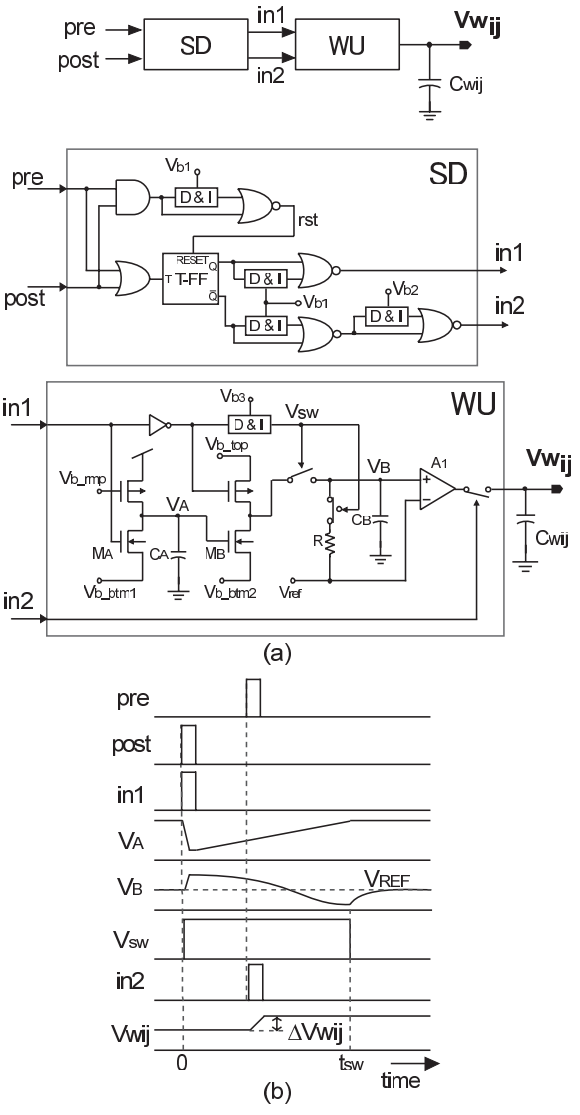

Fig. 8 Symmetric STDP circuit (a) and timing diagram (b).

3.2 Symmetric STDP Circuit

Figure 8 shows our CMOS symmetric STDP circuit and its timing diagram. The circuit consists of a spike-detection part *SD* and a weight-update part *WU*.

In *SD*, the state value of the T-FF (toggle flip-flop) is changed twice by input spikes *pre* and *post*. Changes in the state value are detected by a *D&I* and a NOR gate. As a result, an earlier spike pulse is fed into *in*1 of *WU*, and the other is fed into *in*2. If *pre* and *post* are given at the same time, the state value of the T-FF changes once. In that case, the T-FF is reset by an AND gate, a *D&I* and a NOR gate. Thus, based on only the absolute time difference between input spikes *pre* and *post*, *WU* updates the synaptic weight represented by $V_{w_{ij}}$. The details of the operation in *WU* are as follows.

When the input spike *in*1 is fed into *WU* from *SD*, ramp signal $V_A(t)$ is generated at the terminal of capacitor C_A by MOSFET M_A and is controlled by bias voltage V_{b_rmp}. At the same time, control signal V_{SW}, which is generated by the *D&I*, turns to "High." Ramp signal $V_A(t)$ is transformed to a nonlinear waveform by MOSFET M_B and capacitor C_B, and the waveform is supplied to the input terminal of gm-amp A_1 during this period. After V_{SW} turns to "Low," the terminal voltage of capacitor C_B, V_B, returns to reference voltage V_{ref} by resistor R. Thus, $V_B(t)$, which corresponds to $V_{NW}(t)$ in Fig. 7, is expressed as follows:

$$V_B(t) = \begin{cases} V_{b\_top} - \frac{1}{C_B}\int_0^t I_{M_B}(t')dt' & (t < t_{sw}) \\ (V_B(t_{sw}) - V_{ref})\exp(\frac{-(t-t_{sw})}{RC_B}) + V_{ref} & (t \geq t_{sw}) \end{cases} \quad (6)$$

Here, if M_B operates in the saturation region, the current flowing through this MOSFET is given by

$$I_{M_B}(t) = k\frac{W}{L}(V_A(t) - V_{b\_btm2} + V_{th})^2 \quad (7)$$

where k, W/L, and V_{th} are the capacitive coupling ratio from the gate to the channel, the aspect ratio and the threshold voltage of M_B, respectively. If input spike *in*2 is fed into *WU* while $V_B(t) \neq V_{ref}$, A_1 charges or discharges capacitor $C_{w_{ij}}$, and updates synaptic weight $V_{w_{ij}}$. If *in*2 was given after V_B returns to V_{ref}, the synaptic weight is not updated. The shape of the STDP function is determined by the bias voltages.

3.3 Asymmetric STDP Circuit

Figure 9 shows our CMOS asymmetric STDP circuit and its timing diagram. The circuit updates the synaptic weight based on the temporal order of spikes as well as the absolute time difference. In Fig. 9(b), $V_1(t)$ and $V_2(t)$ which correspond to $V_{NW}(t)$ in the Fig. 7 are expressed as follows:

$$V_1(t) = V_{b\_top1}\exp\left(\frac{-(t-t_{pre})}{\tau_1}\right) + V_{ref2} + V_{th} \quad (t \geq t_{pre}) \quad (8)$$

$$V_2(t) = V_{b\_top2}\exp\left(\frac{-(t-t_{post})}{\tau_2}\right) + V_{ref2} + V_{th} \quad (t \geq t_{post}) \quad (9)$$

where τ_1 and τ_2 are time constants if diode-connected transistors M_1 and M_2 are considered as linear resistors, and V_{th} is the threshold voltage of M_1 and M_2.

In this circuit, A_1 increases synaptic weight $V_{w_{ij}}$ in proportion to $V_1(t) - V_{ref1}$. In contrast, A_2 decreases $V_{w_{ij}}$ in

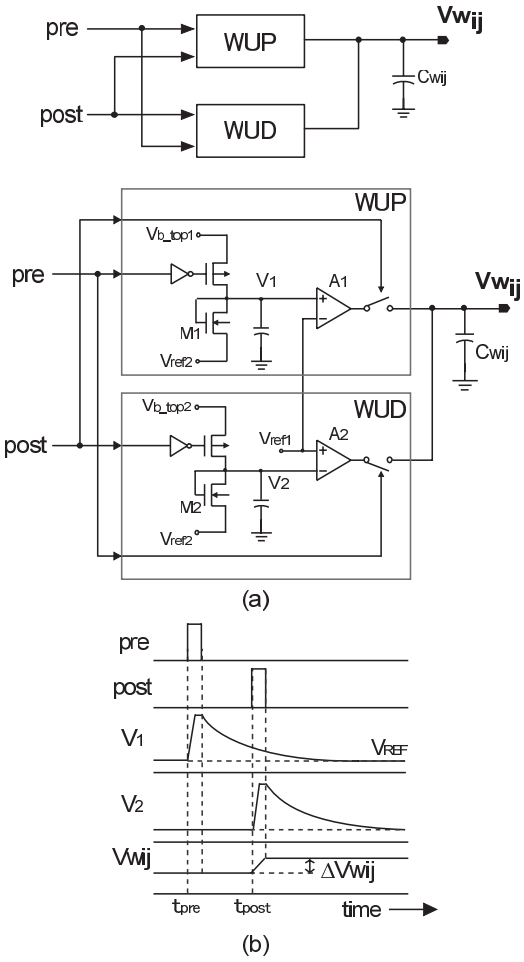

Fig. 9 Assymetric STDP circuit (a) and timing diagram (b).

proportion to $V_2(t) - V_{ref1}$. In other words, the former works for LTP (Long Term Potentiation), the latter works for LTD (Long Term Depression). If $t_{post} - t_{pre} > 0$ as shown in Fig. 9(b), input spike *pre* generates a nonlinear waveform voltage $V_1(t)$ and drives A_2 at the same time. If V_{ref1} are set at $V_{ref2} + V_{th}$, A_2 cannot update $V_{w_{ij}}$ because $V_2(t) - V_{ref1} = 0$. In this case, $V_{w_{ij}}$ is updated only by A_1. If $t_{post} - t_{pre} = 0$, A_1 and A_2 are driven by input spikes at the same time, and the currents cancel out each other.

4. Simulation of Associative Memory with Symmetric STDP

We have constructed an associative memory using a Hopfield-type neural network with our symmetric-STDP synapse circuit. The network is composed of 36 neurons with symmetric connections as shown in Fig. 6. In the typical Hopfield-type associative memory, synaptic weights w_{ij} are expressed by the sum of autocorrelation matrices of the stored pattern vectors:

$$w_{ij} = \sum_{k=1}^{N} (2I_i^k - 1)(2I_j^k - 1), \ for\ i \neq j \tag{10}$$

where $w_{ii} = 0$, and I_j^k is the i-th element of the k-th stored pattern vector.

In the circuit simulation, we gave spike patterns $(I_1^k, I_2^k, \cdots)$ to the network and made it learn the patterns by symmetric STDP. In symmetric STDP, simultaneous spikes increase the synaptic weights, and spikes with a time difference of t_n decrease the weights, as shown in Fig. 1. Thus, the symmetric STDP function can be used for realizing memorization shown in Eq. (10).

The raster plot of spikes are shown in Fig. 10(a). The number of patterns to be memorized was five. The patterns were randomly chosen under the condition that the numbers of '1' (white pixels) and '0' (black pixels) are equal. We used spike patterns that expressed the values '1' and '0' with a timing difference of t_n, where t_n was set at 90 ns. After 5 epochs, we stopped the STDP function, and gave gray-level (5-levels) input patterns that are most similar to pattern #1 to the network. In the simulation, the time step corresponding to one level in gray-level patterns was set at 25 ns. Therefore, the firing timing of input spikes was limited in {0, 25, 50, 75, 100} ns, and the time span for receiving input spikes was 100 ns. The transmission delay time and refractory period were set at 200 ns. The duration of the *psp_cont* was set at 150 ns. The simulations were performed with a fast SPICE simulator, HSIM.

Figure 10(b) shows synaptic weight changes by the symmetric STDP. From Eq. (10), the synaptic weights $w_{ij} \in \{\pm 5, \pm 3, \pm 1\}$. In this simulation, the synaptic weights increased or decreased approximately by the ratio of 5:3:1 after the learning. At 7.5 μs after receiving input spikes, the neuron outputs and the internal potentials converged to pattern #1 as shown in Figs. 10(a), (c). Thus, it has been verified that the network can learn and associate patterns from external spike inputs by using STDP.

Figure 11 shows changes in the direction cosine between stored pattern #1 and the output pattern (or the input pattern if the calculation step is 0). When the direction cosine converges to 1, the network recalls the pattern #1. In contrast, when the direction cosine converges to 0, the network recalls other patterns. Figure 11 shows that our spiking Hopfield network has a reasonable association performance.

5. Measurement Results of Fabricated Chips

We have designed and fabricated two test LSI chips for evaluation of the symmetric and the asymmetric STDP circuits and a five-neuron feedback network by using TSMC 0.25 μm (1-Poly, 5-Metal) CMOS technology. Microphotographs of the test chips are shown in Fig. 12.

5.1 STDP Circuits

A micrograph of the test chip for symmetric/asymmetric STDP circuits is shown in Fig. 12(a). The measurement results of the symmetric and asymmetric STDP circuits are shown in Figs. 13(a) and (b), respectively. The results show that our STDP circuits can update synaptic weights based

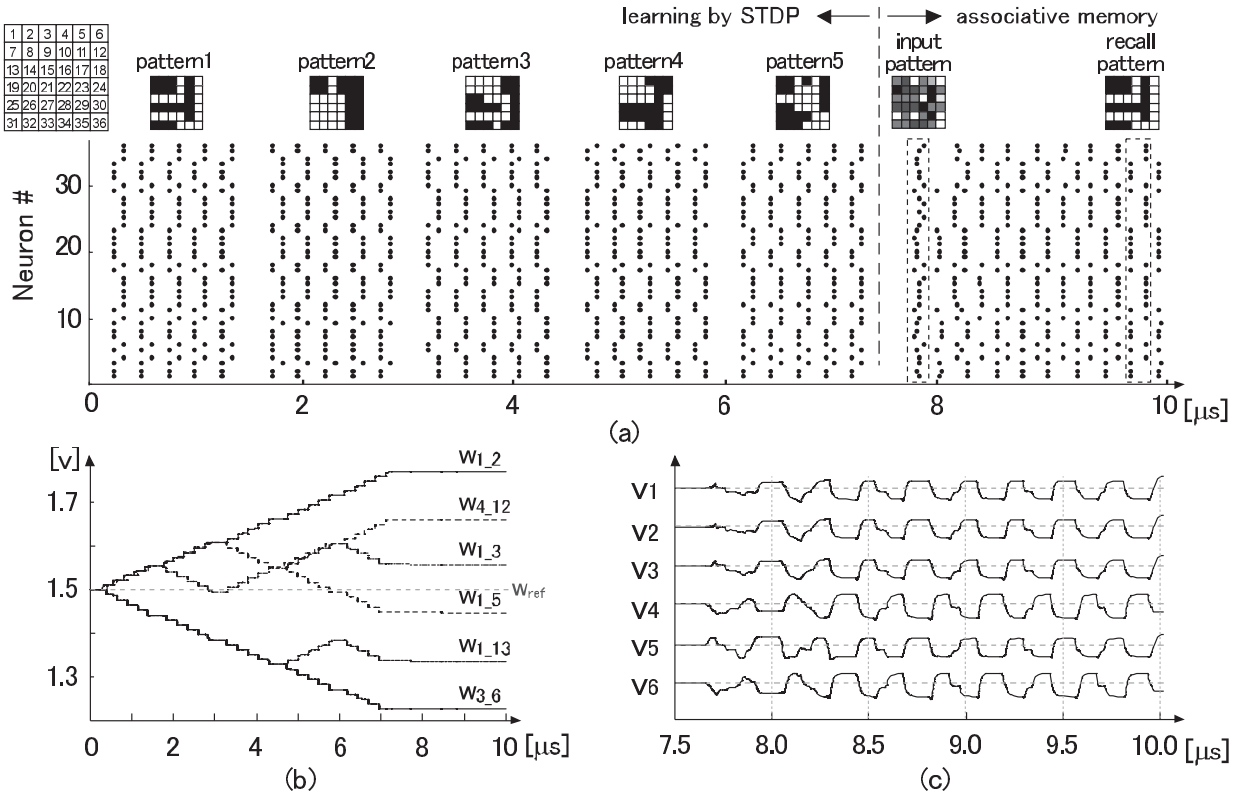

Fig. 10 Circuit simulation results of symmetric STDP learning and associative memory operation: (a) raster plot of spikes, (b) synaptic weights change and (c) internal potential of the neurons.

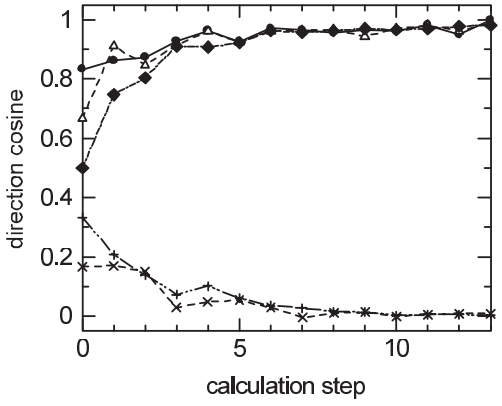

Fig. 11 Association performance of the spiking Hopfield network.

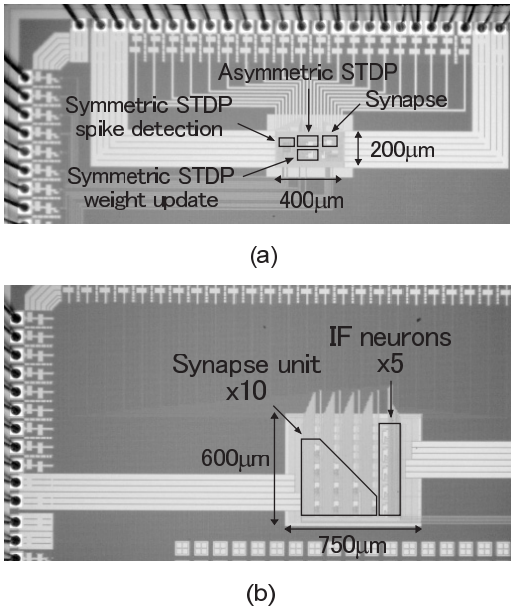

Fig. 12 Micro-photographs of the test chips: (a) symmetric/asymmetric STDP circuits and (b) spiking feedback network with symmetric STDP.

on the relative timing of spikes. In addition, the amplitude of each STDP function can be set arbitrarily by adjusting the bias voltage. Figure 14 shows an increase or a decrease in the amplitude of PSPs generated by the symmetric STDP circuit. When the time difference of two spikes is 0 ns, the circuit increases synaptic weight V_w as shown in Fig. 14(a). In contrast, when the time difference is 90 ns, synaptic weight is decreased as shown in Fig. 14(b).

5.2 Spiking Feedback Network with Symmetric STDP

We evaluated the test LSI chip for spiking feedback network with symmetric STDP shown in Fig. 12(b). This chip includes 5 neurons and 10 synapse units. The synapse unit has 2 synapse circuits shown in Fig. 4(a) and a symmetric STDP circuit. The network has symmetric connections as shown in

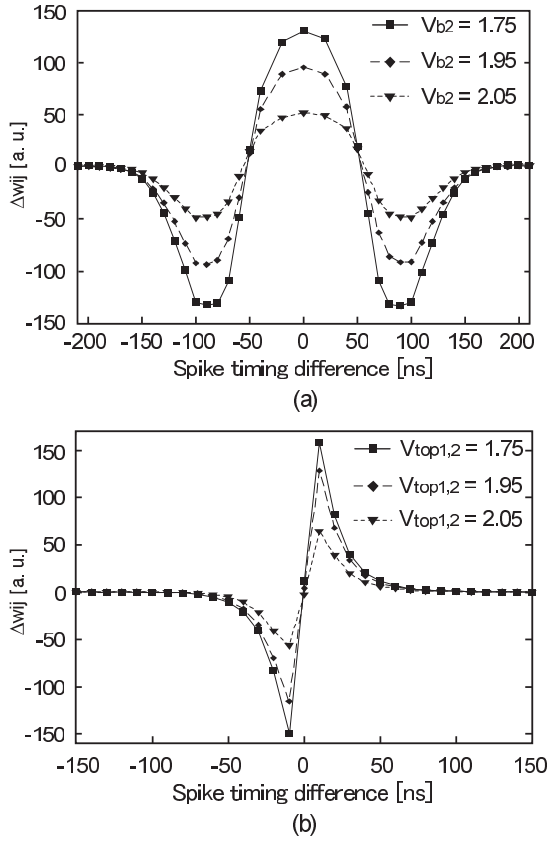

Fig. 13 Measurement results of (a) symmetric and (b) asymmetric STDP circuits.

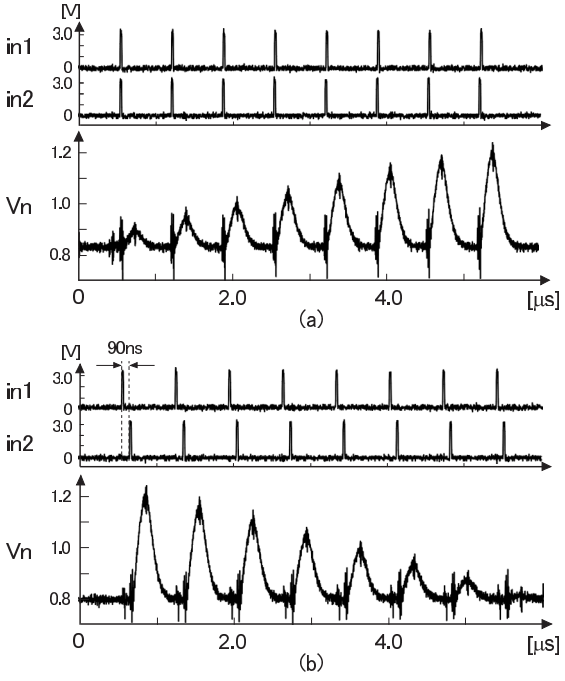

Fig. 14 Measurement results of change in amplitude of PSP by symmetric STDP: (a) timing difference of input spikes 0 ns and (b) 90 ns.

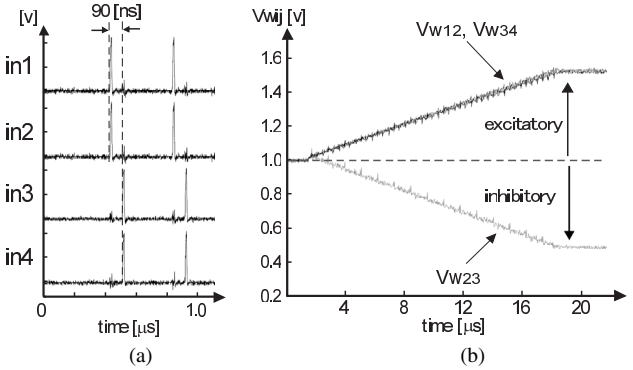

Fig. 15 Learning process using STDP: (a) input spike pattern and (b) synaptic weight change.

Fig. 6. The power consumptions of the neuron and synapse units estimated using HSPICE were 280 μW and 250 μW, respectively at a 3.3 V power supply. In the evaluation of the spiking feedback network chip, we used 4 neurons and the shape of symmetric STDP function when $V_{b2} = 1.95$ as shown in Fig. 13(a). Before network operation, we input the spike pattern shown in Fig. 15(a) to the network for 45 times, and updated synaptic weights as shown in Fig. 15(b).

After setting the synaptic weights, we stopped STDP function, and gave some input spikes to the network. Figure 16 shows measurement results of the spiking feedback network. In this figure, i_n and V_n ($n = 1, 2, 3, 4$) are output spikes and internal potentials of neurons, respectively. In both results, after several spike generations, the network converged at a stable state in which spikes are generated at a constant period. However, the output pattern at each stable state depends on the input spike pattern. In Fig. 16(a), neurons form themselves in two groups each of which generates synchronous spikes with different timing. On the other hand, in Fig. 16(b), each neuron generates spikes asynchronously. However, the spike generation sequence and the period of firing are kept constant.

In Fig. 16, time differences between spikes are almost equal to the duration of *psp_cont* shown in Fig. 17. Because spike timing is determined by the interactions between EPSP and IPSP, our spiking feedback network circuit can operate with a constant period without global clock.

6. Conclusion

We designed and fabricated LSI chips for evaluation of the spiking neural network circuit with symmetric and asymmetric STDP circuits. Measurement results demonstrated that our circuits realized accurate STDP functions, and successfully verified the operation of the spiking feedback network circuit with learning by STDP. At the next step, we will design and fabricate an LSI chip for larger scale spiking neural networks.

Acknowledgments

This work was partly supported by fund from MEXT, Japan,

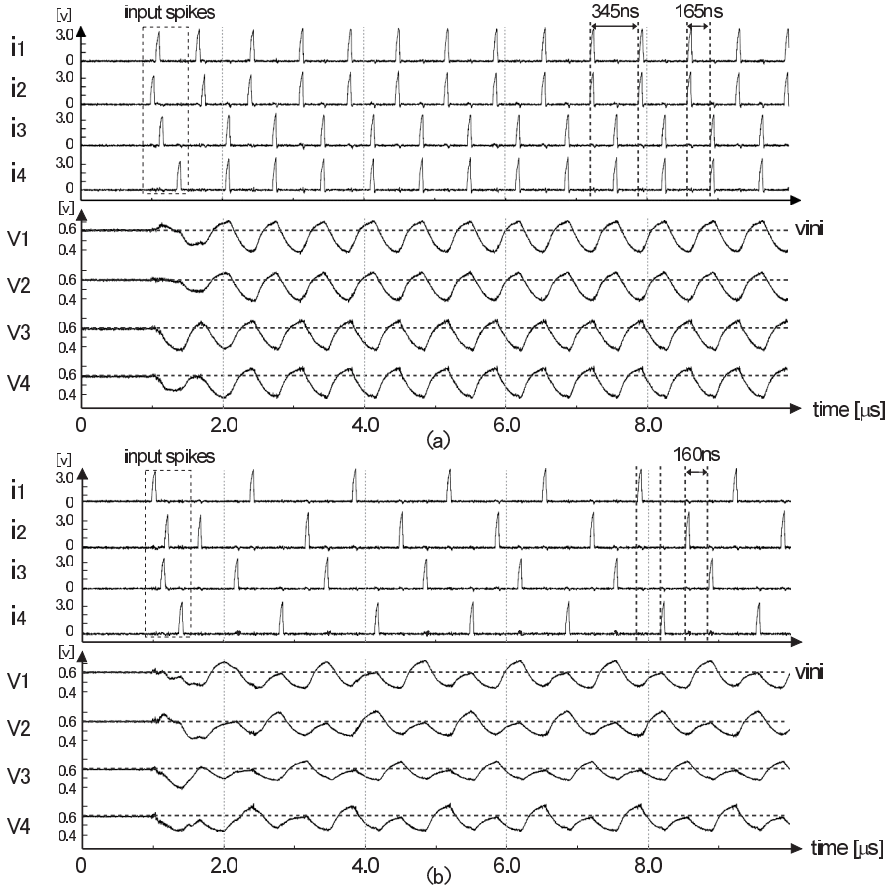

Fig. 16 Measurement results of spiking feedback network: (a) a case of synchrony and (b) a case of asynchrony.

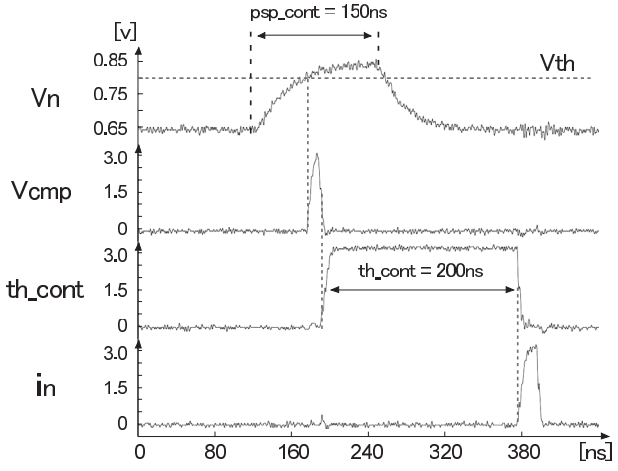

Fig. 17 Measurement results of spiking neuron circuit.

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