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Novel Structure Oriented Compact Model and Scaling Rule for Next Generation Power Semiconductor Devices

次世代パワー半導体用高精度コンパクトモデルの開発とスケーリング則の確立

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Abstract

Power electronics is one of the key technologies to realize a low emission society. Semiconductor power devices, which are the main components of power electronics instruments, are expected to improve in power loss. A lot of research and development have been done especially for IGBTs (Insulated Gate Bipolar Transistor), which are widely used for over 600V class rated voltage, such as EV (Electric Vehicle) and HEV (Hybrid Electric Vehicle). The annual demand for IGBTs is around 2.5 billion dollars annually in 2012, accounting for about 8% of the semiconductor market for Power Management. Its application range has rapidly expanded, from IH (Induction Heating) cookers, inverter air conditioners, and also high voltage DC transmission (HVDC) devices on behalf of several hundred megawatts of Thyristor. Its market is growing at an annual rate of more than 10%. Devices using new materials such as Gallium Nitride and Silicon Carbide as the next generation power devices have been prototyped. But Silicon devices, including the Silicon IGBTs are considered to be the mainstream for the next few decades due to its material cost and ease of processing.

In the development of IGBT application systems, such as inverters, circuit simulation is used to improve its electrical efficiency and estimate heat loss and noise. A mathematically formulated model called the compact model that reproduces the characteristics of the IGBT, is used in the circuit simulation. But current IGBT compact models do not achieve enough accuracy, especially for latest trench-gate IGBT.

In this study, accurate compact model development for the trench gate IGBT was achieved for the first time in the world by analyzing in detail the principle operation of the IGBT. The compact model represents high precision characteristics of the device in the simple formula and device structure parameters. This model has been published as a "Quasi-2D MOS-ADE" model. In addition, in the analysis of the compact model, the newly discovered "Scaling Principle" as well as CMOS technology was also present in the power devices. The possibility to realize the miniaturization of next-generation power devices was demonstrated.

In Chapter 1 and Chapter 2, the background and purpose of the study is reviewed. Discuss on the detail the operating mechanism of the IGBT, in particular, the preparation for the construction of the model starts from Chapter 3.

In Chapter 3, a new mathematical expression for the trench-gate IGBT based on the operation of the semiconductor device physics, was established as a compact model. This model makes possible the representation of potential and carrier distribution of the Cathode side with high accuracy. In this model, the current flows are assumed to be separated into

three portions, the electron current and the hole current flowing through the mesa region that is sandwiched between the trenches, and the electron current flowing through the accumulation layer of the gate sidewalls where the current in the device has been represented as an equivalent circuit conventionally. As a result, the distribution of electrons and holes of IGBT can be expressed accurately. In addition, because it is formulated in the device structure parameters only, any extraction works for fitting parameters are not necessary.

In Chapter 4, the established compact model was verified for 600V, 1200V, and 3.3kV rated IGBT's. The carrier distribution profiles and I-V characteristics calculated by the compact model and TCAD device simulation were compared. As a result of the verification, consistent with high precision characteristics and carrier density distribution, the validity of the model was shown. TCAD simulation needs time-consuming calculation of more than a million times compared to the compact model because it solves all of the basic equations of the semiconductor.

In Chapter 5, a scaling principle for the IGBT was established for the first time. The principle was founded from the analysis of the "Quasi-2D MOS-ADE" model. A roadmap for achieving the next generation power devices was revealed by the principle. Conventional IGBT uses 0.5 to 1 micron design rules, and miniaturization was not considered. The "scaling principle" opened the way to the adoption of large sized wafers and high resolution semiconductor processes, and showed an explicit direction to the realization of next-generation power devices that improve the production and performance.

In Chapter 6, the future of IGBT was discussed based on the knowledge gained in this study.

和文要旨

省エネルギー社会の実現に向け、パワーエレクトロニクス技術には多くの期待が寄せられている。特に、パワーエレクトロニクス機器のキーコンポーネントであるパワーデバイスには一層の低損失化が求められている。中でも、電気自動車やハイブリッド自動車などに搭載されている耐圧 600V 以上のパワーデバイスとして広く用いられている IGBT (Insulated Gate Bipolar Transistor) に対しては多くの技術開発がなされ、低損失化を実現している。2012 年現在、IGBT は年間 2500 億円程度の需要があり、パワーマネジメント関連半導体の約 8%の市場を占めている。また、適用範囲も急拡大しており、エアコンや IH 調理器のインバータから、最近では、サイリスタに代わって数百メガワットの直流送電 (HVDC) にまで用いられるようになってきた。この結果年率 10%以上の勢いで市場が拡大している。次世代のパワーデバイスとして炭化シリコンや窒化ガリウムといった新素材を使用するデバイスが提案および試作されているが、加工容易性や材料コストなどの点から今後数十年はシリコン IGBT をはじめとするシリコンデバイスが主流であると考えられる。

インバータなど、IGBT の応用システムの開発では、発生する熱損失やノイズ等を事前に回路シミュレーションにより見積ることで開発効率を改善してきた。このようなシミュレーションでは IGBT 特性を再現するコンパクトモデルと呼ばれる数式モデルが用いられている。しかし現状の IGBT コンパクトモデルはデバイス特性を十分に表現できず、特に最新のトレンチゲート型 IGBT 構造への適用では精度の点で課題が大きかった。

本研究では、IGBT の動作原理を詳細に分析することにより、最新のトレンチゲート型 IGBT に対応したコンパクトモデルを開発し、素子構造パラメータと単純な数式で素子の特性を高精度に表現することに世界で初めて成功した。本モデルは「Quasi-2D MOS-ADE」モデルとして公表している。また、本コンパクトモデルによる解析で、パワーデバイスでも LSI と同様に「スケーリング則」が存在することを新たに発見し、次世代パワーデバイスが微細化により実現可能であることを明らかにした。

第 1 章、第 2 章では、研究の背景と目的を述べた。特に IGBT の動作メカニズムを詳細に論じ、第 3 章以降のモデル式構築の準備とした。

第 3 章では、トレンチゲート型 IGBT の動作を半導体デバイス物理に基づいた新たな数式表現を考案し、コンパクトモデルとして確立した。本モデルは、カソード側のポテンシャルおよびキャリア分布を高い精度で表現することを可能とした。具体的には、従来は等価回路として表現されていた素子内の電流を、トレンチで挟まれたメサ部分を流れる電子電流およびホール電流と、ゲート側壁の蓄積層を流れる電子電流との 3 つに分離して表現したことが特徴であり、その結果 IGBT 内の電

子およびホールの分布を正確に表すことに成功した。さらに、素子構造パラメータのみで定式化されているため、従来必要であったフィッティングパラメータの抽出作業が完全に不要となり、回路シミュレーションの自動化への道を開いた。

第 4 章では、コンパクトモデルの妥当性の検証を行った。600V, 1200V, 3.3kV の 3 種類の耐圧の IGBT をサンプルとし、半導体の基本方程式をすべて解く TCAD (デバイスシミュレーション) の結果と本コンパクトモデルの結果を比較した。検証の結果、特性およびキャリア密度分布が高い精度で一致し、モデルの妥当性が示された。なお TCAD では、本コンパクトモデルに比べ十万倍以上の計算時間を要する。

第 5 章では、IGBT のスケーリング則を世界で初めて確立した。提案した「Quasi-2D MOS-ADE」モデル式による分析から IGBT 技術における「スケーリング則」の存在を発見し、次世代パワーデバイス実現のロードマップを明らかにした。従来、IGBT では 0.5〜1 ミクロン程度のデザインルールが採用されており、微細化は不可能であると判断されてきた。今回明らかにした「スケーリング則」により、微細半導体の工程と大口径ウェーハの採用への道が開け、性能と量産性を向上した次世代パワーデバイス実現への方向性を明示した。

第 6 章では、得られた知見を元に IGBT の将来像を議論した。大口径ウェーハへの展開、および微細 CMOS プロセスとの互換性による、量産性が高く高品質な IGBT 製品の実現に関し、素子構造の例や半導体プロセスの詳細、さらにパッケージなどの周辺技術も交えて技術開発の方向性を示した。

1 Background

1.1 What's IGBT

Power device is a category of semiconductor devices. It is widely used for electrical power conversion, for example, DC voltage converter and DC to AC converter, so called inverter. Device type is chosen by operating frequency and output power capacity. For Silicon device, the cover area for each device type is summarized in Figure 1.

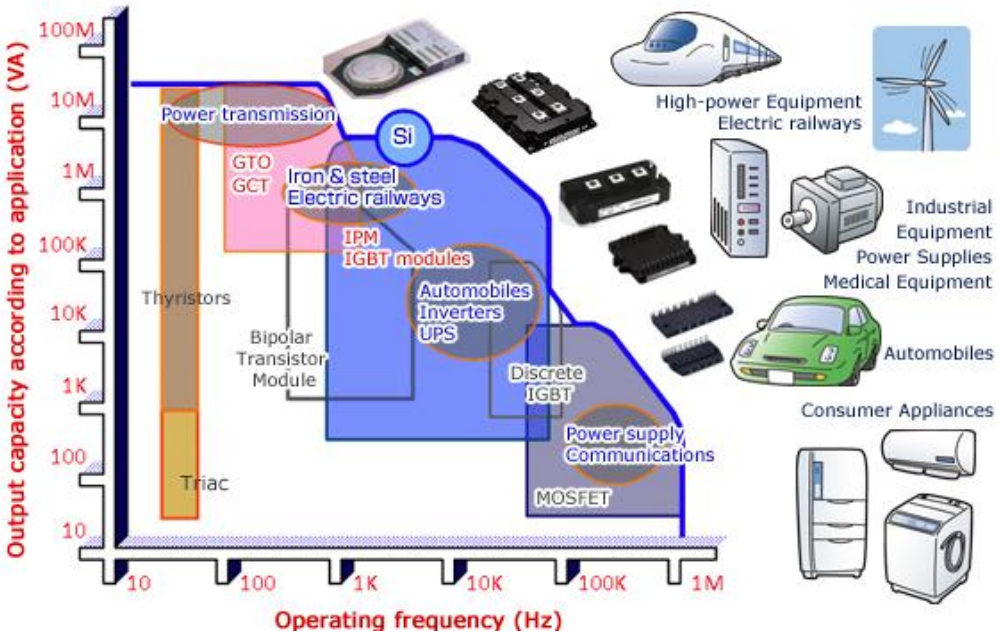


Figure 1. Cover area for various power devices [1].

MOSFET, including vertical MOSFET (Power MOSFET) and lateral diffused MOSFET (LDMOSFET), covers lowest power capability and fastest operating frequency area. MOSFET is unipolar device and its on-state resistance depends on the rated voltage because higher rated voltage needs thicker region with lower doping concentration to expand depletion layer to support the voltage. In result, Power MOSFET has clearly performance limit between rated voltage and on-state resistance as called “Silicon limit”. With Silicon material, the rated voltage is actually limited up to 600V due to high on-state resistance. By using Silicon Carbide material, the limitation expands to higher rated voltage area due to wider band gap than Silicon. However Silicon material is considered as major

material for next several decades due to the material cost and the fabrication process cost, where a lot of research and development for Silicon Carbide device are performed by device companies and research institutes.

IGBT (Insulated Gate Bipolar Transistor) is bipolar device and it realizes lower on-state voltage drop even with higher rated voltage than Power MOSFET by storing much carriers, electrons and holes, in thicker and higher resistivity region than Power MOSFET. On the other hand switching speed is lower than Power MOSFET due to the stored carrier. So IGBT is applied for 1 kHz to 100 kHz frequency and 1kVA to 10MVA power capacity, especially rated voltage of 600V to 4.5kV.

In larger output capacity area than IGBT, Thyristor and GTO (Gate Turn-off Thyristor) are still used due to lower on-state voltage drop than IGBT. But these devices have disadvantages that their control circuits require large displacement and power consumption of the circuit is relatively large because these devices are current controlled. IGBT is MOS controlled device and power consumption for gate drive is very small. In future, Thyristor and GTO should be replaced by improved Silicon IGBT, Silicon Carbide Power MOSFET or Silicon Carbide IGBT.

1.2 Applications and market trends

There is wide range of applications for IGBT. Especially motor control is most major field for IGBT, such as factory robot, electric train, electric vehicle (EV) and hybrid electric vehicle (HEV), air conditioner, and other home appliances. A typical motor control circuit is shown in Figure 2. The circuit converts three phase AC power to three phase AC power with arbitrary frequency and voltage to drive induction motor (IM). Once three phase AC input is converted to DC by diode bridge (“Rectifier” part of Figure 2), then the DC power is converted to AC by six IGBT chips (“Inverter” part of Figure 2). In general the circuit is simply called as “Inverter”. The circuit enables to control induction motor or synchronous motor with arbitrary speed and torque so called “VVVF (Variable Voltage and Variable Frequency) inverter”.

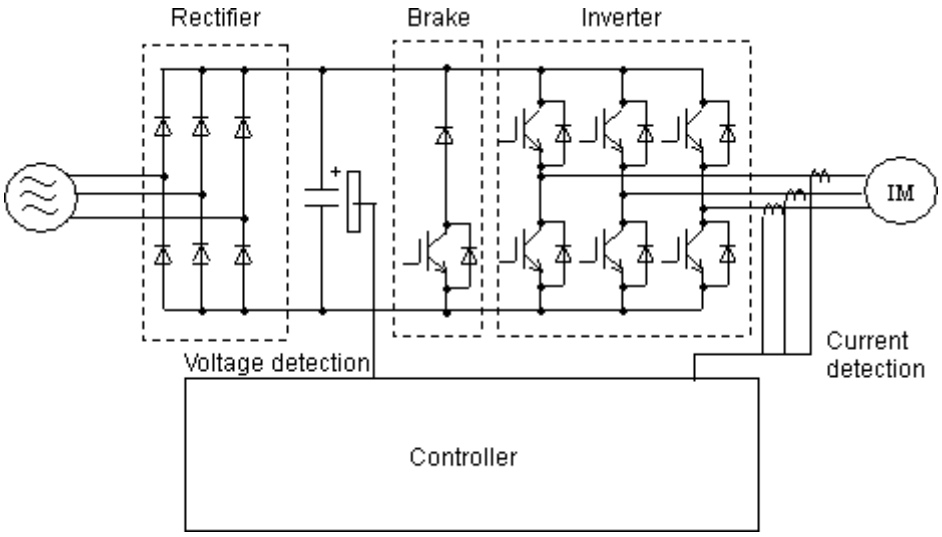


Figure 2. Motor control circuit example [2]. Six IGBT chips on “Inverter” bridge convert to three phase AC power with arbitrary frequency and voltage.

Several types of package are desined for IGBT depends on its application and power capacity. For example, 6-in-1 (Six devices in a package) type has an inverter circuit with six IGBTs and six diodes as “Inverter” section in Figure 2. 2-in-1 (Two devices in a package) type has an arm in the inverter. Typical 2-in-1 packages are shown in Figure 3.

Figure 3. Photograph of IGBT modules [1].

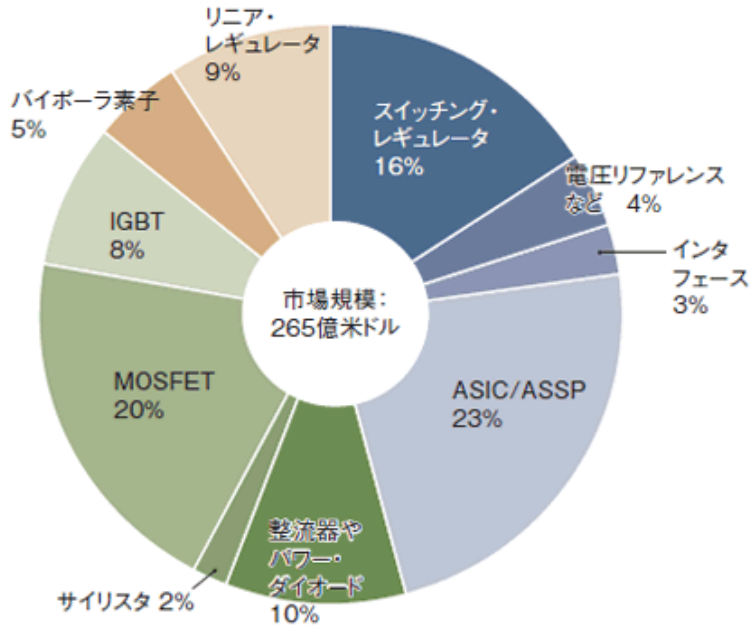


Figure 4. Market share for each power devices [3]. IGBT has 8% of total power device market.

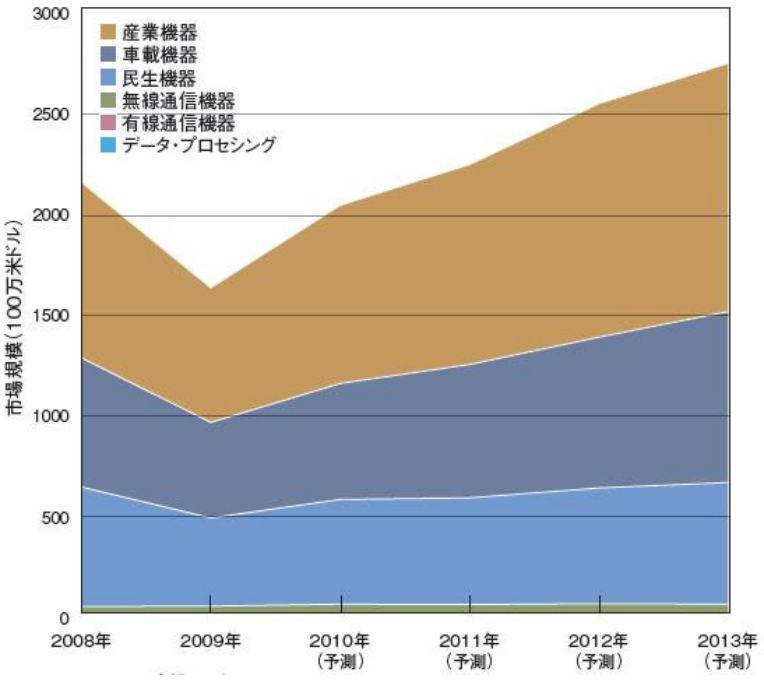


Figure 5. Market trend for IGBT [3]. Vertical axis shows market share in Million US$. Market is shared by mainly Industrial equipment (brown), Automotive applications (dark blue) and Consumer electronics (light blue).

IGBT market shares 8% of total power device market as shown in Figure 4. The market is forecasted to expand about 10% by a year as shown in Figure 5. One market estimated to grow a lot is China. China's government has encouraged fast growth in the photovoltaic (PV) market as part of its long-term new energy development plan [4]. To that end, total installations in China reached 1GigaWatt in capacity in 2010. It is half of the Chinese government's original 2015 target. IGBT should be used for the inverter to change the power from photovoltaic cell (DC) to consumer power line (AC). Another fastest-growing application for IGBT is in new air conditioners. In order to encourage a shift to higher efficiency and power savings in air conditioning equipment, the Chinese government released a new standard last year for room air conditioners. To support the adoption and higher penetration rates of new air conditioners, the government has required that only air conditioners able to meet higher energy efficiency standards will receive financial subsidies. IGBT also should be used for the inverter to drive the compressor with high energy efficiency.

1.3 Issues: Compact Modeling and Process Compatibility

As described in previous section, IGBT is widely used for power electronics industries. The demand of market is also high. In this dissertation, two topics will be discussed as current issues and their solutions will be given.

1.3.1 Compact Modeling

Higher system level electrical efficiency and higher reliability are required continuously in IGBT applications. It means system level optimization is strongly needed. Accurate and fast simulation environment using simple mathematical device model, as called compact model, is desired with capability for wide range of power and device temperature. In the other word, simple and accurate IGBT compact model is required to perform system simulation from medium to high power applications.

Basically, electrical characteristics for IGBT are more complicated than MOSFET that has simply resistive forward characteristic. The key point to represent IGBT's electrical characteristics should be reproducing the stored carrier distribution in high resistivity region because it affects total loss of the device, i.e. both on-state voltage drop and turn-off loss. Physical approach should be better to cover such feature and wide range of device temperature.

Existing IGBT compact models, such as Hefner model [5], have been widely used in

power electronics system and circuit design as the device has expanded the application from small appliances to EV/HEV and tractions etc. The compact models enable to simulate large scale IGBT inverters and systems for many cycle of switching. Most of the IGBT compact models have been formulated based on the combination of physics based simplified analytical equations, equivalent circuits and behavior models with a number of fitting parameters. As far as the models are used within the predetermined validity confirmed operation range of the models, the circuit simulators effectively show the sufficiently accurate results. Once the condition exceeds the validity confirmed range, such as high temperature condition, the model requires re-fitting of the parameters so as to extend the validity range.

In this dissertation, a device structure based compact model for advanced trench gate IGBTs is proposed. The model is formulated by simple equations based on physical equations for semiconductor. Extreme conditions such as under very low or high temperatures can be covered by the model. And only device structure parameters are used so that no fitting parameters are required.

1.3.2 Scaling principle

CMOS technology on large diameter wafer with high resolution lithography technologies enables to produce various digital circuits with higher performance and lower cost. The innovation is continuing at the pace dictated by Moore's Law as shown in Figure 6. The transistor cell structure becomes laterally smaller and smaller and vertically shallower and shallower. On the other hand, trench gate IGBTs introduce rather deeper trench structure to obtain lower on-state voltage drop and turn-off loss. Trench gate IGBT was firstly proposed in 1987. The cell design had 3um width and 5um depth trench, and 8um unit cell pitch [6]. After that unit cell pitch was miniaturized to 4um [7]. But rather deeper trench is still preferred to performance improvement [8]. The technology has been used for more than 10 years. Further miniaturization has not been believed to contribute IGBT performance improvement. In result, currently process compatibility between CMOS and IGBT is so limited. Manufacturing IGBT in CMOS factory is difficult due to the process uniformity and wafer bowing caused by deep trench. The fact can obstruct to improve IGBT's productivity and performance.

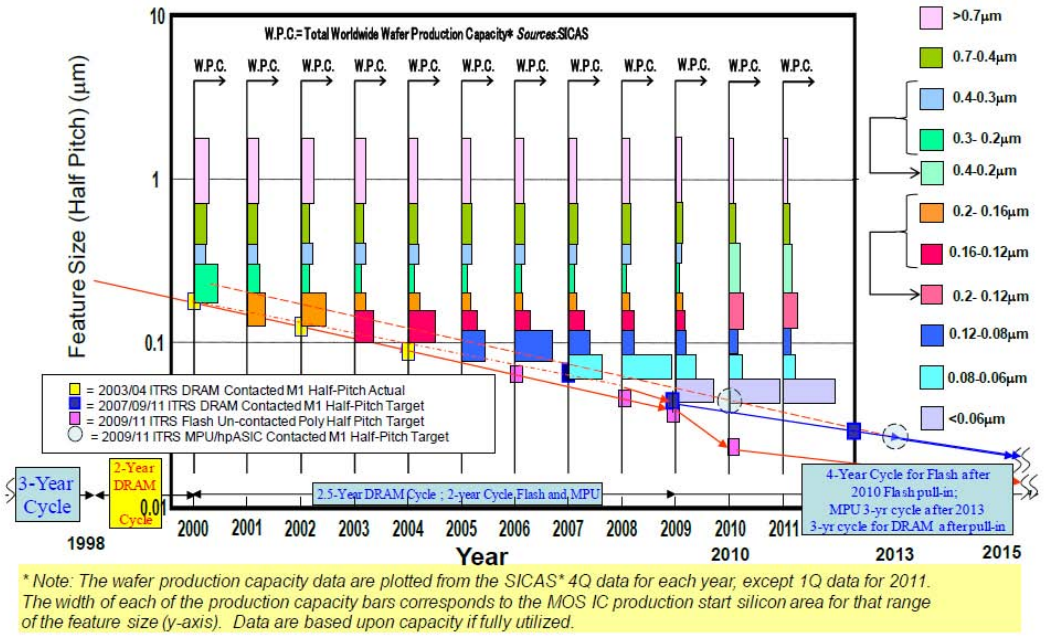


Figure 4 *Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution*[1]

Figure 6. Production technology capacity follwing Moore's law [9].

A scaling principle for IGBT toward shallower structure and smaller thermal budget is also proposed in this dissertation. The principle enables to obtain high manufacturability and better performance that is confirmed by TCAD simulation and theoretically explained by previously proposed compact model. The proposed scaling principle represents a possibility of technology direction and roadmap for future IGBT for improving the device performance consistent with high volume productivity with CMOS compatible large diameter wafer technologies.

1.4 Summary

IGBT is widely used in power electronics system from small appliances to EV/HEV and tractions. The market is forecasted to expand about 10% by a year. But there are some issues in system performance improvement and IGBT's improvement. Firstly, existing compact models have several problems about parameter extraction and validity range. Secondly, IGBT process has poor compatibility with CMOS process that enables to improve performance and manufacturability.

In this dissertation, a device structure based compact model for advanced trench gate

IGBTs will be proposed. And a scaling principle for IGBT toward shallower structure and smaller thermal budget will be also proposed. The compact model has superior characteristics such that the model doesn’t need fitting parameters and parameter extractions, and can adapt for extreme conditions such as under very low or high temperatures. The scaling principle shows a possibility of technology direction and roadmap for future IGBT. It predicts the device performance improvement with high volume productivity with alignment for CMOS wafer process.

2 Objective

In this dissertation, two topics will be discussed as current issue and its solutions will be shown. From section 3 to 4, new compact model will be proposed. The model is structure based such that no fitting parameters are required. It enables to delete parameter extraction step as shown in Figure 7. The model is formulated by simple equations based on physical equations for semiconductor. Extreme conditions such as under very low or high temperatures can be covered by the model without any re-modeling process. The model can be also used for structure optimization because it is based on only the structure parameters, no fitting parameters.

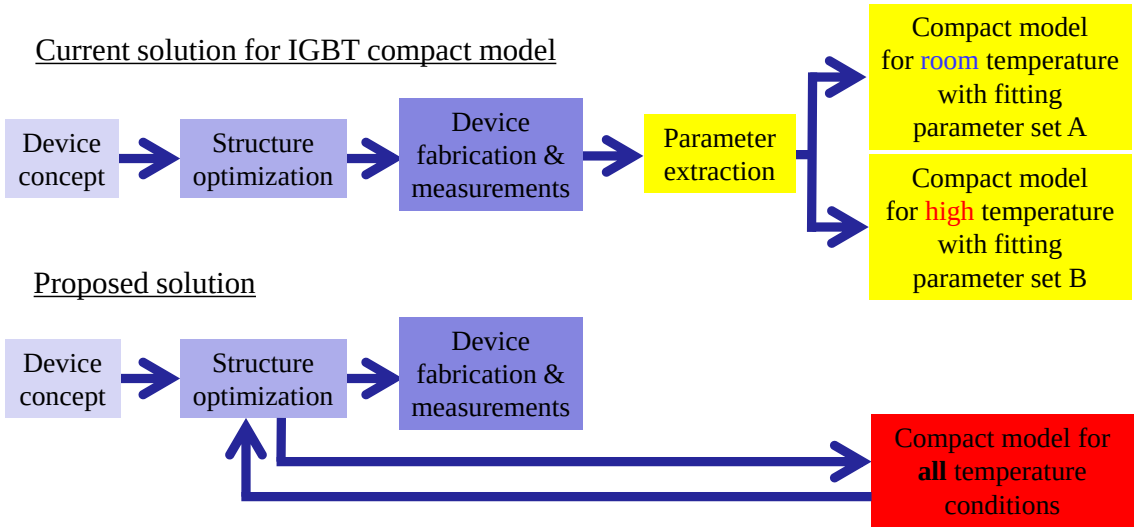


Figure 7. The interpretation of the contribution of this work.

In section 5, a scaling principle for IGBT toward CMOS-like shallower and narrower structure will be proposed. The principle is based on previously proposed compact model formulation. The principle enables to obtain high manufacturability and better performance that is confirmed by TCAD simulation and theoretically explained by previously proposed compact model. The proposed scaling principle represents a possibility of technology direction and roadmap for future IGBT for improving the device performance consistent with high volume productivity with CMOS compatible large diameter wafer technologies.

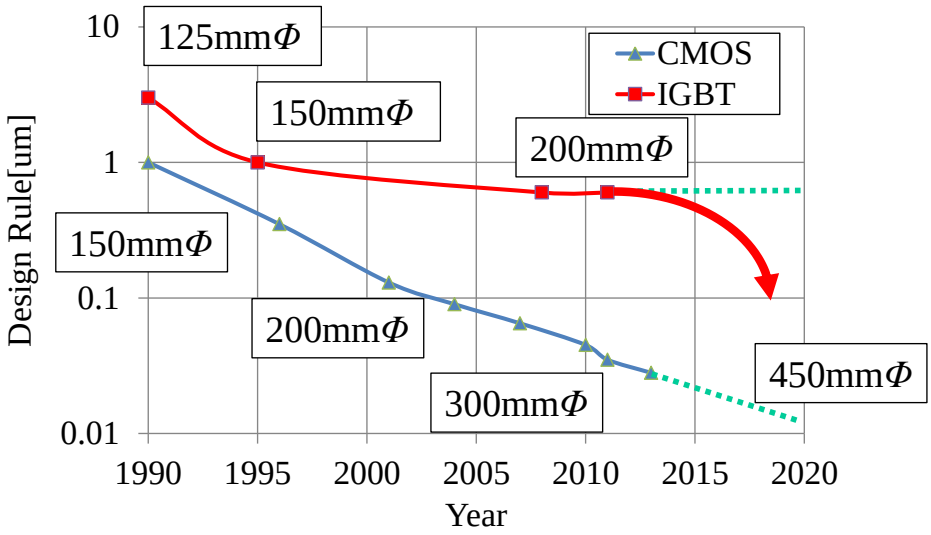


Figure 8. IGBT process direction. Keeping process compatibility with CMOS is needed.

3 Structure Oriented Analytical Modeling for Modern Trench Gate IGBT

3.1 IGBT Basic Operations

Generally, IGBT rated voltage is chosen to more than double of input voltage because the device have to support surge voltage occurred by di/dt and parasitic inductance during turn-off. The relationship between commercial power voltage and device rated voltage is summarized in Table 1. 600V and 1200V rated devices are used for home appliances, air conditioners, automotive and industrial applications. Higher rated voltage devices are used for electric railways, iron/steel rollings, and power plants.

Table 1. Relationship between commercial power voltage and device rated voltage [2].

	Area	Device voltage ratings (V_{CES})			
		600V	1200V	1400V	1700V
Commercial power voltage (Input voltage AC)	Japan	200V 220V	400V 440V		
	U.S.A	208V 230V 240V 246V	460V 480V	575V	
	Europe	200V 220V 230V 240V	346V 350V 380V 400V 415V 440V		690V

A cross sectional view of IGBT is shown in Figure 9. IGBT has three electrodes, Gate, Cathode and Anode. Electrical conduction from Anode to Cathode is established when applying a voltage between Gate to Cathode. With zero or negative gate voltage, the conduction is disappeared and high blocking voltage between Anode and Cathode is realized.

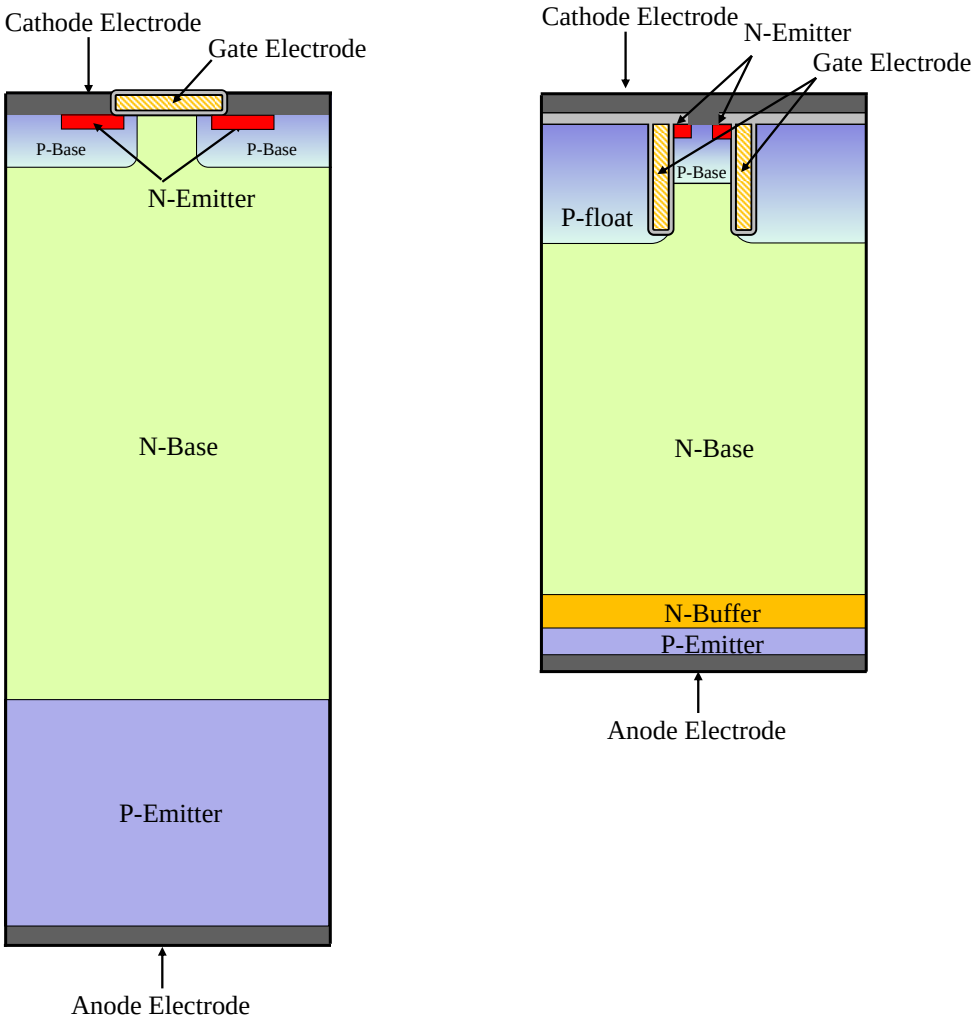


Figure 9. IGBT structure. The left side figure shows old designed Planar gate thick wafer IGBT. The right side figure shows newest Trench gate thin wafer IGBT.

IGBT has basically four doping layers, N-Base, P-Base, N-Emitter and P-Emitter. MOS gate is formed beside P-Base to establish electron conduction between N-Base and N-Emitter. In conduction mode, applied gate voltage creates electron channel beside MOS gate oxide. And applied forward voltage from Anode to Cathode makes IGBT act as PiN diode. Electron injection from N-Emitter to N-Base via MOS gate channel, and hole injection from P-Emitter to N-Base are occurred simultaneously.

During the conduction mode, N-Base conduction resistance is kept as very low because stored carrier density of N-Base is very higher as 100x or 1000x than N-Base doping concentration. So, N-Base carrier concentration exceeds 1e16cm^{-2} where N-Base

doping concentration is chosen for 1e13cm^{-2} to 1e14cm^{-2} depends on rated voltage. This phenomenon is most different point of MOSFET's conduction mode which carrier concentration is kept as doping concentration. The stored carriers form distribution profiles in N-Base as shown in Figure 10. The densities for electron and hole are almost same due to keep charge neutrality, as called "conductive modulation".

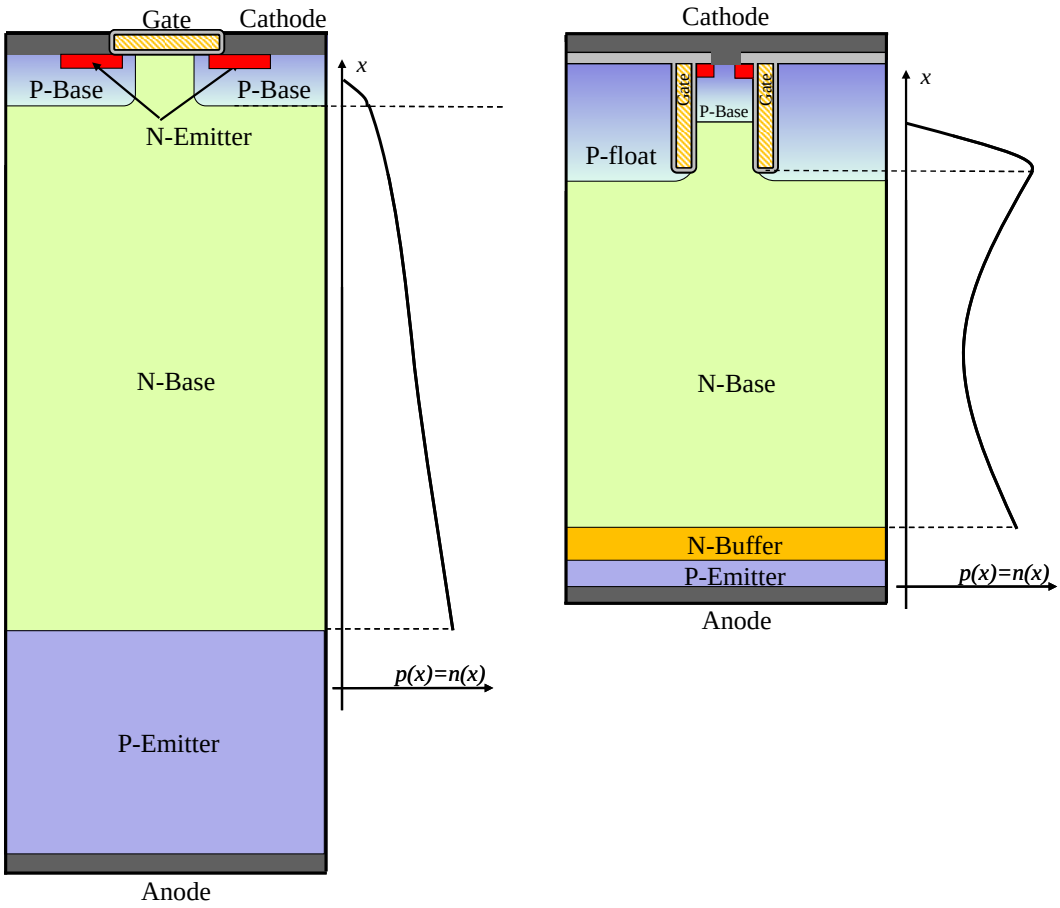


Figure 10. Carrier distribution for conduction mode. Electron and hole form same distribution in N-Base region. The left side figure shows Planar gate IGBT. The right side figure shows Trench gate IGBT. Carrier distribution profile is different.

On-state carrier distribution profile strongly affects power loss of IGBT. IGBT's conduction loss consists of MOS channel resistance, built-in potential and N-Base conduction resistance where MOSFET on-state resistance simply consists of MOS channel resistance and N-Base conduction resistance that clearly depends on N-Base doping concentration. N-Base conduction resistance of IGBT is dominant of conduction loss

especially high rated voltage devices which have thick N-Base region. Turn-off loss also depends on stored carrier because turn-off is exactly exhausting operation for stored carrier. So basically IGBT has a trade-off relationship between conduction loss and turn-off loss, i.e. higher stored carrier enables lower conduction loss but also makes larger turn-off loss. Improvement for the trade-off relationship is most important point for IGBT development.

In off state, i.e. Gate is biased zero or negative voltage against Cathode, applied Anode voltage makes the junction between P-Base and N-Base as reversely biased condition and depletion layer is formed in N-Base. It is completely same as the state of MOSFET. In punch-through (PT) type IGBT, the extension of the depletion layer is blocked by additional N-Buffer layer as shown in the left side of Figure 11. In non-punch-through (NPT) type IGBT, the depletion layer is extended in thicker N-Base as shown in the right side of Figure 11. N-Base doping concentration and thickness are designed to keep rated voltage. For example to obtain rated voltage as 600V, N-Base doping concentration should be around $1.5x10^{14}cm^{-3}$ and the thickness should be 100um for NPT-IGBT [10] [11] and 60um for PT-IGBT [12].

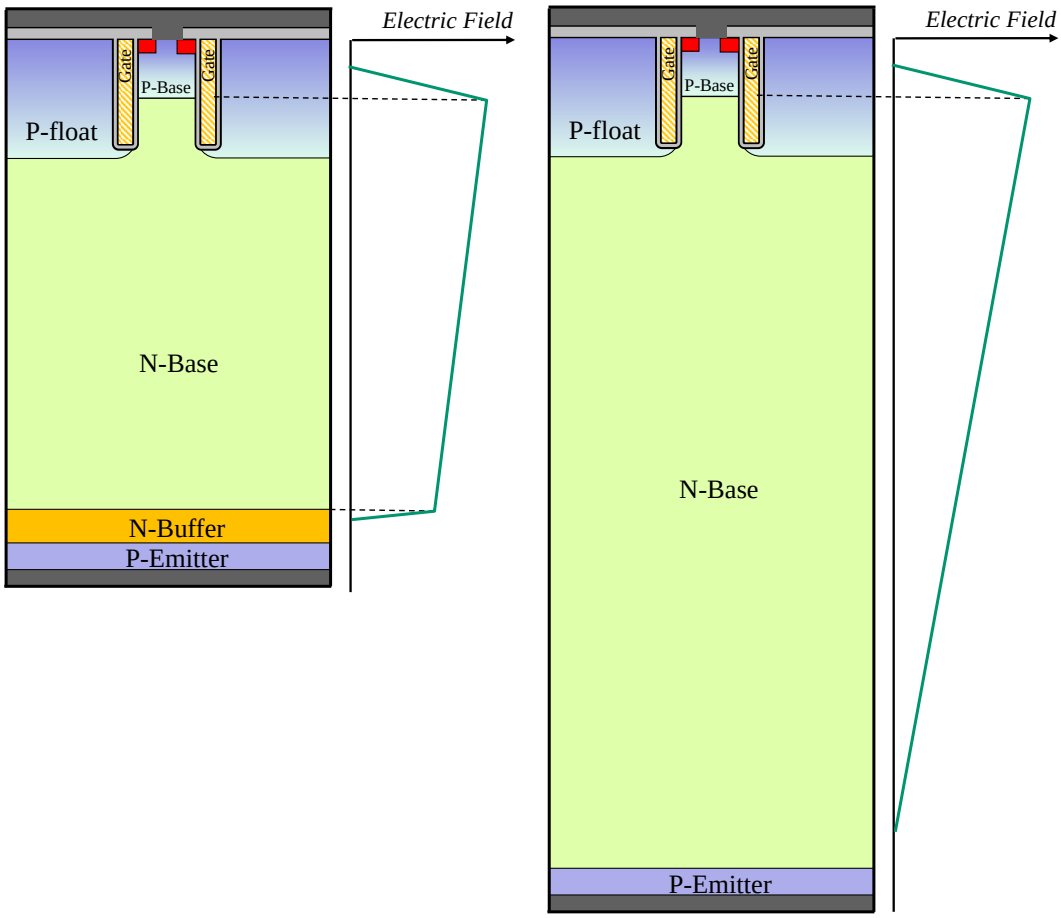


Figure 11. Electric field distribution in off state (left: PT-IGBT, right: NPT-IGBT).

3.2 Modeling Concept

A lot of researches were performed to improve the trade-off relationship between on-state voltage drop and turn-off loss. After that a lot of Cathode designs, such as IEGT (Injection Enhancement Gate Transistor) or other injection enhancement structures, were proposed to control the carrier distribution profile and improve the trade-off relationship [13] [14] [15] [16] [17] [18] [19] [20]. And low injection efficiency Anode design is commonly used for latest IGBT to suppress parasitic operation during turn-off [10] [12] [14] [21] [22] [23] [24]. By considering these technological trends, three main modeling concepts were found as following.

- Accurate on-state carrier distribution realized: the model aims to realize accurate

N-Base carrier distribution. On-state carrier distribution in N-Base is most important point to describe IGBT characteristics accurately, especially on-state voltage drop *Vce(sat)* and turn-off loss Eoff.

- Physical based: the model formulation is based on basic semiconductor equations and some additional physical equations. It leads an advantage that the model can apply for wide range of structure and temperature with high accuracy.
- Structure oriented: the model parameters consist of only structure parameters. No fitting parameters are needed. No parameter extraction work is required in result.

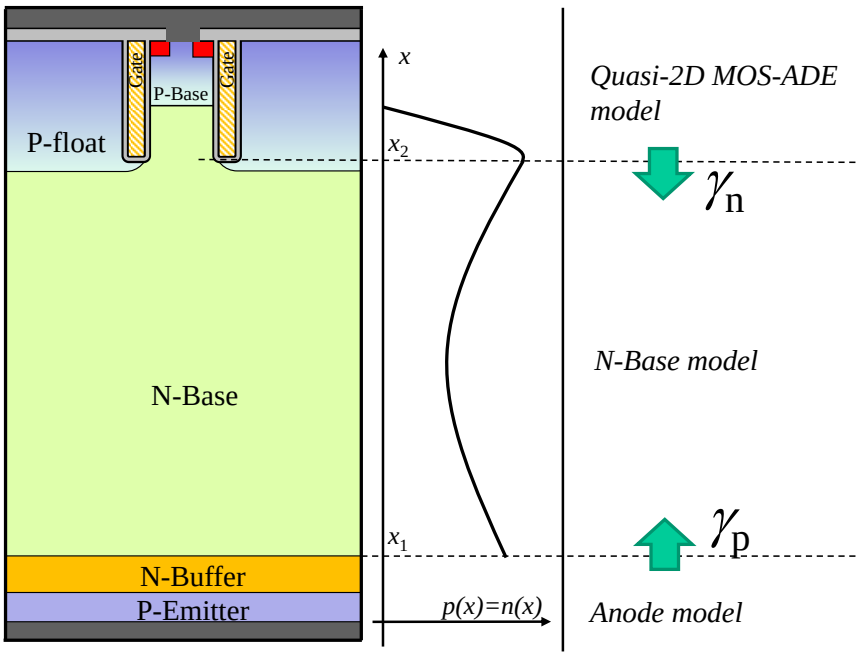


Figure 12. Modeling structure.

Proposed model is formed by three parts as shown in Figure 12. The first is for Cathode side structure named "Quasi-2D MOS-ADE model". Electron injection efficiency γ_n from Cathode side to N-Base can be calculated by the structure parameters and current density. γ_n is defined as

$$\gamma_n = \frac{J_n(x_2)}{J} \qquad (1)$$

where $J_n(x_2)$ is electron current density at Cathode side N-Base edge, $x = x_2$ in Figure 12. And J is total current density. The part covers for trench gate IGBT and IEGT

structures. These structures are widely used to improve trade-off relationship between on-state voltage drop and turn-off loss by injection enhancement effect.

The second is for Anode side structure. Hole injection efficiency γ_p from Anode side to N-Base can be calculated by the structure parameters and current density. γ_p is defined as

$$\gamma_p = \frac{J_p(x_1)}{J} \qquad (2)$$

where $J_p(x_1)$ is hole current density at Anode side N-Base edge, $x = x_1$ in Figure 12. The model covers thin wafer punch-through type IGBT which has shallow P-Emitter layer and shallow N-Buffer layer, called "Field Stop IGBT", and thin wafer non-punch-through type IGBT which has only shallow P-Emitter layer. Shallow P-Emitter design is widely used for various voltage range of IGBT to suppress parasitic operation during turn-off period.

The last part is for N-base structure. Carrier distribution profile for electron and hole can be calculated by the structure parameters, current density, and injection efficiencies from Cathode side and Anode side.

In result, the model can be applied for the combination of trench gate and punch-through or non-punch-through structure with shallow doping layers. It covers various latest IGBT structures proposed by power device manufacturers.

3.3 Quasi-2D MOS-ADE Model

Proposed Cathode side formulation is named as "Quasi-2D MOS-ADE model". The model formulates the relationship between Cathode side structure parameters and electron injection efficiency for trench gate IGBT. The injection efficiency will be used to calculate N-Base carrier distribution.

The main idea of the model is that the electron current flowing from MOS channel is divided to two paths as shown in Figure 13. One is flowing in mesa region keeping same carrier concentration of hole by "conductive modulation" and it holds ADE (Ambipolar Diffusion Equation). The other is flowing along trench gate accumulation layer. In this model, the carrier distributions in mesa region are assumed such that carrier concentrations are constant for horizontal direction, i.e., one-dimensional carrier distribution is assumed in mesa region. For vertical direction, the quasi-Fermi potential for electron $\emptyset_n(x)$ affects to electron flow of trench gate and mesa region. No carrier recombination is also assumed in

mesa region.

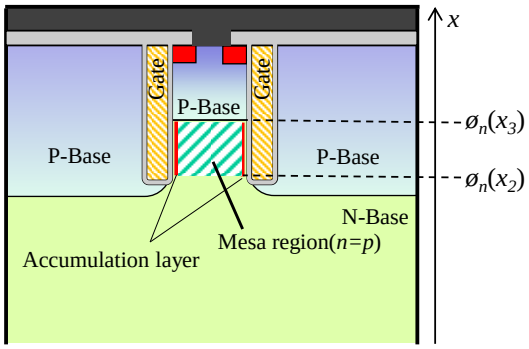


Figure 13. The main idea of the model. Current flow paths are assumed to accumulation layer and mesa region.

This part can be calculated by ADE with considering electron current along the accumulation layer of the trench MOS gate as a function of vertical position. ADE is delivered by general current equation for semiconductor.

$$J_n(x) = q\mu_n n(x)E(x) + qD_n\frac{dn}{dx} \quad (3)$$

$$J_p(x) = q\mu_p p(x)E(x) - qD_p\frac{dp}{dx} \quad (4)$$

With Einstein's relation, they can be arranged to following.

$$J_n(x) = q\mu_n n(x)E(x) + kT\mu_n\frac{dn}{dx} \quad (5)$$

$$J_p(x) = q\mu_p p(x)E(x) - kT\mu_p\frac{dp}{dx} \quad (6)$$

In “conductive modulation” condition, $n = p$ can be assumed. Equation (6) is modified to

$$J_p(x) = q\mu_p n(x)E(x) - kT\mu_p\frac{dn}{dx} \quad (7)$$

From (5) and (7),

$$\mu_p J_n(x) - \mu_n J_p(x) = 2\mu_p \mu_n kT \frac{dn}{dx} \quad (8)$$

Equation (8) forms the relationship between the gradient of carrier density and current densities for electron and hole.

On the other hand, the electron current flowing along the accumulation layer I_n^{acc} can be calculated by the electron mobility and the accumulated carrier density of MOS gate.

$$I_n^{acc}(x) = -\sigma_{acc} \frac{d\emptyset_n}{dx} \quad (9)$$

Where $\emptyset_n(x)$ is electron quasi-Fermi potential along mesa region. σ_{acc} is sheet conductance for the accumulation layer. So,

$$\sigma_{acc} = \mu_{acc} Q_{acc} \quad (10)$$

$$Q_{acc} = \varepsilon_{ox} \frac{V_{ge}}{T_{ox}} \quad (11)$$

where μ_{acc} and Q_{acc} are electron mobility and charge density for the accumulation layer, respectively. ε_{ox}, V_{ge} and T_{ox} are epsilon of the gate oxide, gate voltage and gate oxide thickness, respectively. μ_{acc} is degraded than bulk mobility due to carrier interaction with the Silicon/Oxide interface by high transverse electric field. Several degradation models were proposed [25] [26] [27] [28].

The relationship of current elements between mesa region and N-Base is shown in Figure 14. *W* and *S* are half of cell pitch and half of mesa width, respectively.

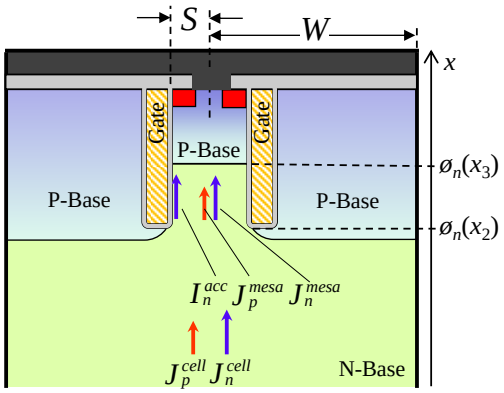


Figure 14. Current elements in Trench structure

Total hole current is kept as constant at the boundary between N-Base and mesa region due to assumed no recombination. Following equation can be formed.

$$WJ_p^{cell}(x_2) = SJ_p^{mesa}(x) \tag{12}$$

Total electron current is kept as constant at the boundary between N-Base and sum of mesa region and accumulation layer. Following equation can be formed for arbitrary *x*,

$$WJ_n^{cell}(x_2) = I_n^{acc}(x) + SJ_n^{mesa}(x) \tag{13}$$

$$J_n^{mesa}(x) = -q\mu_n n(x)\frac{d\emptyset_n}{dx} \tag{14}$$

By (9) and (14), $\frac{d\emptyset_n}{dx}$ can be canceled as

$$J_n^{mesa}(x) = q\mu_n n(x)\frac{I_n^{acc}(x)}{\sigma_{acc}} \tag{15}$$

From (13) and (15), J_n^{mesa} can be formed as

$$J_n^{mesa}(x) = \frac{\sigma_{mesa}(n(x))}{\sigma_{acc} + \sigma_{mesa}(n(x))}\frac{W}{S}J_n^{cell}(x_2) \tag{16}$$

Where

$$\sigma_{mesa}(n(x)) = q\mu_n n(x) S \tag{17}$$

The differential equation which expresses the relationship between structure parameters and electron injection efficiency γ_n, can be obtained by substituting (12) and (16) for (8).

$$\frac{\mu_p}{\mu_n}\left(\frac{\sigma_{mesa}(n(x))}{\sigma_{acc}+\sigma_{mesa}(n(x))}+1\right)\gamma_n - 1 = \frac{2qD_p}{J}\frac{S}{W}\frac{dn}{dx} \tag{18}$$

Re-expanding σ_{mesa} and σ_{acc},

$$\frac{\mu_p}{\mu_n}\left(\left(\frac{\varepsilon_{ox}\mu_{acc}V_{ge}}{T_{ox}q\mu_n n(x)S}+1\right)^{-1}+1\right)\gamma_n - 1 = \frac{2qD_p}{J}\frac{S}{W}\frac{dn}{dx} \tag{19}$$

In conduction mode, the junction of P-Base and N-Base is reversely biased. So the boundary condition of (18) is

$$n(x_3) = 0 \tag{20}$$

3.4 Hole Injection Model for Shallow P-Emitter

Proposed model for Anode structure covers punch-through (PT) type IGBT which has shallow P-Emitter layer and shallow N-Buffer layer, and non-punch-through (NPT) type IGBT which has only shallow P-Emitter layer. No carrier recombination is considered in this model because the thickness of P-Emitter and N-Buffer layers are much shorter than carrier diffusion length. No voltage drops for majority carriers are also considered. Constant doping concentration is assumed for P-Emitter and N-Buffer layers. Not doping profile curve but total doping dose is dominant to calculate γ_p by this model.

3.4.1 NPT model

Firstly NPT type modeling is described. Cross sectional view and carrier distribution profile is shown in Figure 15.

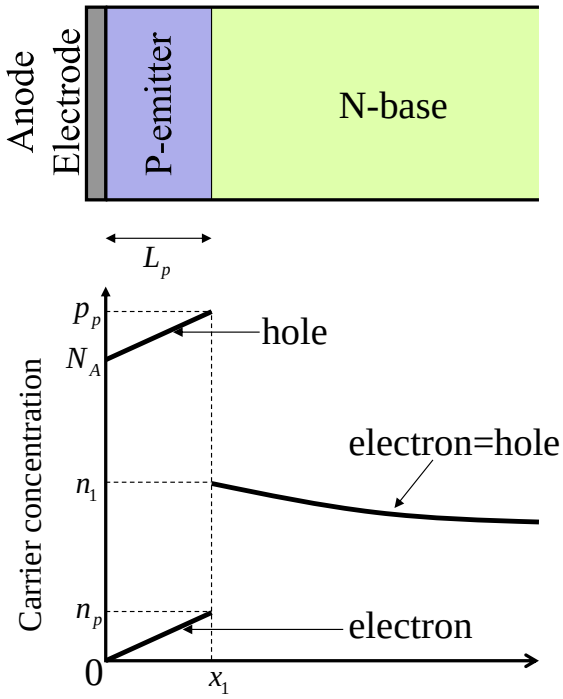


Figure 15. Structure and carrier distribution for NPT-IGBT with shallow P-Emitter

N_A and L_p are P-Emitter doping concentration and thickness, respectively. n_p and p_p, are electron and hole concentration at P-Emitter edge of N-Base side. n_1 is carrier electron and hole concentration at N-Base edge of P-Emitter side. By considering only diffusion current, reversely injected electron from N-Base to P-Emitter can be calculated as following.

$$J_n(x_1) = qD_n \frac{dn}{dx} = qD_n \frac{n_p}{L_p} \tag{21}$$

where D_n is diffusion coefficients for hole and electron, respectively. It can be calculated by carreir lifetimes. Carrier lifetime degradation model due to higher doping concentration should be applied [29] [30] [31] [32].

By p-n power continuity across N-Base / P-Emitter junction and charge neutrality in P-Emitter,

$$n_p = \frac{n_1^2}{p_p} = \frac{n_1^2}{n_p + N_A} \tag{22}$$

By solving the quadratic equation,

$$n_p = \frac{-N_A \pm \sqrt{N_A^2 + 4n_1^2}}{2} \tag{23}$$

The electron current density can be obtained by substituting (22) for (20). Only the plus side solution of (22) can be applied.

$$J_n(x_1) = qD_n \frac{-N_A + \sqrt{N_A^2 + 4n_1^2}}{2L_p} \tag{24}$$

The relationship between structure parameters and hole injection efficiency γ_p, can be obtained by (2) and (23)

$$\gamma_p = 1 - qD_n \frac{-N_A + \sqrt{N_A^2 + 4n_1^2}}{2JL_p} \tag{25}$$

3.4.2 PT model

Next, PT type modeling is described. Cross sectional view and carrier distribution profile is shown in Figure 16. N_A, L_p, N_D and L_n are P-emitter concentration, thickness, N-buffer concentration and thickness, respectively.

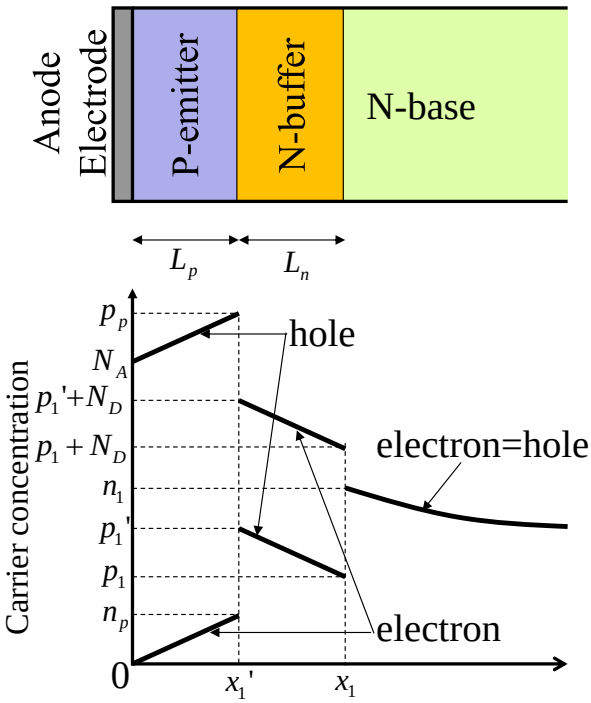


Figure 16. Structure and carrier distribution for PT-IGBT with shallow P-Emitter and shallow N-Buffuer

By considering only diffusion current, the current densities J_n and J_p at N-base edge can be calculated by

$$J_n(x_1) = qD_n\frac{dn}{dx} = qD_n\frac{n_p}{L_p} \tag{26}$$

$$J_p(x_1) = qD_p\frac{dp}{dx} = qD_p\frac{p_1{}' - p_1}{L_n} \tag{27}$$

Following boundary conditions can be obtained by power continuity across P-Emitter / N-Buffer junction and N-Buffer / N-Base boundary.

$$(p_1 + N_D)p_1 = n_1^2 \tag{28}$$

$$p_p n_p = (N_A + n_p)n_p = (p_1' + N_D)p_1' \tag{29}$$

Equations (25)-(28) can be modified with process parameters as following.

$$J_n(x_1) = qD_p \frac{\sqrt{N_D^2 + 4(N_A + n_p)n_p} + \sqrt{N_D^2 + 4n_1^2}}{2L_n} \tag{30}$$

The relationship between structure parameters and hole injection efficiency γ_p, can be obtained by (2) and (29)

$$\gamma_p = 1 - qD_p \frac{\sqrt{N_D^2 + 4(N_A + n_p)n_p} + \sqrt{N_D^2 + 4n_1^2}}{2JL_n} \tag{31}$$

3.5 N-Base Model

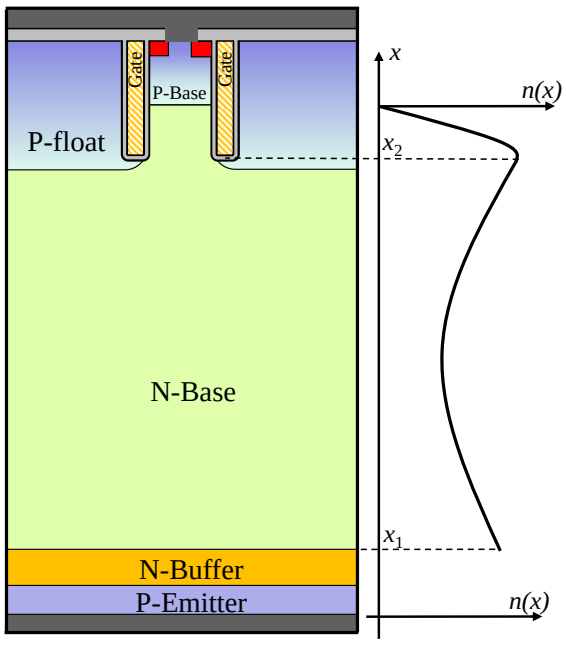


Figure 17 Cross sectional view of Trench gate IGBT

A cross-sectional view of Trench gate IGBT is shown in Figure 17. N-base carrier concentration $n(x)$ can be delevered by carrier transport equations (5)(6) and following continuity equations.

$$\frac{dn}{dt} = -\frac{1}{q}\frac{dJ_n}{dx} + G_n - R_n \tag{32}$$

$$\frac{dp}{dt} = \frac{1}{q}\frac{dJ_p}{dx} + G_p - R_p \tag{33}$$

Where G_n and G_p are generation rate for electron and hole. R_n and R_p are recombination rate for electron and hole. In the model G_n=G_p=0 is assumed. For R_n and R_p, only Shockley–Read–Hall (SRH) recombination is assumed in the model.

$$R_n = R_p = \frac{pn - n_i^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{34}$$

where τ_n and τ_p are carrier lifetime for electron and hole.

$$n_1 = n_i e^{\frac{E_{trap}}{kT}} \tag{35}$$

$$p_1 = n_i e^{\frac{-E_{trap}}{kT}} \tag{36}$$

where E_{trap} is the difference between the defect level and intrinsic level.

In high injection condition, (34) can be approximated as

$$R_n = R_p = \frac{n}{\tau_p + \tau_n} = \frac{n}{\tau} \tag{37}$$

where τ is carrier lifetime in high injection condition.

$$\tau = \tau_p + \tau_n \tag{38}$$

With using τ and n=p, (32) and (33) can be rewritten as

$$\frac{dJ_n}{dx} = -\frac{dJ_p}{dx} = q\left(\frac{n}{\tau} + \frac{dn}{dt}\right) \tag{39}$$

By differentiating (8) with respect to x,

$$\mu_p \frac{dJ_n}{dx} - \mu_n \frac{dJ_p}{dx} = 2\mu_p \mu_n kT \frac{d^2 n}{dx^2} \tag{40}$$

By substituting (39) for (40),

$$q(\mu_p + \mu_n)\left(\frac{n}{\tau} + \frac{dn}{dt}\right) = 2\mu_p \mu_n kT \frac{d^2 n}{dx^2} \tag{41}$$

Finally carrier distribution function $n(x)$ is formed as

$$L_A^2 \frac{d^2 n}{dx^2} = n + \tau \frac{dn}{dt} \tag{42}$$

Where L_A is diffusion length of high injection condition.

$$L_A = \sqrt{\frac{kT}{q} \frac{2\mu_p \mu_n}{\mu_p + \mu_n} \tau} \tag{43}$$

For the steady state conditions, time dependent term is omitted and the solution can be formed as

$$L_A^2 \frac{d^2 n}{dx^2} = n \tag{44}$$

The solution of the differential equation (44) can be

$$n(x) = L_A \frac{-\frac{dn}{dx}(x_1) \cosh\left(\frac{x_2 - x}{L_A}\right) + \frac{dn}{dx}(x_2) \cosh\left(\frac{x - x_1}{L_A}\right)}{\sinh\left(\frac{x_2 - x_1}{L_A}\right)} \tag{45}$$

where x_1 and x_2 are positions of Anode edge and Cathode edge of N-Base region as shown in Figure 17. Equation (45) means that N-Base carrier distribution depends on the differentials of the carrier distribution at both edges.

The differentials of the carrier distribution at N-Base edges can be obtained by (8).

$$\frac{dn}{dt}(x_1) = -\frac{J\left(\gamma_p - \frac{\mu_p}{\mu_p + \mu_n}\right)}{2\frac{\mu_p\mu_n}{\mu_p + \mu_n}kT} \quad (46)$$

$$\frac{dn}{dt}(x_2) = -\frac{J\left(\gamma_n - \frac{\mu_n}{\mu_p + \mu_n}\right)}{2\frac{\mu_p\mu_n}{\mu_p + \mu_n}kT} \quad (47)$$

where γ_p and γ_n are hole injection efficiency at Anode side and electron injection efficiency at Cathode side, respectively.

3.6 Summary

IGBT structure has thick and high resistive N-Base layer. Electron and hole are stored in the layer in conduction mode. The shape of stored carrier concentration profile is most important for IGBT characteristics. To reproduce accurate carrier concentration profile, three models were established. Firstly, "Quasi-2D MOS-ADE" Cathode side model was created to calculate electron injection efficiency from trench gate structure. It can be applied for conventional trench gate structures and injection enhancement structures such as IEGT. Secondly, Anode side model was also created to calculate hole injection efficiency from shallow P-Emitter and N-Buffer structure. It can be applied to for PT-IGBT and NPT-IGBT with shallow P-Emitter and N-Buffer layer. Finally N-Base model is formulated by using Cathode side injection efficiency and Anode side injection efficiency. All models are described by semiconductor basic equations and structure parameters. No fitting parameter is used for proposed model.

4 IGBT Compact Modeling for Wide Range Structure and Temperature

4.1 IGBT Circuit Simulation Environments

In power electronics system development, circuit simulation must be required for system optimization, such as checking output waveforms and estimating power loss and heat generation. Two approaches exist currently, compact model and TCAD (Technology CAD).

On the compact model approach, semiconductor device electrical characteristics are expressed by simple equations. And circuit topology is written as “Netlist” in a text file. Then circuit simulator such as SPICE (Simulation Program with Integrated Circuit Emphasis) solves them. The advantage and disadvantages of this approach is following.

- Computing cost: Calculation time is much shorter than TCAD approach because the number of nodes to be solved is much smaller.
- Capability: The number of circuit nodes and devices can be over 10 million and 9 million, respectively [33]. It is enough to describe power electronics circuit.
- Modeling complexity: Compact model consists of a lot of parameters which stands on physical meaning and for fitting. Parameter extraction is required and parameters strongly affect calculation results.
- Accuracy: Accuracy depends on the quality of the compact model itself and parameter extraction.

On the other approach, calculation by TCAD simulator, semiconductor geometrical structure is written in FEM (Finite Element Method) model with a lot of nodes. The simulator solves the FEM model with a lot of basic semiconductor physical models, and connected circuits. The advantage and disadvantages of this approach is following.

- Computing cost: It consumes much longer calculation time than compact model approach due to large node number for FEM model.
- Capability: The number of the circuit nodes solved with FEM model should be limited by computing cost and convergence issue.
- Modeling complexity: Good quality mesh is necessary to avoid convergence

problem and to get accurate results.

- Accuracy: In general, much better accuracy than compact model approach is realized even if using default physical parameter set. With physical calibration, extremely accurate result can be obtained.

The comparison of these two approaches is summarized in Table 2.

Table 2. Pros and cons of compact model and TCAD approach.

	Compact Model	TCAD
Computing cost	Smaller	Larger
Capability for circuit node	Larger	Smaller
Modeling complexity	Needs parameter extraction	Needs FEM model creation
Accuracy	Depends on the compact model and its parameters	Better

4.2 Previous Research for IGBT Compact Model

A lot of researches were performed for IGBT compact model. Existing models are categorized into three types.

- Physics based model: Based on semiconductor basic equations. Better to express complex characteristics of IGBT.
- Combination model by MOSFET model and Bipolar Transistor model: A limitation exists due to wide base PNP transistor in IGBT. Bipolar Transistor model is designed for narrow base transistors.
- Behavior model: Electrical characteristics are written in the combination of mathematical formula. Once the condition is changed, re-fitting is required.

Two physics based models will be reviewed in this section.

4.2.1 Hefner's Model

Dr. Allen R. Hefner Jr. proposed his first IGBT compact model in 1988 [5]. It was very early because IGBT had been firstly founded as IGR in 1982 and non-latch up IGBT had been produced by Nakagawa in 1985. He wrote his modeling approach in his Ph. D. thesis[1]

[1] A. R. Hefner, "Characterization and Modeling of the Power Insulated Gate Bipolar Transistor." Ph. D. Dissertation, University of Maryland. Ann Arbor, MI: University Microfilms International, 1987.

in 1987. He seemed to research this topic from very early of IGBT history. From the first research, load circuit was considered to calculate device-circuit interaction. Then gate drive condition dependencies also took into account [34]. Implementation for Saber simulator [35] and IG-SPICE [36] were also reported. Furthermore, model extension toward considering self-heating effect [37] and thermal calculation approach on IGBT module [38], were reported. For model validation with load circuit, PWM inverter case [39] and soft switching case [40] were reported.

Hefner model is physics based and the motif structure is NPT-IGBT with thick P-Emitter as shown in Figure 18. High injection efficiency from Anode side and low injection efficiency from Cathode side are assumed to represent Planar gate NPT-IGBT at that time. N-Base on-state carrier distribution profile is linearly decreasing from Anode to Cathode as shown in Figure 19. After that the model was extended to consider N-Buffer layer [41].

Hefner model is still most popular IGBT compact model and widely used in industrial applications. Even in 2009, regarding report was published for pulse power application [42].

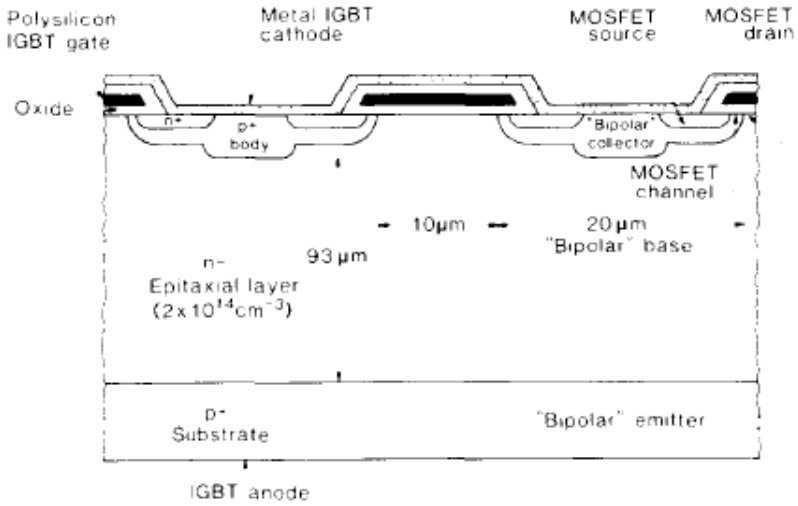


Fig.1. A diagram of two of the many thousand diffused cells of an n-channel IGBT.

Figure 18. IGBT structure for Hefner model [5]. Cell structure is planar gate type. Thick P+ substrate layer exists and act as P-Emitter.

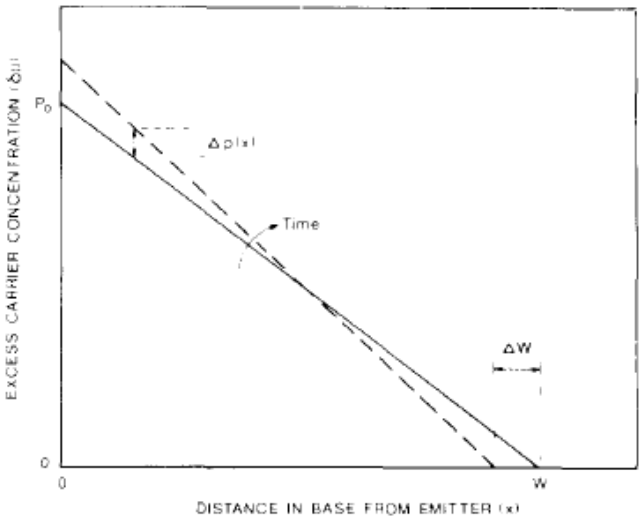


Fig.5. The carrier distribution in the base indicating the change in excess carrier concentration with time due to the moving collector-base depletion edge boundary.

Figure 19. Assumed carrier distribution in Hefner model [5]. Horizontal axis shows distance from P-Emitter. The profile is linearly decreasing from Anode to Cathode.

4.2.2 Palmer & Santi's Model

Dr. Patrick R. Palmer and Associate Prof. Enrico Santi's group in the University of South Carolina proposed several physical models for IGBT and Diode [43] [44] [45]. ADE is solved by Fourier based calculation. The second-order partial differential equation is converted into an infinite set of first-order linear differential equations in time with series coefficients $p_0,\ldots, p_k,\ldots,p_n$ forming equivalent R_kC_k components. In earlier articles the model assumed zero carrier concentration at Cathode side N-Base edge as Hefner's model. From [43], the model started taking into account Cathode side electron injection.

The motif structure is shown in Figure 20. In this model, no electron current in mesa region is assumed. The main idea of Cathode side treatment is considering hole horizontal distribution profile observed by two-dimensional TCAD simulation as shown in Figure 21. The vertical hole current density in mesa region is assumed as linearly increasing from center of mesa to trench edge as shown in Figure 22. And the horizontal hole current density under the trench gate is also assumed as linearly increasing from center of trench gate to trench edge as shown in Figure 22. By these assumption, horizontal hole distribution profile can be calculated. Finally the average of the hole concentration is used for the boundary condition of ADE in N-Base.

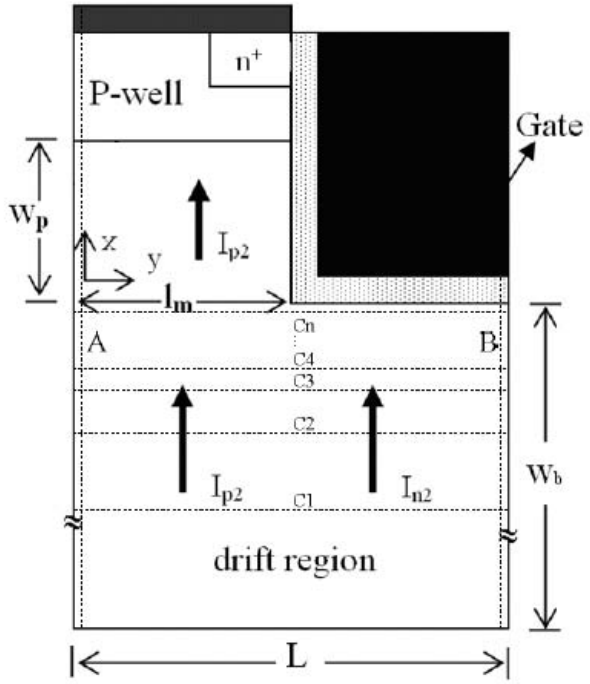


Fig. 4 Trench IGBT structure with physical dimensions. Vertical cutlines A, B and horizontal cutlines C1, C2… Cn are also shown.

Figure 20. Motif structure for Palmer & Santi's model [43]. Cutline C1 to Cn is corresponding hole distribution in Figure 21.

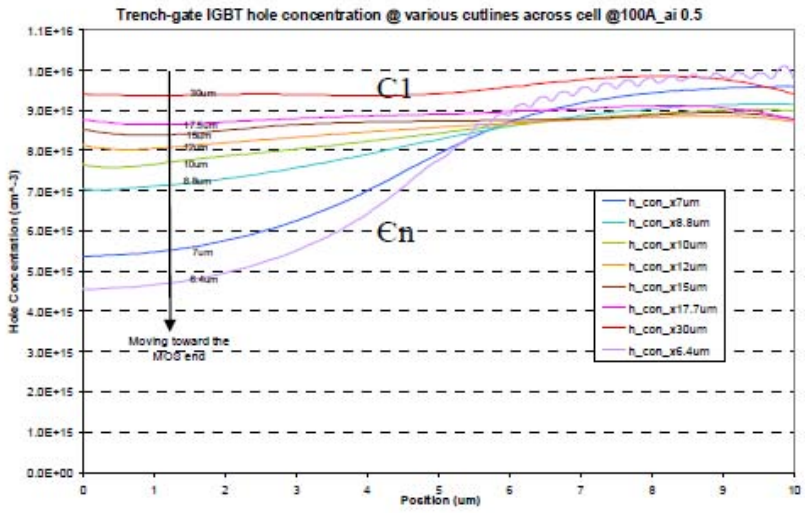


Fig. 6 Carrier concentration along horizontal cutlines C1, C2… Cn defined in Fig. 4.

Figure 21. Hole horizontal distribution calculated by two-dimentional TCAD simulation [43]. A gradient is observed at cutline Cn, just below the trench gate.

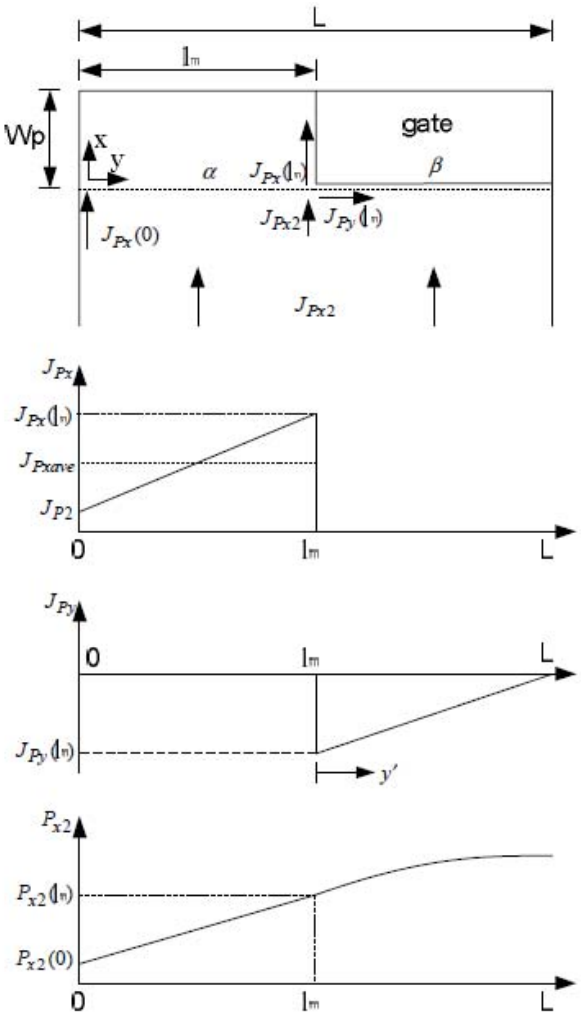


Fig. 17 From top to bottom: hole current flow at the MOS end, hole current density distributions J_{px} and J_{py} along cutlines α and β, and carrier distribution along cutlines α and β.

Figure 22. Assumed hole current distributions and hole distribution for Palmer & Santi's model [43].

4.3 Model Formulation and Implementation

By combining "Quasi-2D MOS-ADE" Cathode model, Anode model, and N-Base model described in previous section, new IGBT compact model is established. By reviewing modeling concept:

- Accurate on-state carrier distribution realized: the model aims to realize accurate N-Base carrier distribution. On-state carrier distribution in N-Base is most important point to describe IGBT characteristics accurately, especially on-state voltage drop *Vce(sat)* and turn-off loss Eoff.
- Physical based: the model formulation is based on basic semiconductor equations and some additional physical equations. It leads an advantage that the model can apply for wide range of structure and temperature with high accuracy.
- Structure oriented: the model parameters consist of only structure parameters. No fitting parameters exist. No parameter extraction work is required in result.

In this implementation, on-state voltage drop is divided to following elements.

- Voltage drop in N-Base
- Voltage drop in mesa region
- Voltage drop in MOS channel
- Built-in potential.

The voltage drop in N-Emitter, P-Emitter and N-Buffer were ignored because these are very small due to very thin layers.

4.3.1 Voltage drop in N-Base

N-Base carrier distribution can be calculated by following equations, Cathode side injection efficiency formed as

$$\frac{\mu_p}{\mu_n}\left(\frac{\sigma_{mesa}(n(x))}{\sigma_{acc}+\sigma_{mesa}(n(x))}+1\right)\gamma_n - 1 = \frac{2qD_p}{J}\frac{S}{W}\frac{dn(x)}{dx} \qquad (48)$$

Anode side injection efficiency formed as,

$$\gamma_p = 1 - qD_n\frac{-N_A+\sqrt{N_A^2+4n_1^2}}{2JL_p} \qquad (49)$$

and N-Base carrier distribution formed as

$$n(x) = L_A\frac{-\frac{dn}{dx}(x_1)\cosh\left(\frac{x_2-x}{L_A}\right)+\frac{dn}{dx}(x_2)\cosh\left(\frac{x-x_1}{L_A}\right)}{\sinh\left(\frac{x_2-x_1}{L_A}\right)} \qquad (50)$$

$$\frac{dn}{dt}(x_1) = -\frac{J\left(\gamma_p - \frac{\mu_p}{\mu_p + \mu_n}\right)}{2\frac{\mu_p\mu_n}{\mu_p + \mu_n}kT} \tag{51}$$

$$\frac{dn}{dt}(x_2) = -\frac{J\left(\gamma_n - \frac{\mu_n}{\mu_p + \mu_n}\right)}{2\frac{\mu_p\mu_n}{\mu_p + \mu_n}kT} \tag{52}$$

The voltage drop in the N-base can be calculated based on the above stored carrier concentration.

$$V_{N-Base} = \frac{\mu_p - \mu_n}{\mu_p + \mu_n} \cdot \frac{kT}{q} \int_{x=x_1}^{x_2} \frac{1}{n}\frac{dn}{dx}dx + \frac{J}{q(\mu_p + \mu_n)} \int_{x=x_1}^{x_2} \frac{1}{n}dx \tag{53}$$

4.3.2 Voltage drop in mesa region

Carrier distribution profile in mesa region can be calculated by

$$\frac{\mu_p}{\mu_n}\left(\frac{\sigma_{mesa}(n(x))}{\sigma_{acc} + \sigma_{mesa}(n(x))} + 1\right)\gamma_n - 1 = \frac{2qD_p}{J}\frac{S}{W}\frac{dn(x)}{dx} \tag{54}$$

The voltage drop in mesa region can be calculated based on the above stored carrier concentration.

$$V_{mesa} = -\frac{J\gamma_n}{q\mu_n} \cdot \frac{W}{S} \int_{x=x_2}^{x_3} \frac{1}{n(x)} \frac{\sigma_{mesa}(n(x))}{\sigma_{acc} + \sigma_{mesa}(n(x))} \frac{dn(x)}{dx} dx \tag{55}$$

where x_3 is the junction position between P-Base and N-Base.

4.3.3 Voltage drop in MOS channel

The voltage drop of the channel can be calculated by power of electron current via MOS gate, which is calculated by Cathode side electron injection efficiency, and channel conductance, which is calculated by surface potential along the channel.

To simplify the model, strong inversion condition is assumed for the channel region. Surface potential $\varphi_S(x)$ can be calculated by following.

$$\varphi_S(x) = 2\varphi_P(x) + V_{ds}(x) \tag{56}$$

where $\varphi_P(x)$ is the difference of intrinsic Fermi potential and P-base Fermi potential. $V_{ds}(x)$ is the potential drop from source side. The charge concentration of gate oxide can be calculated by

$$Q_G(x) = C_{ox}(V_{ge} - \varphi_S(x)) \tag{57}$$

where C_{ox} is the capacitance per unit area of gate oxide, and V_{ge} is gate-emitter voltage. The charge concentration of channel region can be calculated by

$$\begin{aligned} Q_C(x) &= -\big(Q_G(x) + Q_A(x)\big) \\ &= -C_{ox}\Big(V_{ge} - \varphi_S(x)\Big) - Q_A(x) \end{aligned} \tag{58}$$

where $Q_A(x)$ is acceptor concentration of P-Base region. We can modify it by using acceptor concentration of P-Base region $N_A(x)$,

$$\begin{aligned} Q_C(x) = -C_{ox}\big(V_{ge} - (2\varphi_P(x) + V_{ds}(x))\big) \\ + \sqrt{2\varepsilon_{Si}\varepsilon_0(2\varphi_P(x) + V_{ds}(x))qN_A(x)} \end{aligned} \tag{59}$$

Finally the channel conductance can be calculated by

$$\sigma_{channel}(x) = \mu_{channel}(x)Q_C(x) \tag{60}$$

$\mu_{channel}(x)$ is the electron mobility in the channel. As mentioned before, it is much degraded than bulk mobility due to carrier interaction with the Silicon/Oxide interface by high transverse electric field. Degradation model [25] [26] [27] [28] must be applied to estimate accurate $\mu_{channel}(x)$.

4.3.4 Built-in potential

The built-in potential is the difference between quasi-Fermi potential and electro static potential. In case of high injection device, such as PiN diode, it can be illustrated as Figure 23. Hole quasi-Fermi potential $\emptyset_p$ is equal to Anode potential connected to P-Emitter because hole is majority carrier in P-Emitter. Similarly, electron quasi-Fermi potential $\emptyset_n$ is equal to Cathode potential. In on-state, N-Base potential φ is lower than hole quasi-Fermi potential and higher than electron quasi-Fermi potential. The definitions for

quasi-Fermi potential are following.

$$n(x) = n_i e^{\frac{q}{kT}(\varphi - \emptyset_n)} \tag{61}$$

$$p(x) = n_i e^{\frac{q}{kT}(\emptyset_p - \varphi)} \tag{62}$$

where n_i is intrinsic carrier density. Band gap narrowing model [46] [47] [48] should be considered to apply effective intrinsic carrier density.

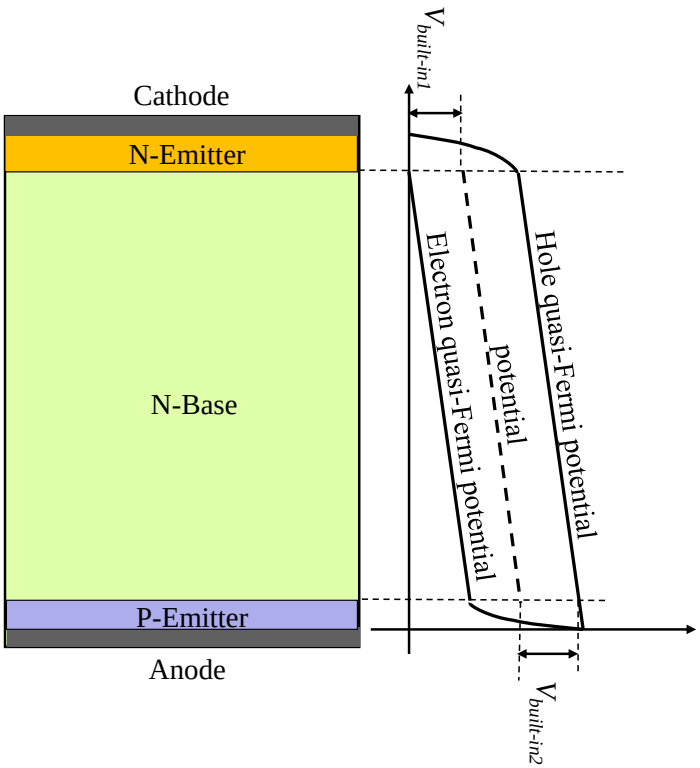


Figure 23. Built-in potential for high injection devices.

In proposed IGBT model, the built-in potential is calculated as the sum of the difference between hole quasi-Fermi potential and potential at x_1 and the difference between electron quasi-Fermi potential and potential at x_2 as shown in Figure 24. They can be calculated by (53) and (54).

$$V_{built-in}(x_1) = \frac{kT}{q} \log \frac{n(x_1)}{n_i} \tag{63}$$

$$V_{built-in}(x_2) = \frac{kT}{q}\log\frac{n(x_2)}{n_i} \tag{64}$$

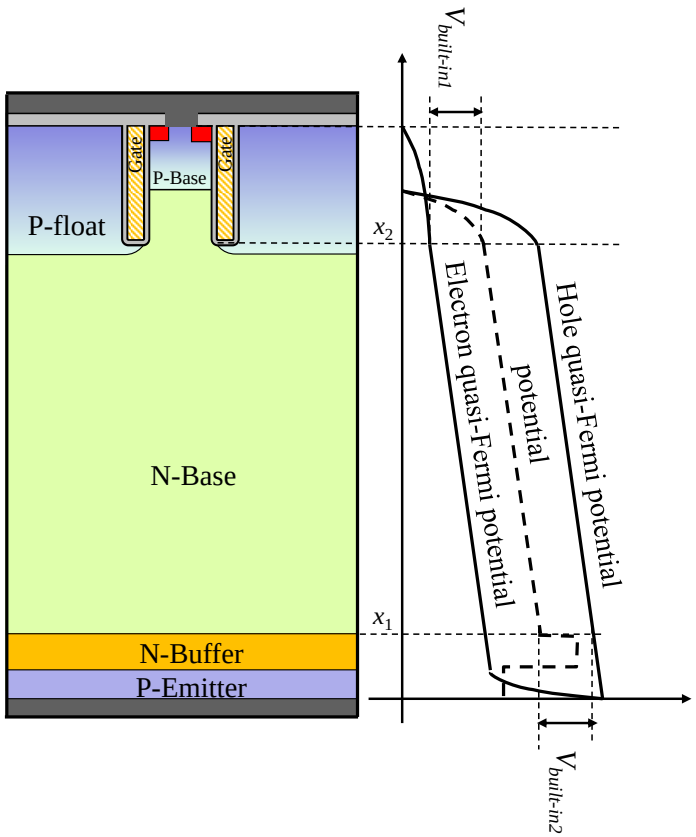


Figure 24. Built-in potential definition for the model.

4.4 Implementation

The established model was implemented on *Microsoft Excel* spreadsheet application software as shown in Figure 25. A solution between current density, Anode side hole injection efficiency, and Cathode side electron injection efficiency is found by genuine newton solver add-on of the software. GRG non-linear method is used due to good convergence.

The equations mentioned above are described on the spreadsheet. The solution for each current density is found by least squares method with varying electron injection efficiency from Cathode side and hole injection efficiency from Anode side. Carrier distribution profiles for N-Base and mesa region is also calculated. The step is repeated from small

current density to rated current density. Finally, *Jc-Vce* characteristic is formed. Typical calculation time is several seconds for each current density by standard performance laptop PC (*Lenovo ThinkPad X121e*; *AMD E-300* processor 1.30GHz).

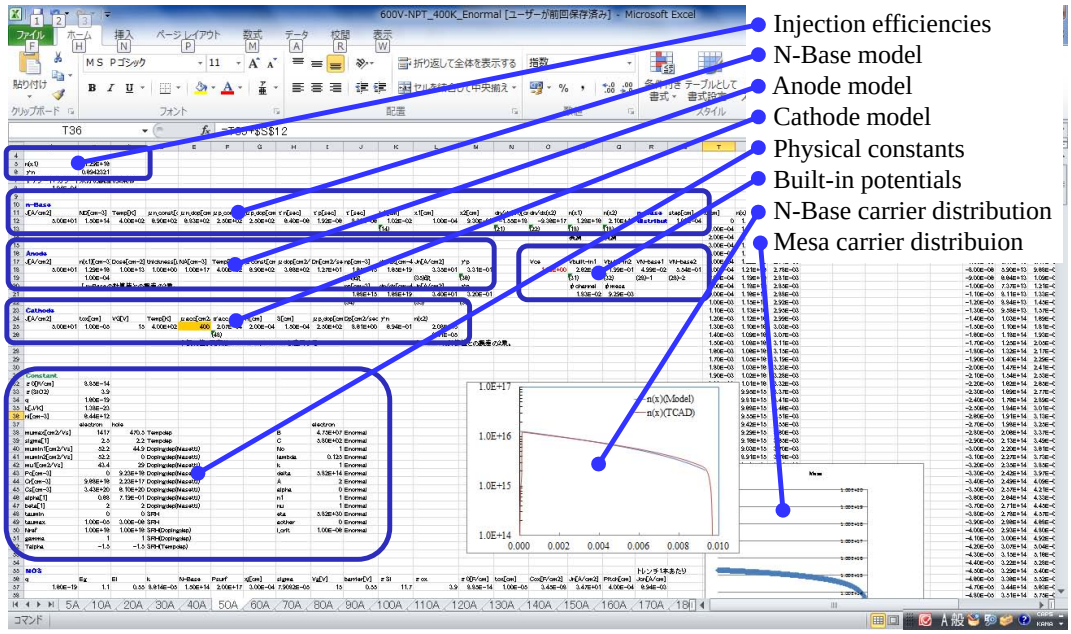


Figure 25. Model implementation on Microsoft Excel.

4.5 Verification Results

Established model was verified by comparing with two-dimensional TCAD calculation results. *Synopsys Sentaurus Process* and *Sentaurus Device* version E-2010.12 was used for TCAD calculation. Process simulation was performed to create FEM models of IGBT. Then voltage boundary conditions were applied in device simulation.

4.5.1 Structures

Three types of trench gate IGBT are used for the validation; 600V rated NPT-IGBT, 1200V rated PT-IGBT and 3.3kV rated IEGT. Cross sectional views and structure parameters for these structures are summarized in Figure 26 and Table 3. For 3.3kV IEGT structure, cell pitch and trench depth were varied to confirm the model could follow injection enhancement effect.

The 600V NPT-IGBT has shallow P-Emitter and no N-Buffer. Wafer thickness is 100um. Cell structure is standard trench gate IGBT with 2um half cell pitch. No dummy

cell for injection enhancement is used. Rated current density is 200A/cm^2.

The 1200V PT-IGBT has shallow P-Emitter and shallow N-Buffer. Wafer thickness is 120um. Cell structure is standard trench gate IGBT with 2um half cell pitch. No dummy cell for injection enhancement is used. Rated current density is 150A/cm^2.

The 3.3kV IEGT has also shallow P-Emitter and shallow N-Buffer. Wafer thickness is 350um. Cell structure is trench gate IEGT type. It has dummy cell with P-float layer for injection enhancement. Rated current density is 50A/cm^2.

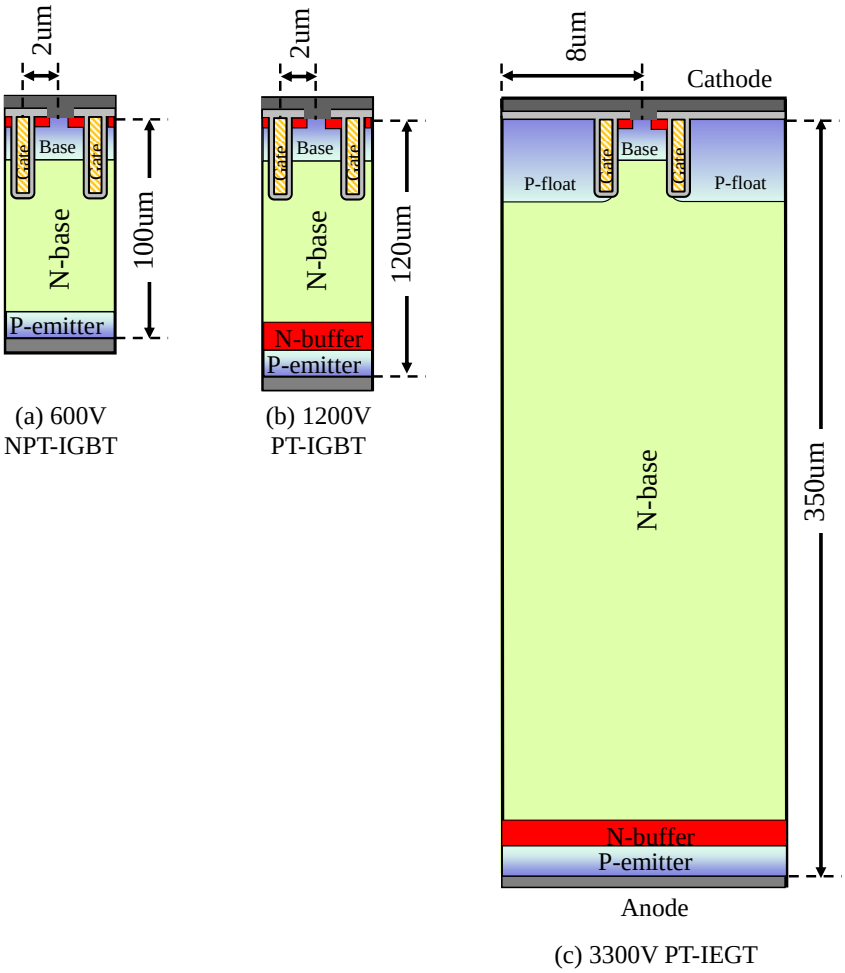


Figure 26. Structures used for verifications.

Table 3. Parameters using model verification.

Parameters	600V NPT-IGBT	1200V PT-IGBT	3.3kV PT-IEGT
N-Base concentration [1/cm^3]	1.5 x10^{14}	8x10^{13}	2x10^{13}
N-Base thickness [um]	93	112	342
Half-cell pitch: *W* [um]	2.0	2.0	8.0(center)
Half mesa width: *S* [um]	1.5	1.5	1.5
P-Base surface concentration[1/cm^3]	2x10^{17}	2x10^{17}	2x10^{17}
P-Base thickness: *Db* [um]	3.0	3.0	3.0
Trench depth: *DT* [um]	6.0	6.0	6.0(center)
Gate oxide thickness: *Tox* [angstrom]	1000	1000	1000
P-Emitter concentration: *NA* [1/cm^3]	1x10^{17}	1x10^{17}	2x10^{17}
P-Emitter thickness: *Lp* [um]	1.0	1.0	1.0
N-Buffer concentration: *ND* [1/cm^3]	No N-Buffer	9x10^{16}	9x10^{16}
N-Buffer thickness: *Ln* [um]		1.0	1.0

4.5.2 Physical models

Several physical models were commonly applied for the proposed model and TCAD. Especially temperature dependences were taken into account to follow device temperature. The device temperature is varied from 300K, 400K and 450K in the validation.

Physical constants for room temperature are summarized in Table 4. For carrier mobility, doping concentration dependence and temperature dependence are considered. And Electron mobility degradation by normal electric field in MOS channel is considered to calculate electron current through MOS channel.

For carrier lifetime, doping concentration dependence and temperature dependence are considered.

For effective intrinsic carrier density, doping concentration dependence [47] and temperature dependence [49] band gap narrowing model are applied.

Table 4. Physical constants for 300K.

Constants	For electron	For hole
Carrier mobility [cm^2/Vs]	1417	470.5
Carrier lifetime [usec]	10.0	3.0
Intrinsic carrier density [$1/ cm^3$]	$1.18x10^{10}$	

4.5.3 Calculation Results

Forward *Jc-Vce* characteristics and on-state carrier distribution profiles were calculated and compared with TCAD results. TCAD carrier distribution profile was measured at the center of trench MOS cell as Figure 27.

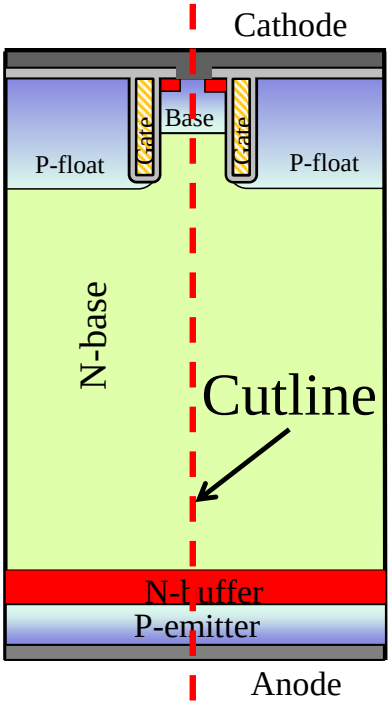


Figure 27. Carrier distribution profile measurement.

Forward *Jc-Vce* characteristics for 600V NPT-IGBT are summarized in Figure 28. These calculation results show good agreement with TCAD results. On-state N-Base carrier distribution profiles for 600V NPT-IGBT are calculated at *Jc*=50A/cm^2, 100A/cm^2, 150A/cm^2 and 200A/cm^2 as shown in Figure 29, Figure 30, Figure 31, and Figure 32, respectively. These calculation results show good agreement with TCAD results. It means the model can be applied to low rated voltage IGBT from room temperature to extremely high temperature, perfectly.

Forward *Jc-Vce* characteristics for 1200V NPT-IGBT are summarized in Figure 33. These calculation results also show good agreement with TCAD results. On-state N-Base carrier distribution profiles for 1200V PT-IGBT are calculated at *Jc*=50A/cm^2, 100A/cm^2, and 150A/cm^2 as shown in Figure 33, Figure 34, and Figure 35, respectively. These calculation results show good agreement with TCAD results. It means the model can be applied to medium rated voltage IGBT from room temperature to extremely high

temperature, perfectly.

Forward *Jc*-*Vce* characteristics for 3.3kV IEGT are summarized in Figure 37. These calculation results also show better agreement with TCAD results but slight difference is observed in T=450K case. On-state N-Base carrier distribution profiles for 3.3kV IEGT are calculated at *Jc*=10A/cm^2, 30A/cm^2, and 50A/cm^2 as shown in Figure 38, Figure 39, and Figure 40, respectively. These calculation results show better agreement with TCAD results but slight differences are observed especially N-Base both edges.

For trench depth variation for 3.3kV IEGT, trench depth-*Vce(sat)* relationship with 8.0um of half-cell pitch is summarized in Figure 41. For cell pitch variation for 3.3kV IEGT, cell pitch-*Vce(sat)* relationship with 6.0um of trench depth is summarized in Figure 42. These calculation results show better agreement with TCAD results. They indicate the model can predict device improvement accurately.

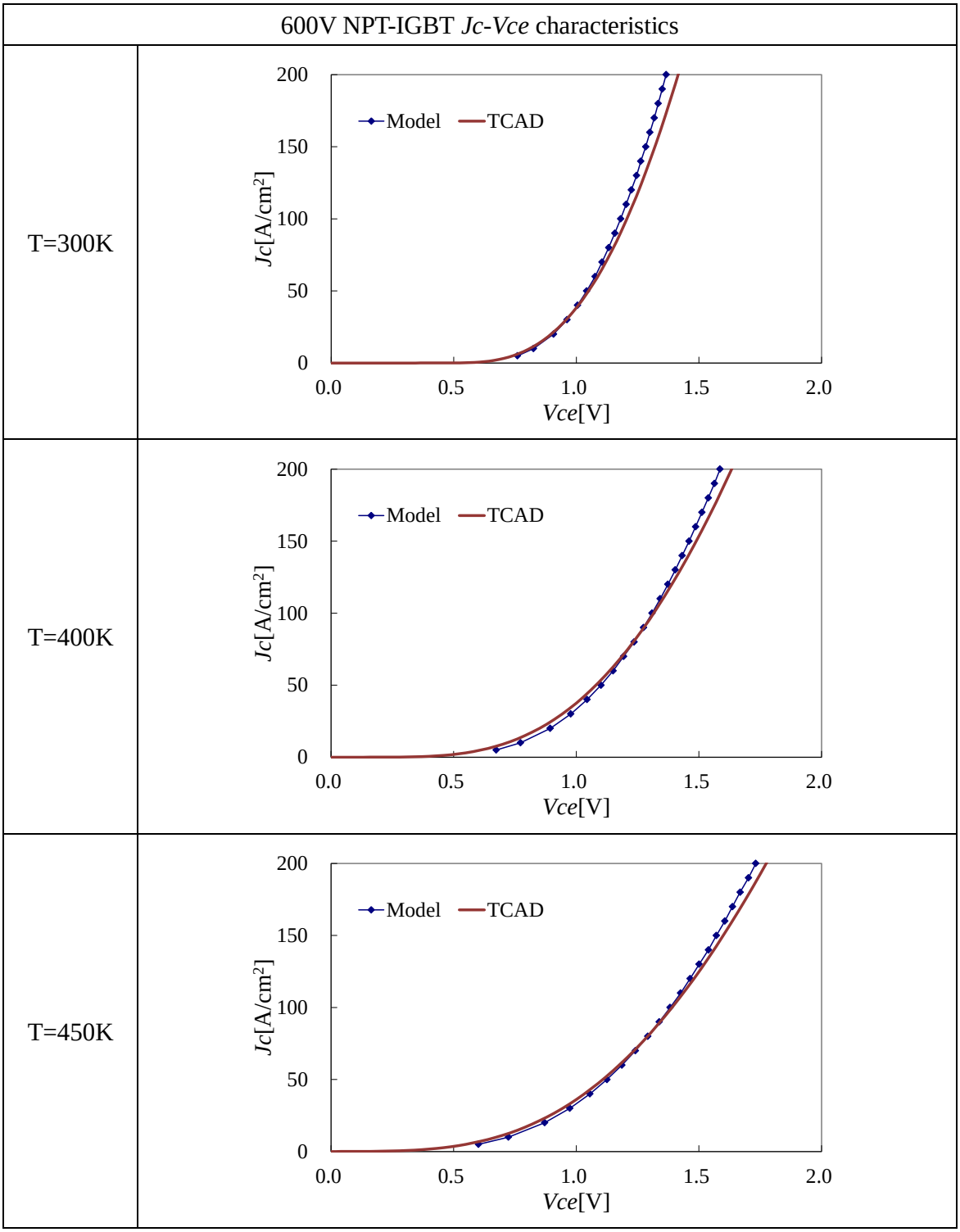


Figure 28. Calculated *Jc*-*Vce* characteristic comparison between proposed compact model and TCAD simulator for 600V NPT-IGBT.

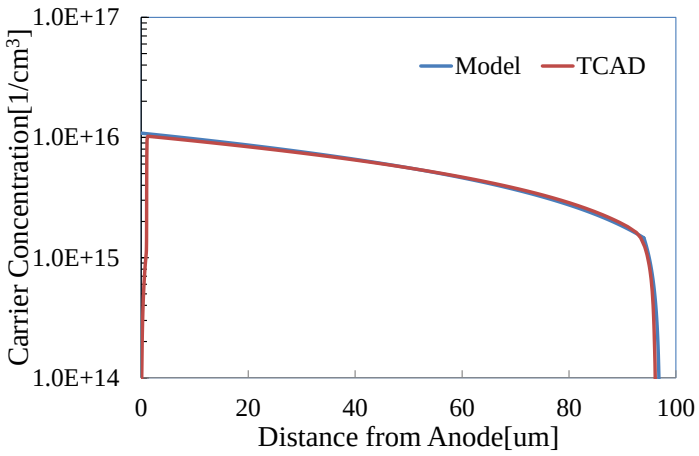
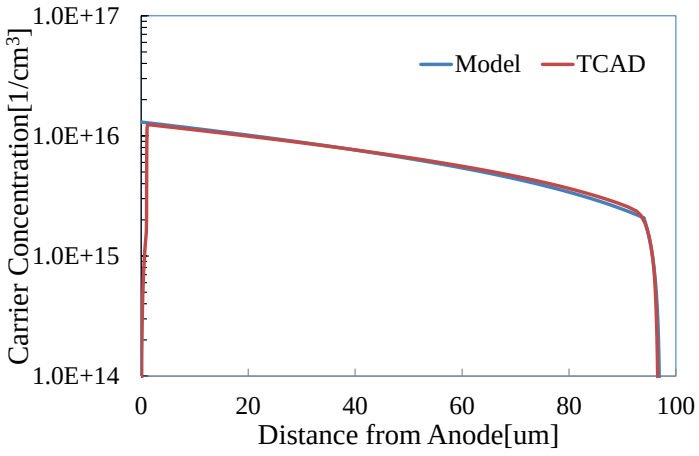
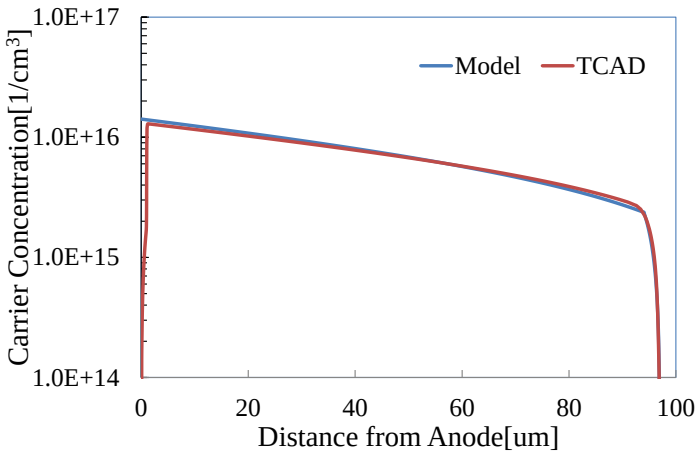
600V NPT-IGBT carrier distribution at 50A/cm^2	
T=300K	
T=400K	
T=450K	

Figure 29. Calculated carrier distribution comparison between proposed compact model and TCAD simulator for 600V NPT-IGBT at 50A/cm^2.

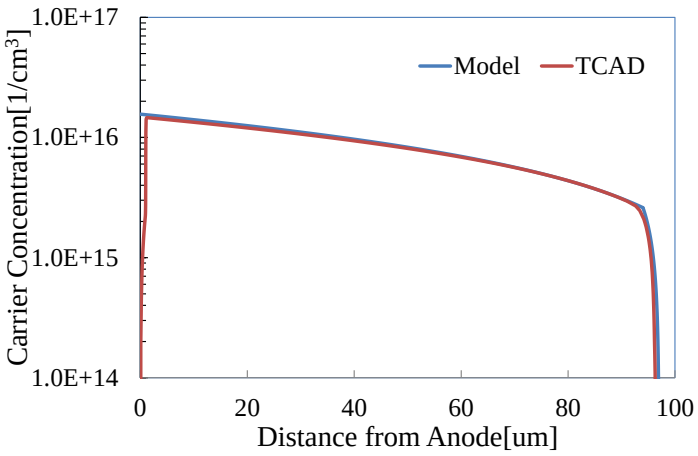
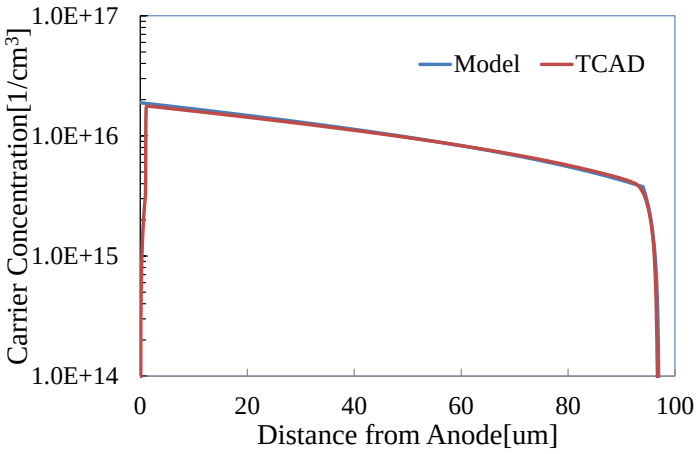
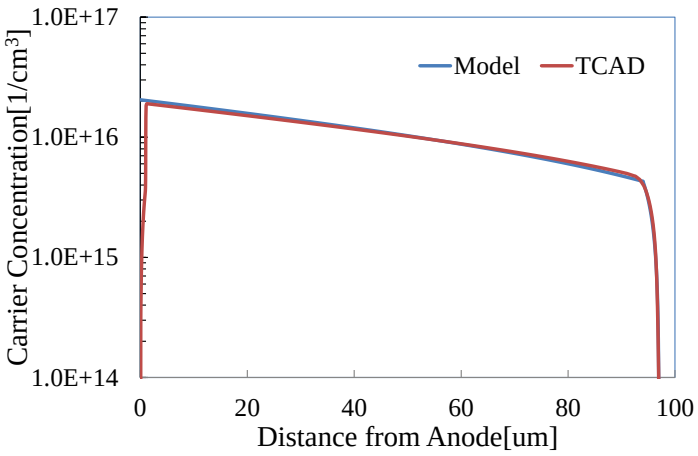
600V NPT-IGBT carrier distribution at 100A/cm^2	
T=300K	
T=400K	
T=450K	

Figure 30. Calculated carrier distribution comparison between proposed compact model and TCAD simulator for 600V NPT-IGBT at 100A/cm^2.

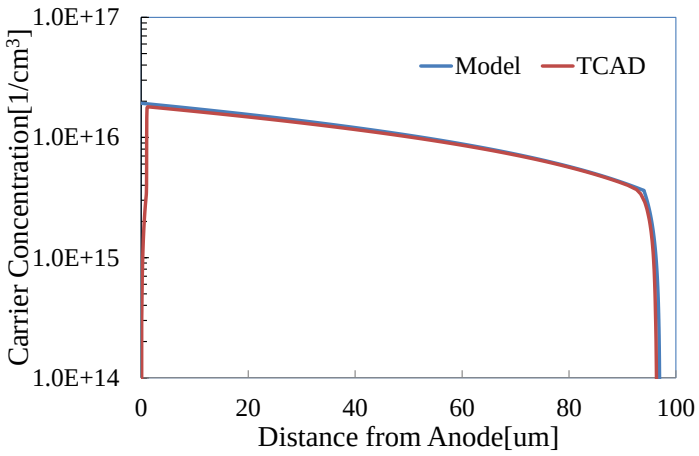
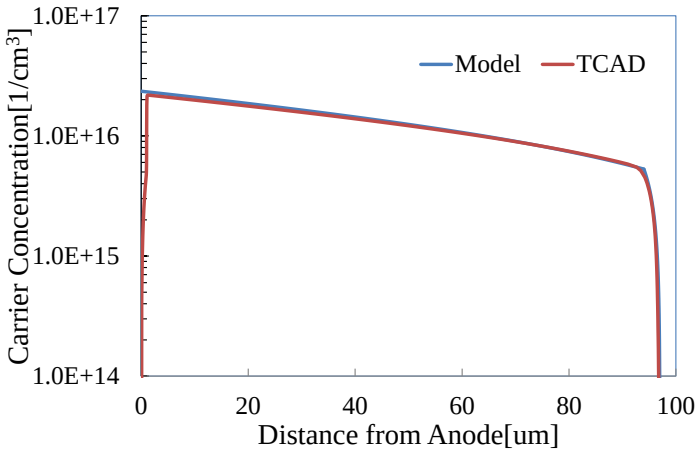
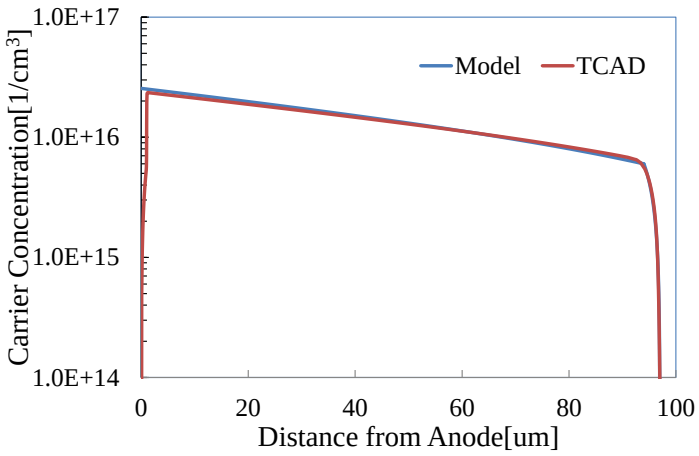
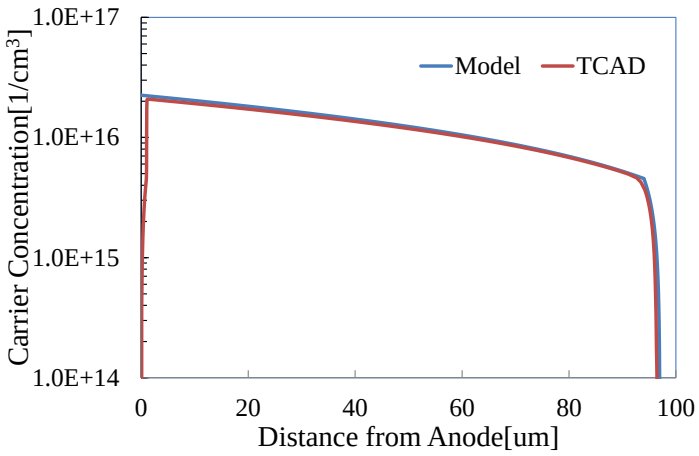
600V NPT-IGBT carrier distribution at 150A/cm^2	
T=300K	
T=400K	
T=450K	

Figure 31. Calculated carrier distribution comparison between proposed compact model and TCAD simulator for 600V NPT-IGBT at 150A/cm^2.

<table>
<tr><td colspan="2">600V NPT-IGBT carrier distribution at 200A/cm^2</td></tr>
<tr><td>T=300K</td><td> 
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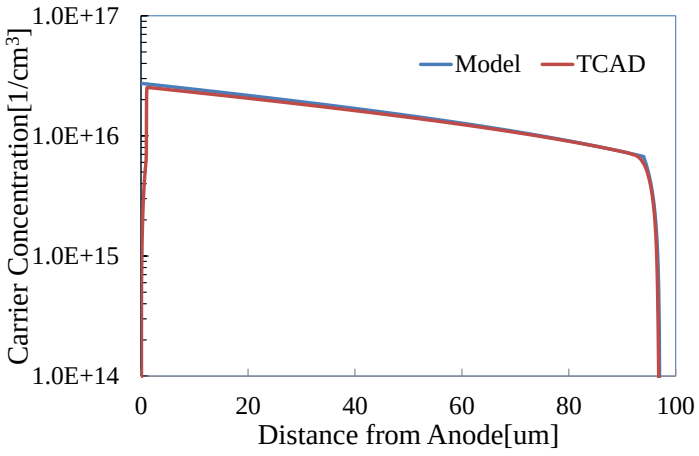
<tr><td>T=400K</td><td> 
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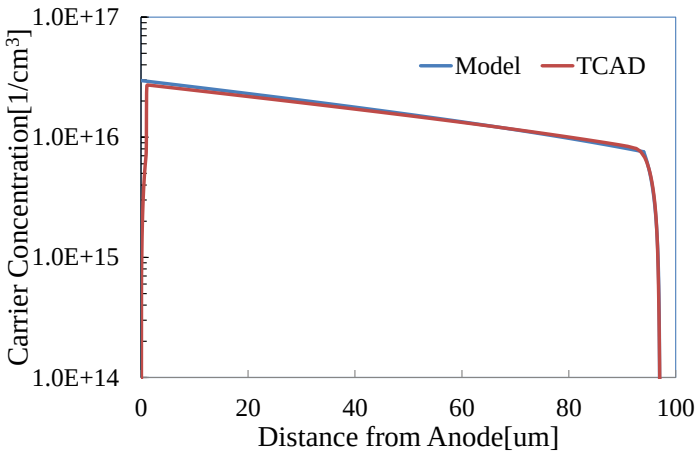
<tr><td>T=450K</td><td> 
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</table>

Figure 32. Calculated carrier distribution comparison between proposed compact model and TCAD simulator for 600V NPT-IGBT at 200A/cm^2.

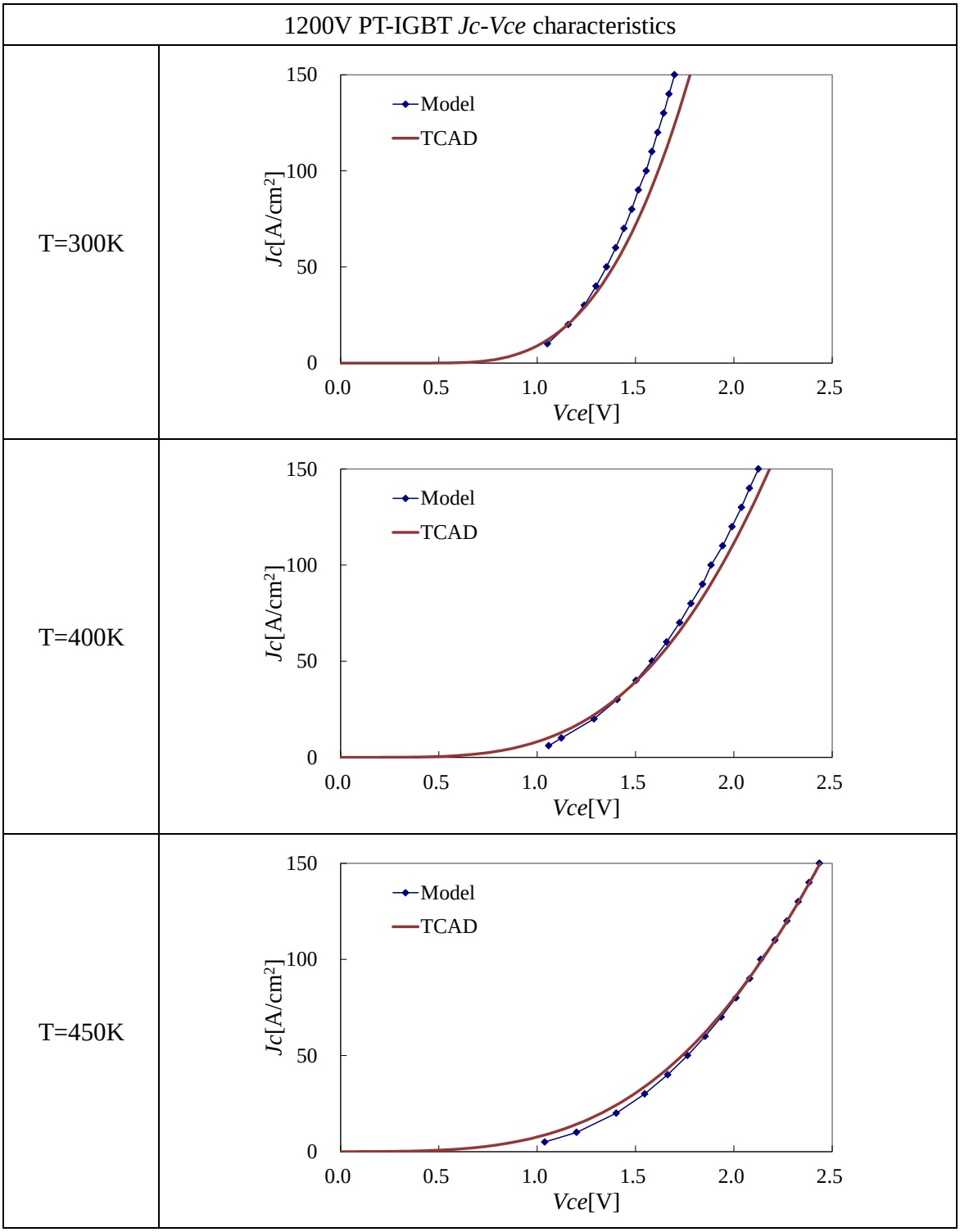


Figure 33. Calculated *Jc-Vce* characteristic comparison between proposed compact model and TCAD simulator for 1200V PT-IGBT.

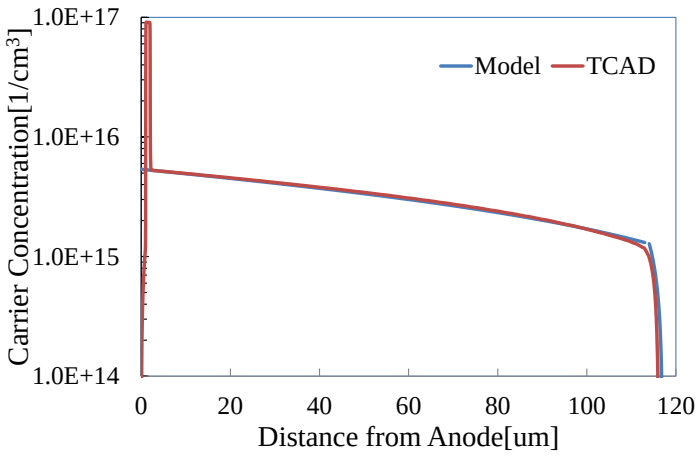
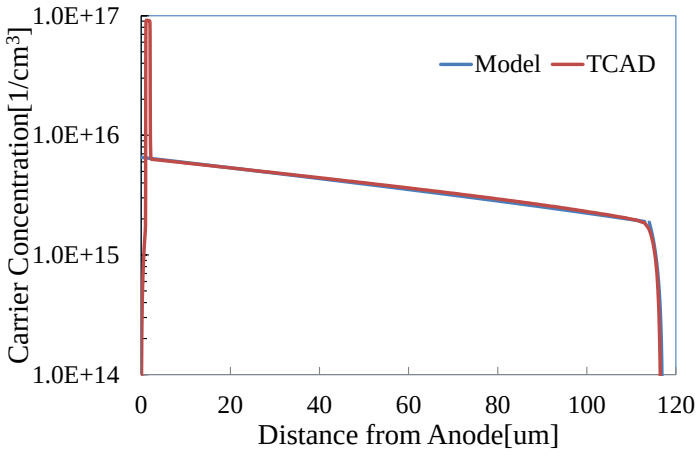
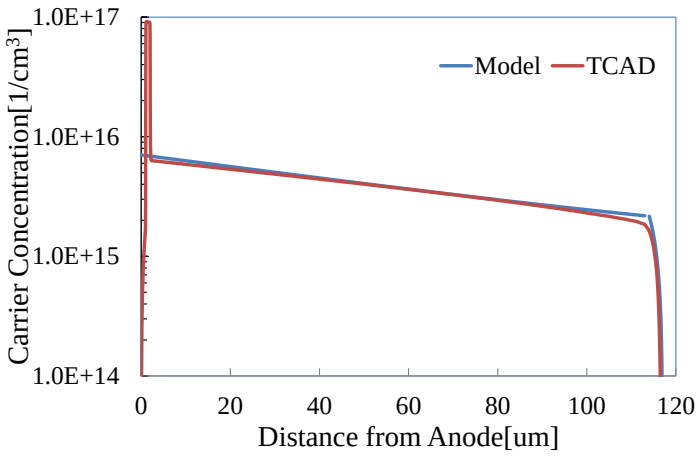
1200V PT-IGBT carrier distribution at 50A/cm^2	
T=300K	
T=400K	
T=450K	

Figure 34. Calculated carrier distribution comparison between proposed compact model and TCAD simulator for 1200V PT-IGBT at 50A/cm^2.

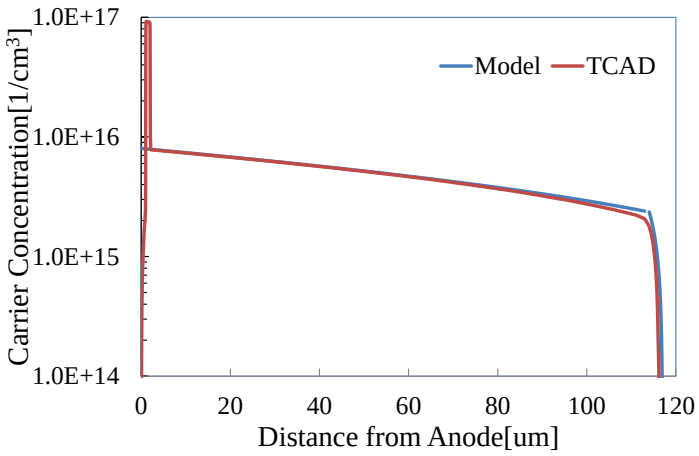
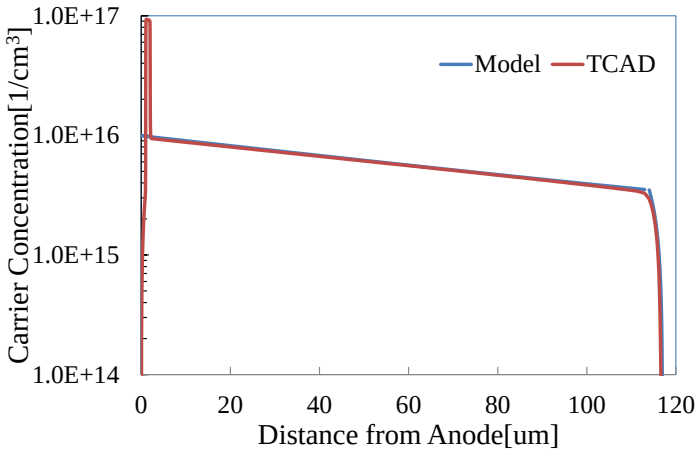
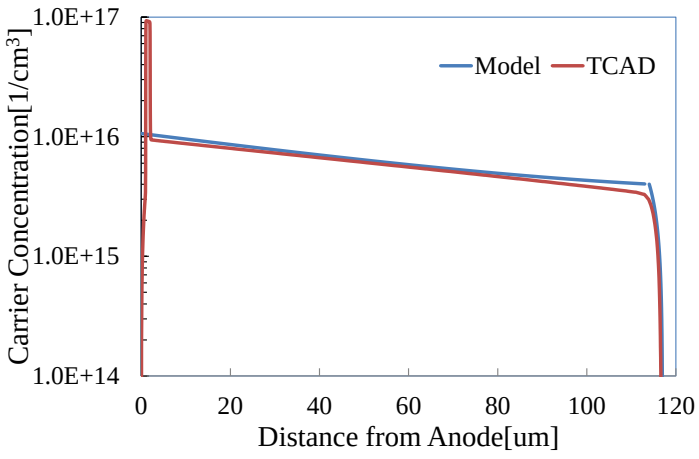
1200V PT-IGBT carrier distribution at 100A/cm^2	
T=300K	
T=400K	
T=450K	

Figure 35. Calculated carrier distribution comparison between proposed compact model and TCAD simulator for 1200V PT-IGBT at 100A/cm^2.

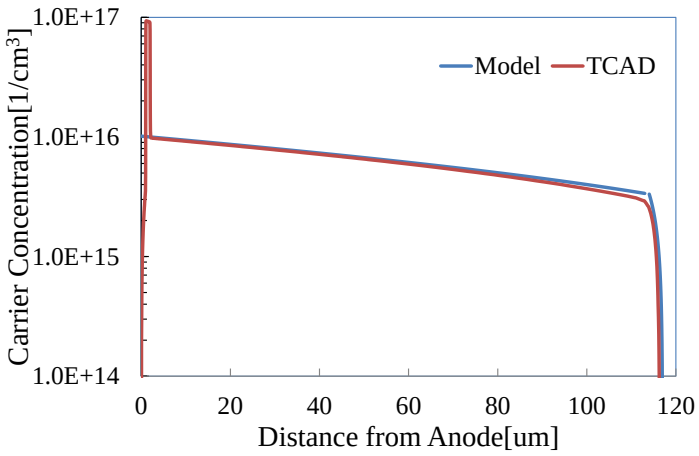
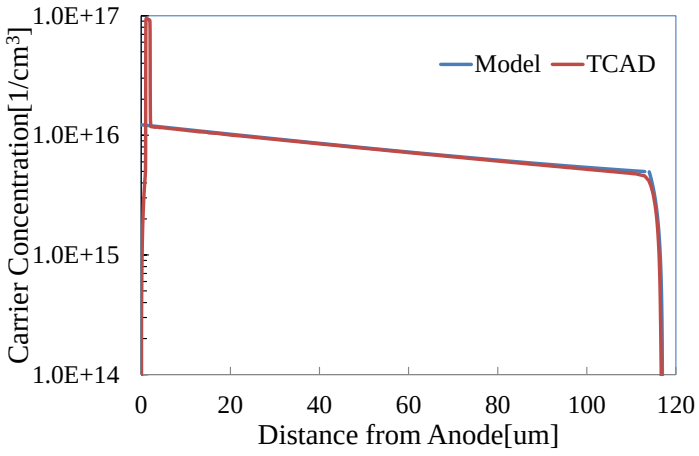
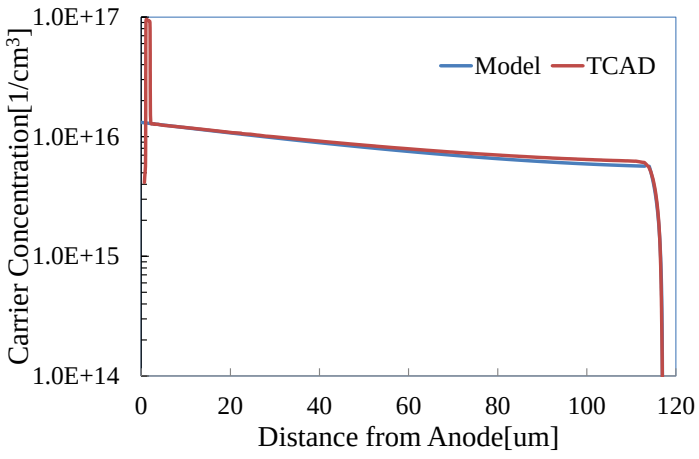
1200V PT-IGBT carrier distribution at 150A/cm^2	
T=300K	
T=400K	
T=450K	

Figure 36. Calculated carrier distribution comparison between proposed compact model and TCAD simulator for 1200V PT-IGBT at 150A/cm^2.

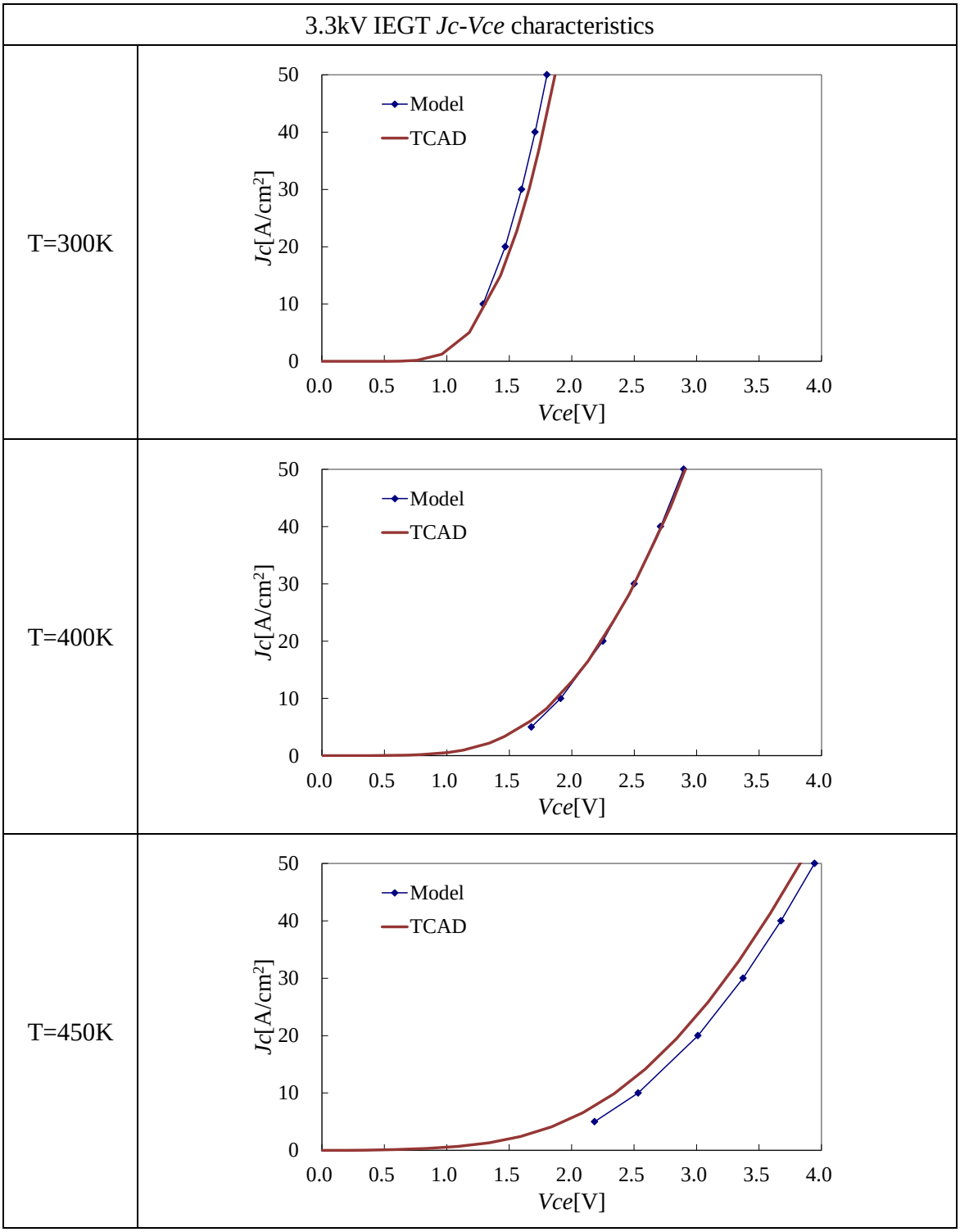


Figure 37. Calculated *Jc-Vce* characteristic comparison between proposed compact model and TCAD simulator for 3.3kV IEGT.

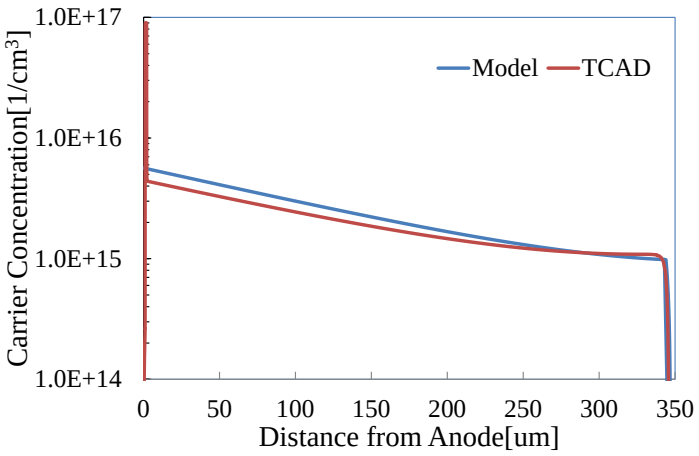
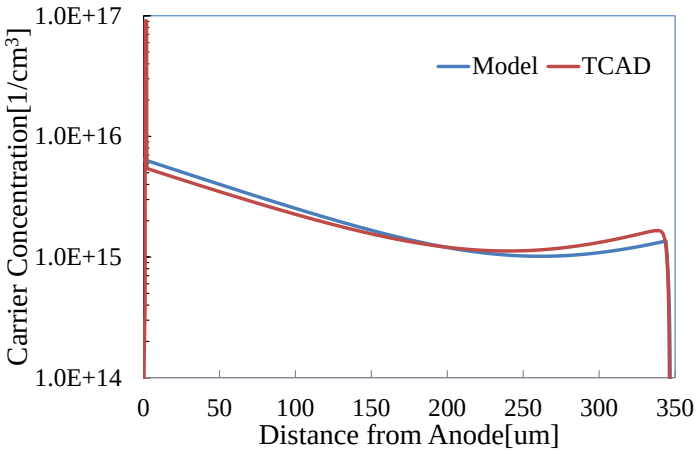
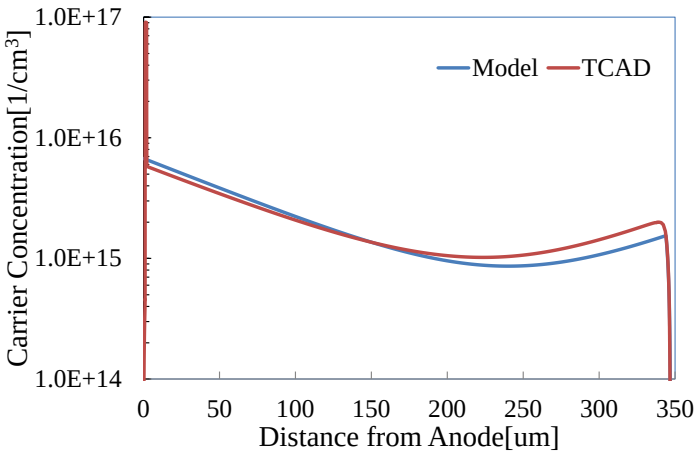
3.3kV IEGT carrier distribution at 10A/cm^2	
T=300K	
T=400K	
T=450K	

Figure 38. Calculated carrier distribution comparison between proposed compact model and TCAD simulator for 3.3kV IEGT at 10A/cm^2.

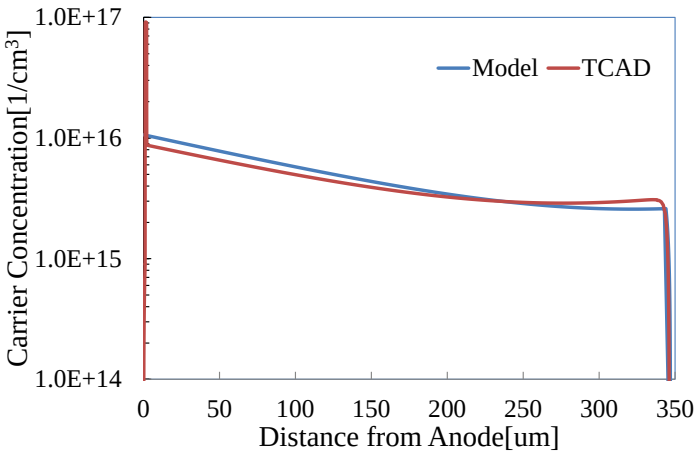
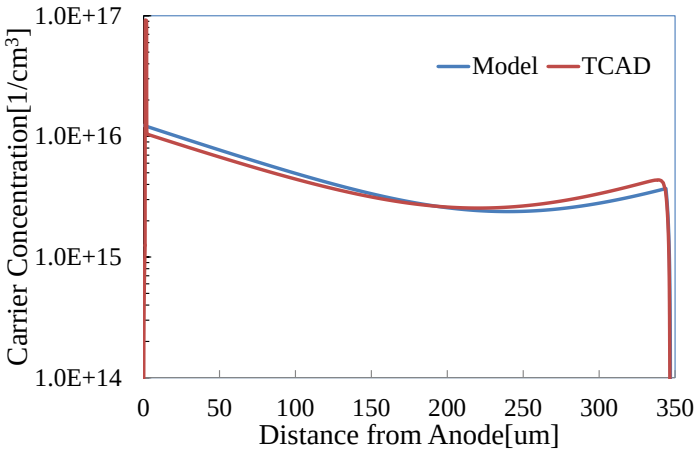
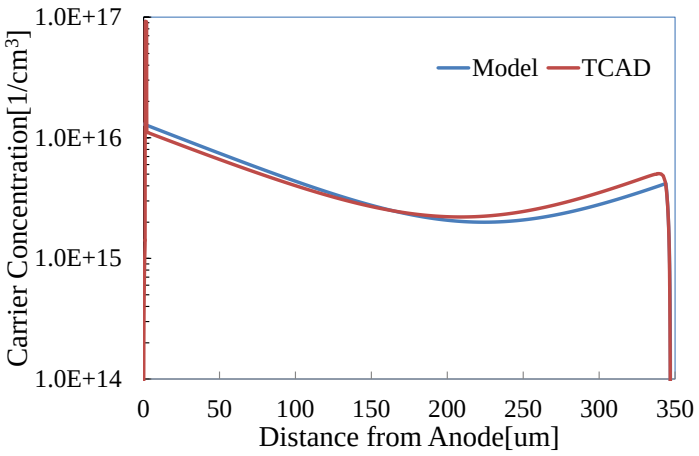
3.3kV IEGT carrier distribution at 30A/cm^2	
T=300K	
T=400K	
T=450K	

Figure 39. Calculated carrier distribution comparison between proposed compact model and TCAD simulator for 3.3kV IEGT at 30A/cm^2.

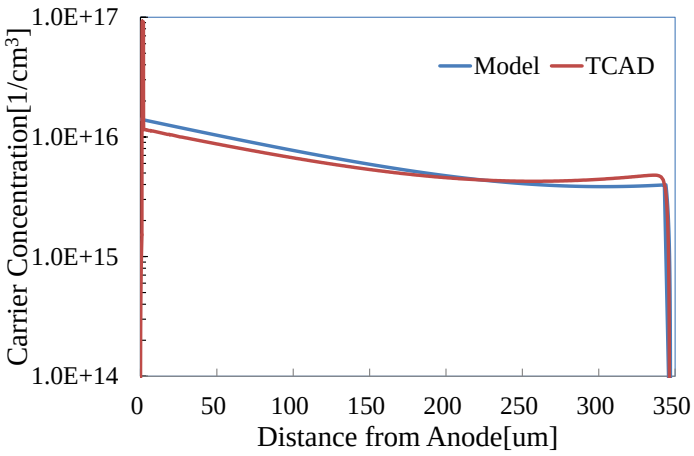
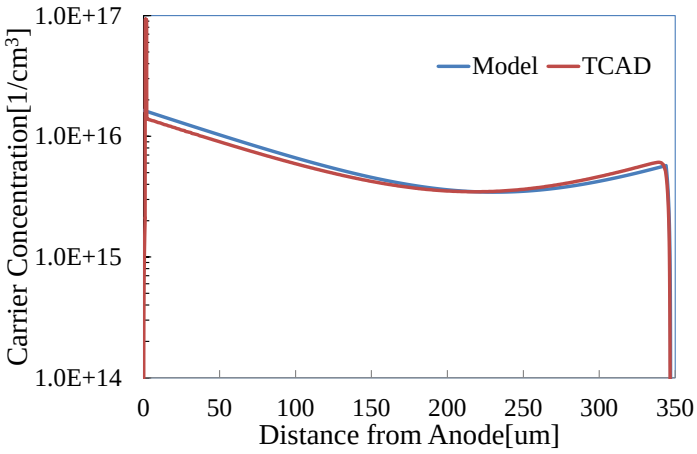
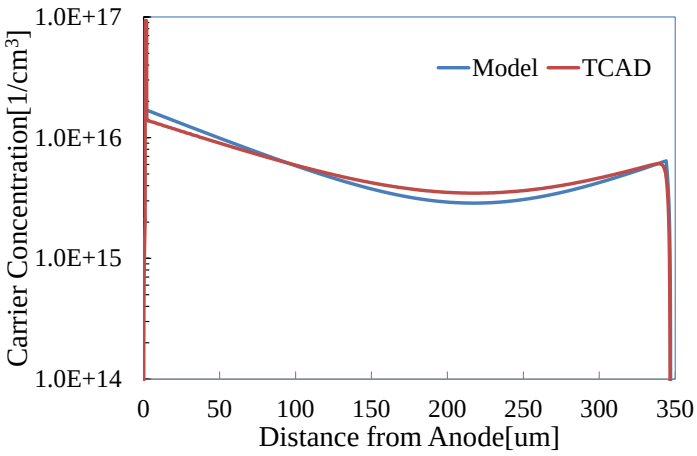
3.3kV IEGT carrier distribution at 50A/cm^2	
T=300K	
T=400K	
T=450K	

Figure 40. Calculated carrier distribution comparison between proposed compact model and TCAD simulator for 3.3kV IEGT at 50A/cm^2.

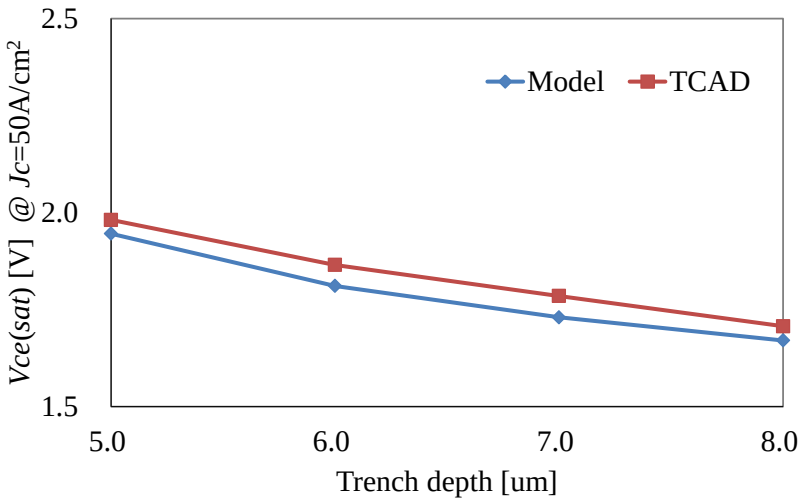


Figure 41. Trench depth-*Vce(sat)* relationship comparison between proposed model and TCAD for 3.3kV IEGT.

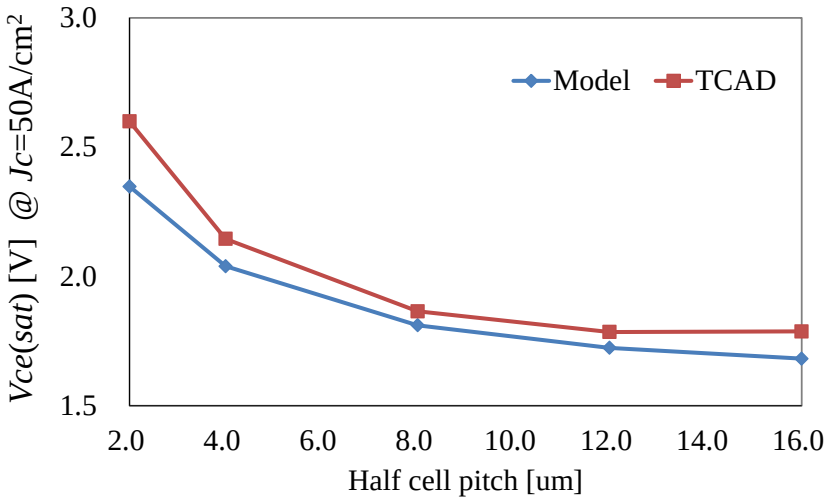


Figure 42. Cell pitch-*Vce(sat)* relationship comparison between proposed model and TCAD for 3.3kV IEGT.

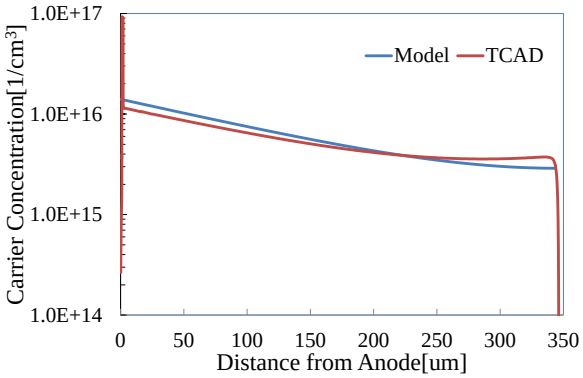
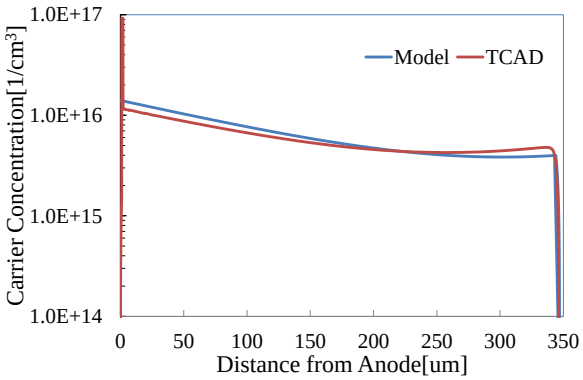
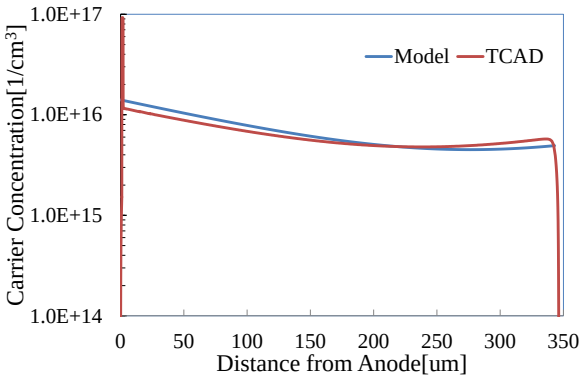
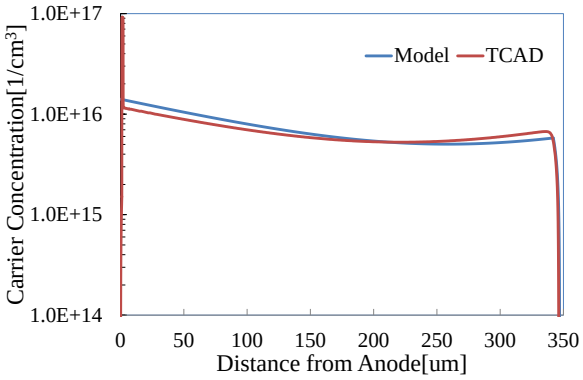
3.3kV IEGT carrier distribution at 50A/cm^2, trench depth dependencies	
5um	
6um(ref.)	
7um	
8um	

Figure 43. On-state carrier distribution profiles with varied trench depth for 3.3kV IEGT at 50A/cm^2. Electron injection efficiency from Cathode side depends on the depth.

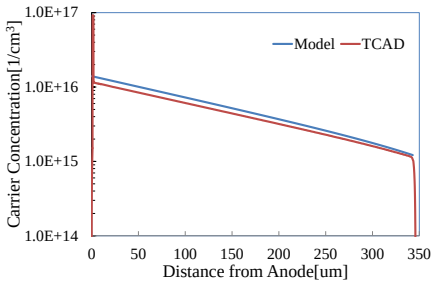
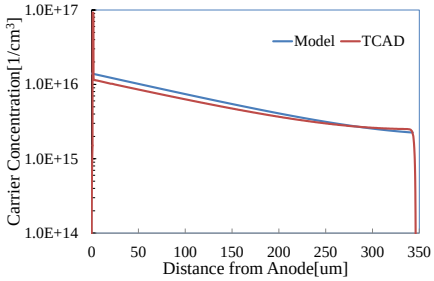
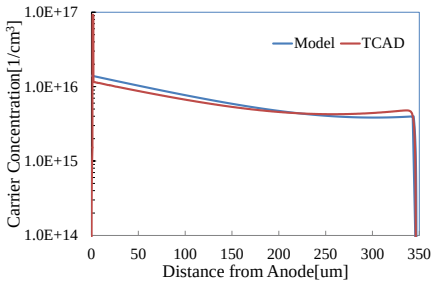
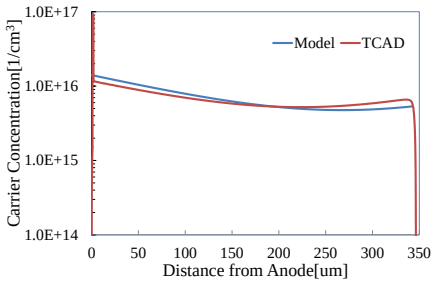
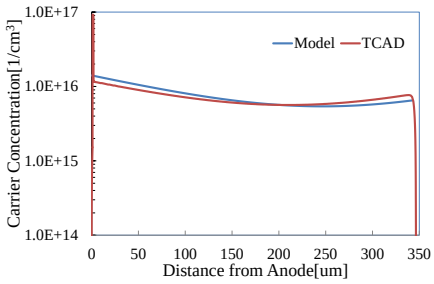
3.3kV IEGT carrier distribution at 50A/cm^2, cell pitch dependencies	
2um	
4um	
8um(ref.)	
12um	
16um	

Figure 44. On-state carrier distribution profiles with varied half cell pitch for 3.3kV IEGT at 50A/cm^2. Electron injection efficiency from Cathode side depends on the cell pitch.

4.6 Discussion

By the results shown in previous paragraph, the basic feasibility of the model is proved. The model can be applied for wide range of rated voltage and device temperature. Three topics will be discussed in this paragraph.

4.6.1 Boundary condition between P-Base and N-Base

In this model, zero carrier concentration is assumed as a boundary condition at the junction between P-Base and mesa region (N-type) to calculate carrier distribution in mesa region. However, there is depletion layer extended from the junction toward mesa region as shown in Figure 45 for 600V NPT-IGBT and Figure 46 for 3.3kV IEGT. Carrier distribution profile is different from TCAD calculation results. It affects the boundary condition between N-Base and mesa region. Especially in 3.3kV IEGT case, the width of the depletion layer is about 0.8um and it is considerable by comparing mesa length of 3.0um. It is equivalent to shallower trench depth.

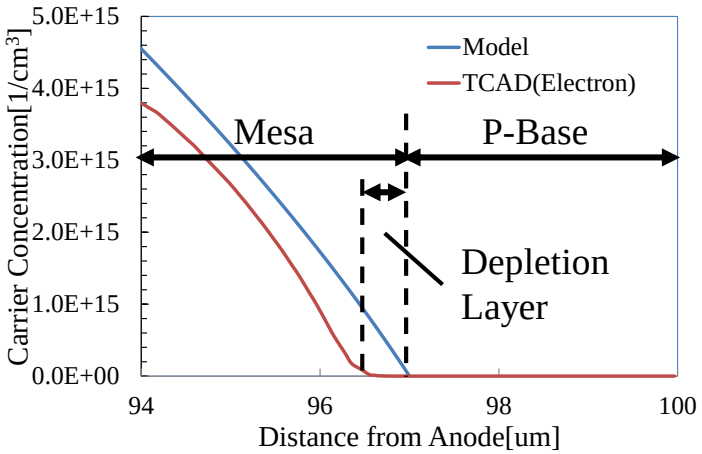


Figure 45. Carrier distribution in mesa region of 600V NPT-IGBT at 200A/cm^2.

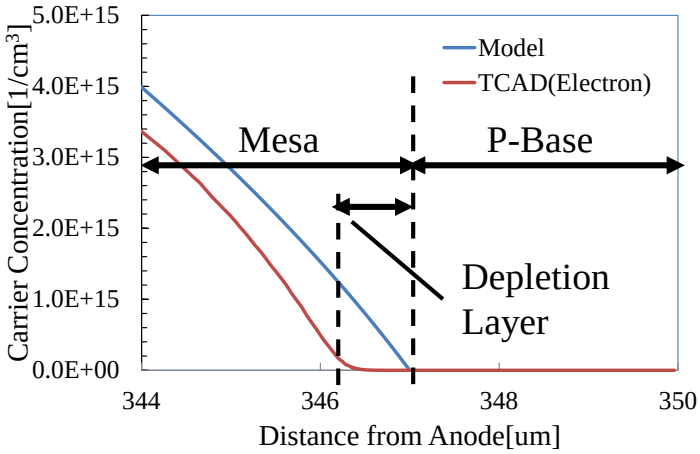


Figure 46. Carrier distribution in mesa region of 3.3kV IEGT at 50A/cm^2.

4.6.2 Electron current via accumulation layer

Electron current via accumulation layer acts an important role. Carrier concentration in mesa region, electron current density in mesa region and electron current via accumulation layer are shown in Figure 47. The structure is 1200V PT-IGBT. The current density is 150A/cm^2.

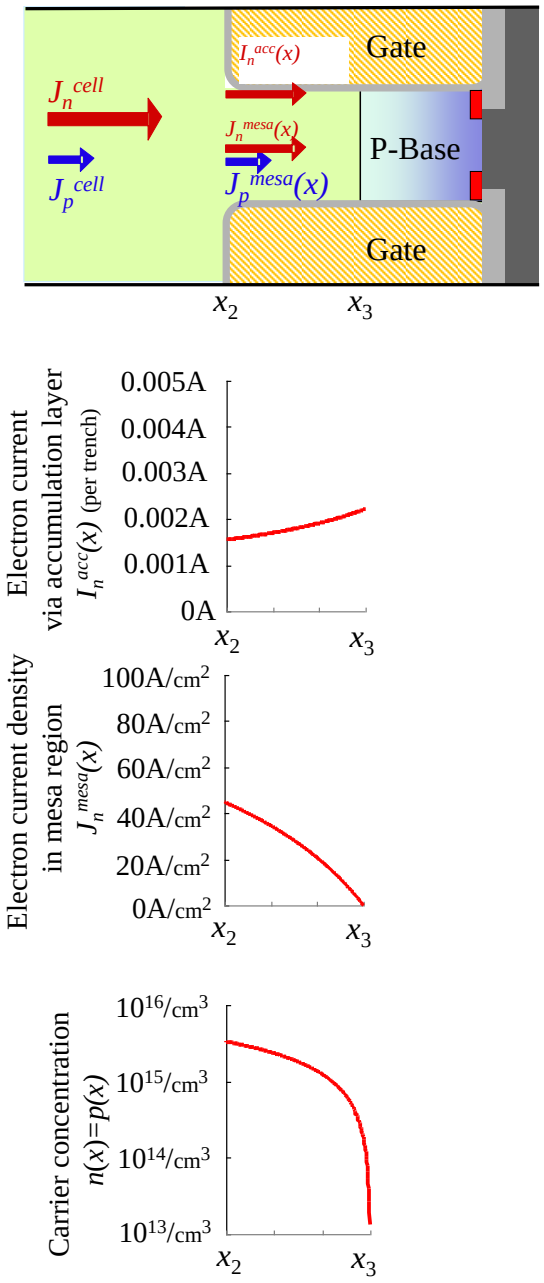


Figure 47. Relationship for carrier concentration in mesa region, electron current density in mesa region and electron current via accumulation layer. The structure is 1200V PT-IGBT. The current density is 150A/cm^2.

In this condition, the electron current density in N-Base region is 111A/cm^2 by $\gamma_n = 0.74$. On the other hand, the electron current density at position x_2 is about 44.4A/cm^2

as shown in Figure 47. So, 40% of electron current at N-Base edge, position x_2, flows from mesa region. And 60% of that flows from the accumulation layer. Therefore, the mobility of the accumulation layer μ_{acc} strongly affects the balance of each electron current element. Moreover, electron injection efficiency γ_n can be improved by increasing μ_{acc}. The proposed compact model formulates this aspect accurately.

4.7 Further works

In this work, accurate on-state modeling for modern trench gate IGBT is realized. Accurate carrier distribution can be obtained by the established model. For further works, compact modeling for turn-off characteristics can be considered. Several works were reported for PiN diode reverse recovery characteristics calculation by on-state carrier distribution [50]. The carrier distribution of PiN diode is similar to IGBT's because PiN diode and IGBT has both high resistivity N-Base layer and their stored carrier keep "conductive modulation" status. And turn-off process of IGBT is also similar to reverse recovery process of PiN diode because they are exhausting operations for stored carrier by applied electric field. The difference is that IGBT has P-Emitter region and it acts as hole injection source during turn-off process. The phenomena can be explained by the Anode model previously described in section 3.4. So, accurate turn-off characteristics should be calculated by these models. Some parasitic capacitances, they affect turn-off characteristics, should be also modeled by structure parameters.

4.8 Summary

New compact model for Trench gate IGBT was established. The model is formulated by only physical parameters. Based on previously proposed structure oriented design model, calculation program to write *Jc*-*Vce* characteristics and carrier distribution profiles was implemented. Modeling is easier than existing compact models because parameter extraction is not required. And also no fitting parameter exists for the modeling. The model is validated by comparing with two-dimensional TCAD simulation results for three IGBT structures. The forward characteristics and the internal carrier distributions of 600V thin wafer NPT-IGBT, 1200V thin wafer PT-IGBT and 3.3kV IEGT show superior agreement with TCAD results with temperature range from 300K to 450K. The model capability for structure parameter dependencies was also confirmed.

5 IGBT Scaling Principle toward Shallow Trench Structure

5.1 Cutting Edge Silicon Technology and IGBT

The 300mm to 450mm "More Moore" field semiconductor technology based on high resolution lithographic techniques enhances significant performance and mass-productivity improvements in digital integrated circuits by Moore's Law as a scaling by a factor of 0.7 every 2 years for critical dimension [51] as shown in Figure 48. On the other hand, the importance of "More than Moore" field like that analog and mixed signal processors, sensors and actuators, micro-mechanical devices, and power devices, is increased a lot. And these "More than Moore" devices also will be forced to be designed in the compatibility of the large diameter wafer process technology to realize better performance and manufacturability as shown in Figure 49.

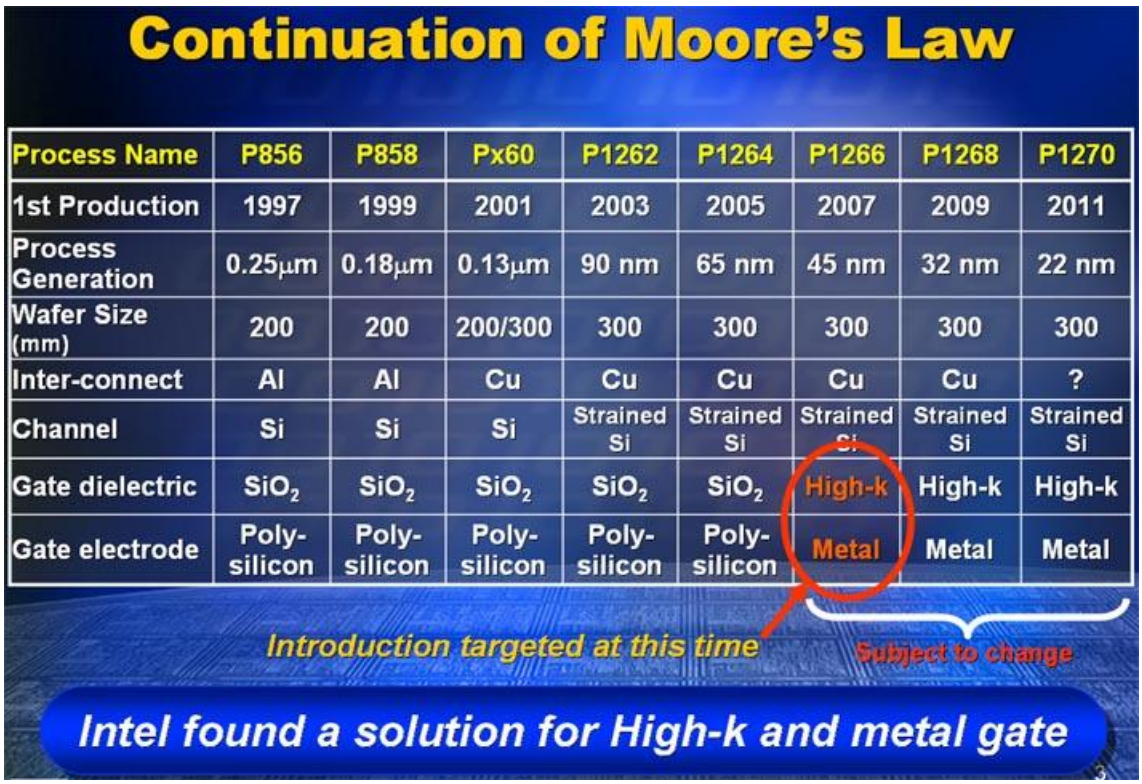


Figure 48. Technology node shrinking [52].

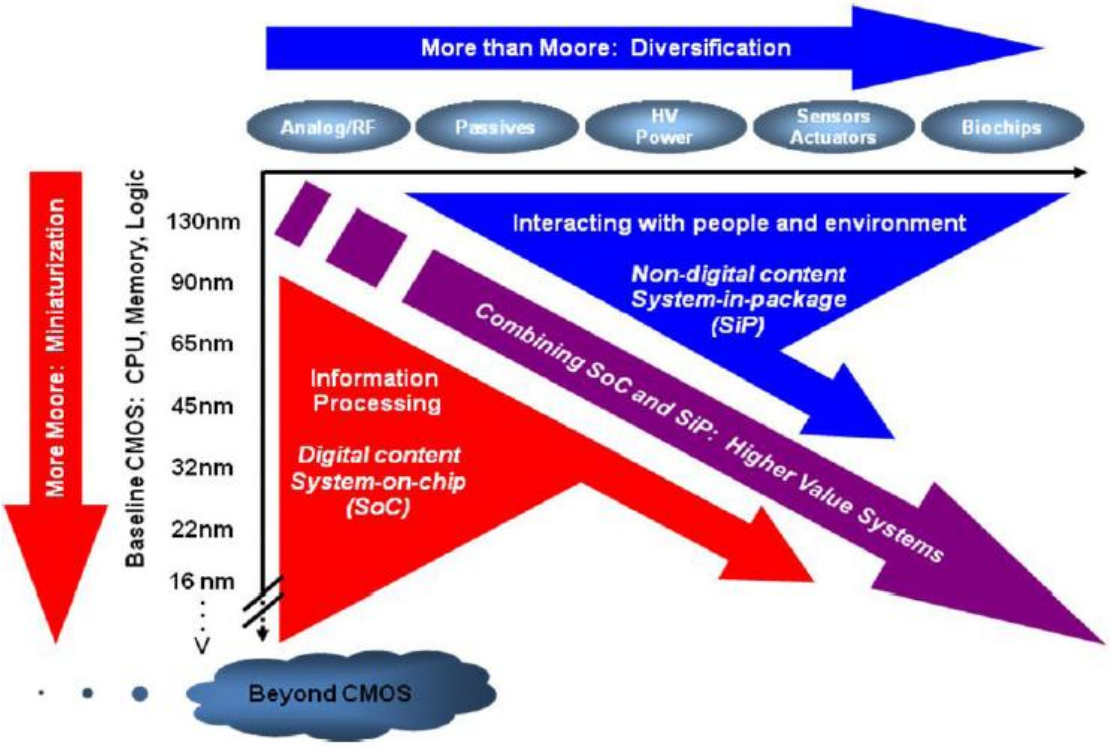


Figure 5 *Moore's Law and More*

Figure 49. "More Moore" field and "More than Moore" field [9].

The basic principle of "More Moore" technological trend is the scaling principle proposed by Dr. Robert H. Dennard in 1974 [53]. The concept is shown in Figure 50. Reducing the channel length of MOSFET leads to undesirable changes in the device characteristics. These changes become significant when the depletion layer surrounding the Source and Drain extend over a large portion of the region in the Silicon substrate under the Gate electrode. And most undesirable short-channel effect reduces *Vth*. MOSFET. In the Dennard's scaling, to decrease channel length the device is scaled by a transformation in three variables: dimension, voltage and doping. First, all linear dimensions are reduced by a unitless scaling factor *k*, i.e. Gate oxide thickness $Tox'=Tox/k$, where primed parameters refer to the new scale down device. This reduction includes vertical dimensions such as gate insulator thickness, junction depth, etc., as well as the horizontal dimensions of channel length and width. Second, the voltages applied to the device are reduced by the same factor (e.g., $Vds' = Vds/k$). Third, the substrate doping concentration is increased, again using the same scaling factor (i.e., $N_A' = k\,N_A$). After that the depletion layer *wd*, *Vth*, and drain current *Id* are reduced as $wd' \approx wd/k$, $Vth' \approx Vth/k$, and $Id' \approx Id/k$, respectively.

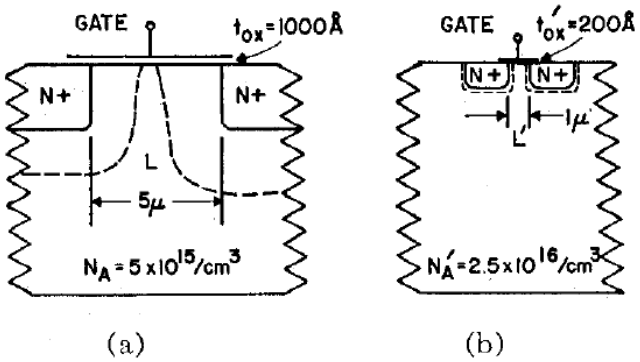


Fig. 1. Illustration of device scaling principles with $\kappa = 5$. (a) Conventional commercially available device structure. (b) Scaled-down device structure.

Figure 50. MOSFET scaling principle [53]. The principle scales channel length *L*, Gate oxide thickness *Tox*, and substrate doping concentration N_A to $L'=L/k$, $Tox'=Tox/k$, and $N_A'= k\,N_A$, respectively.

Trench gate IGBTs are currently mass produced on the wafers of ~200mm diameter. Current structures have several microns of deep trench gate to obtain better trade-off relationship between on-state voltage drop *Vce*(*sat*) and turn-off loss. Miniaturization has not been believed to contribute IGBT performance improvement. However, to improve its manufacturability, certain process compatibility to "More Moore" field semiconductor must be required i.e. IGBT process have to follow "More Moore" process technology. To apply such technology for IGBT fabrication, Cathode side cell structure should be shallower as CMOS structure to keep process uniformity and avoid wafer warpage.

In this section, a scaling principle for trench gate IGBT will be proposed toward CMOS process compatibility. As Dennard's scaling principle, a unitless scaling factor *k* is introduced into "Quasi-2D MOS-ADE" model described before. With CMOS process, high resolution lithographic techniques enable very small trench-trench spacing for IGBT cell structure and it leads significant performance improvement.

5.2 Previous Research for IGBT Performance Limit

Before establishing scaling principle, two researches mentioned about IGBT performance limit are reviewed. One is a theoretical prediction. The other includes experimental results. Both researches show increasing Cathode side injection efficiency

improves IGBT performance.

5.2.1 High precision process approach

Dr. Akio Nakagawa proposed a theory for IGBT performance limit in [54]. In the paper, asymmetrical conduction is assumed to get lowest on-state voltage drop. All of the current flows by electrons and holes contribute only to the conductivity modulation. The phenomenon is realized under the condition that hole diffusion current is equal to hole drift current, and they are flowing opposite direction. In this condition, N-Base carrier distribution is linearly decreasing from Cathode to Anode as shown in Figure 51. The relationship between Cathode side electron injection efficiency and *Vce*(*sat*) is shown in Figure 53. With extremely high electron injection efficiency case, proposed device design has 40nm mesa width. The channel inversion layer is connected to opposite side channel layer, and they form a barrier for holes. The author predicted Silicon IGBT will realize low on-resistance even below Silicon Carbide material limit for over 2kV range as shown in Figure 54.

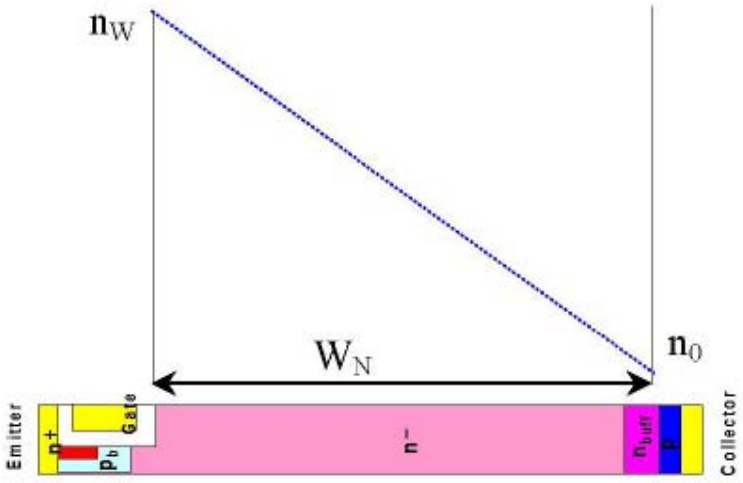


Fig.1 Linearly graded carrier distribution in N-base

Figure 51. N-Base carrier distribution profile for lowest on-state voltage drop [54]. N-Base carrier distribution is linearly decreasing from Cathode to Anode (in this figure, “Collector” to “Emitter”).

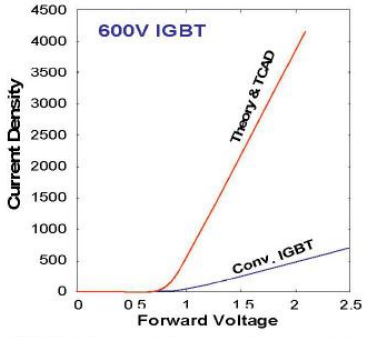


Fig.3 V-I curve comparison between proposed theory, TCAD result and conventional 600V IGBTs. (Theory and TCAD exactly coincides with each other) (a=3.7e18, b=9.39e16)

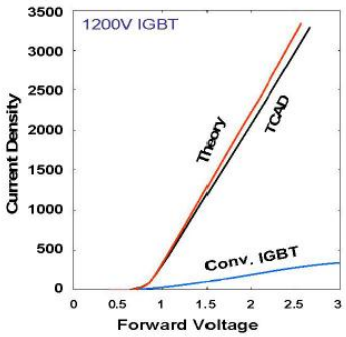


Fig.4 V-I curve comparison between proposed theory, TCAD result and conv. 1.2kV IGBTs.

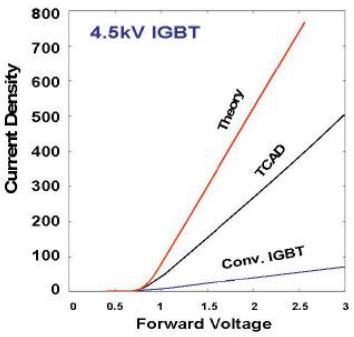


Fig.5 V-I curve comparison between proposed theory, TCAD result and conventional 4.5kV IGBTs.

Figure 52. Simulated Ic-Vc characteristic of IGBT performance limit [54].

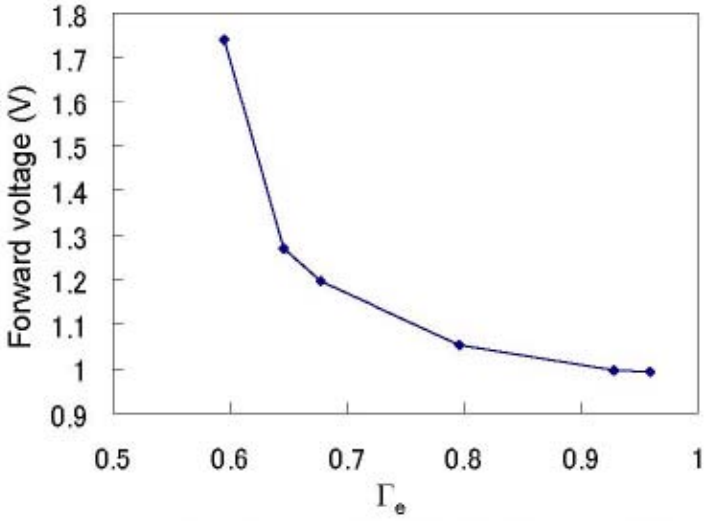


Fig.7 Forward voltage of 600V IGBTs at 500A/cm2 as a function of electron injection efficiency, Γ_e. Γ_e of more than 0.8 is desired.

Figure 53. The relationship between Cathode side injection efficiency and on-state voltage drop [54].

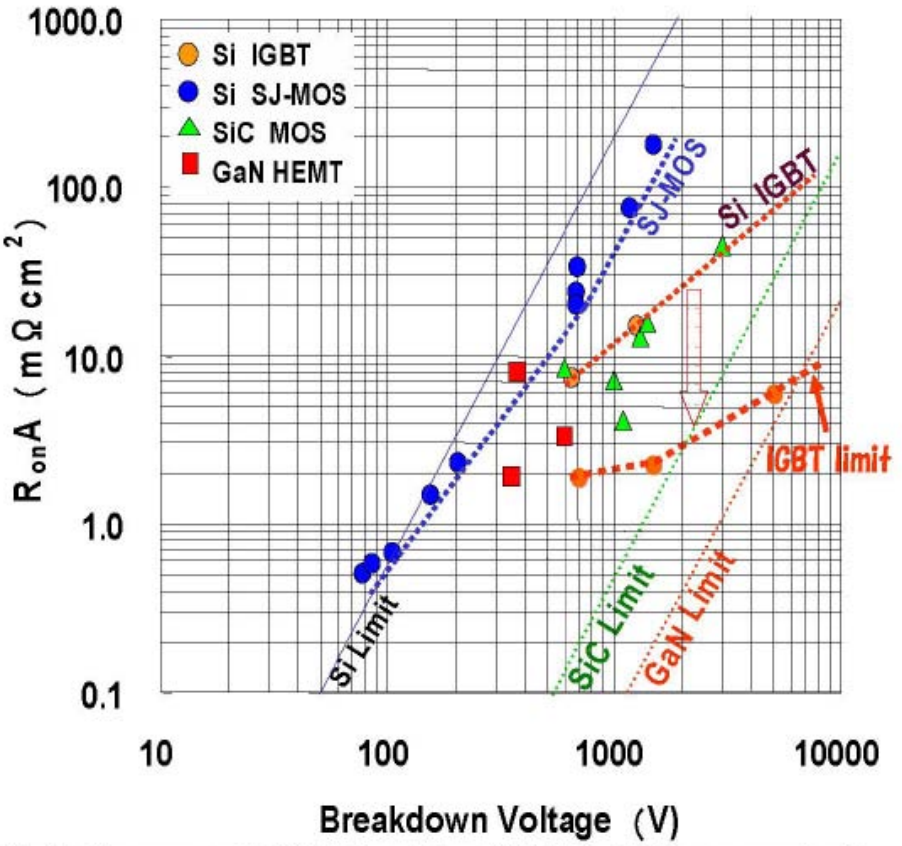


Fig.11 The proposed IGBT, denoted as "IGBT limit," is compared with state of the art devices. Predicted IGBT limit surpasses so called SiC limit for over 2kV range.

Figure 54. IGBT performance limit prediction [54]. The author predicted Silicon IGBT will realize low on-resistance even below SiC limit for over 2kV range.

5.2.2 Conventional process approach

Mr. Manabu Takei developed experimental device which put previous Nakagawa's theory into concrete shape [55]. The device called as DB (Dielectric Barrier)-IGBT has buried layer between P-Base and N-Base as shown in Figure 55. The proposed DB-IGBT structure is equivalent to the trench IGBT with wide and deep trench, and with very narrow mesa width. It enables extreme electron injection efficiency from Cathode side. Simulated N-Base carrier distribution is linearly decreasing from Cathode to Anode as shown in Figure 56, and as Nakagawa's proposal.

Lateral selective epitaxial growth is selected to fabricate experimental device. The epitaxial layer is grown from 1um width Silicon window in buried oxide. After the growth, unnecessary portion is removed by CMP (Chemical Mechanical Polishing). Other than these processes, the device can be fabricated by older planar gate process without

submicron technologies.

Fabricated device shows much better trade-off relationship between on-state voltage drop and turn-off loss as shown in Figure 57.

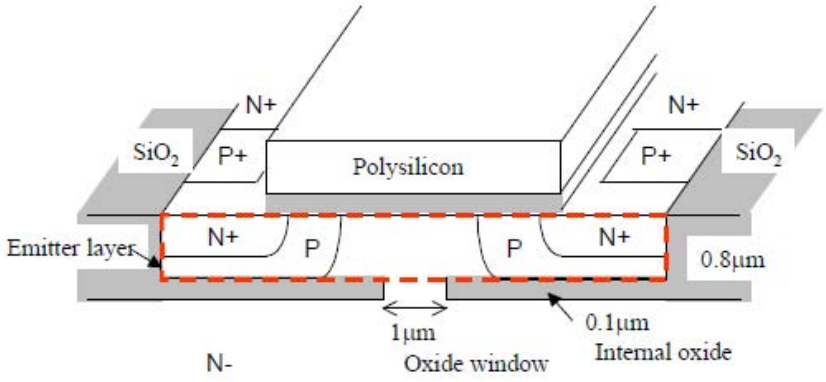


Figure 1. Schematic cross sectional view of a DB-IGBT

Figure 55. Cross sectional view of DB-IGBT [55]. Internal oxide layer is inserted between P-Base and N-Base.

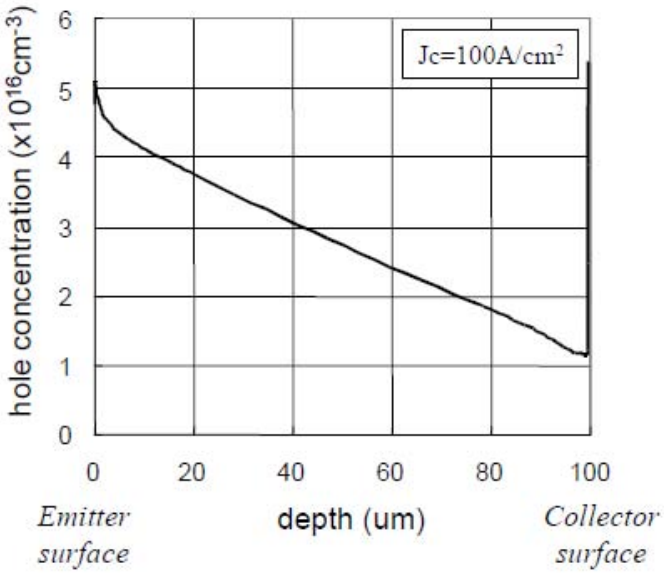


Figure 2. Simulated hole profile of the DB-IGBT under steady on-state

Figure 56. Calculated hole distribution in N-Base [55]. Hole concentration is linearly decreased from Cathode side to Anode side.

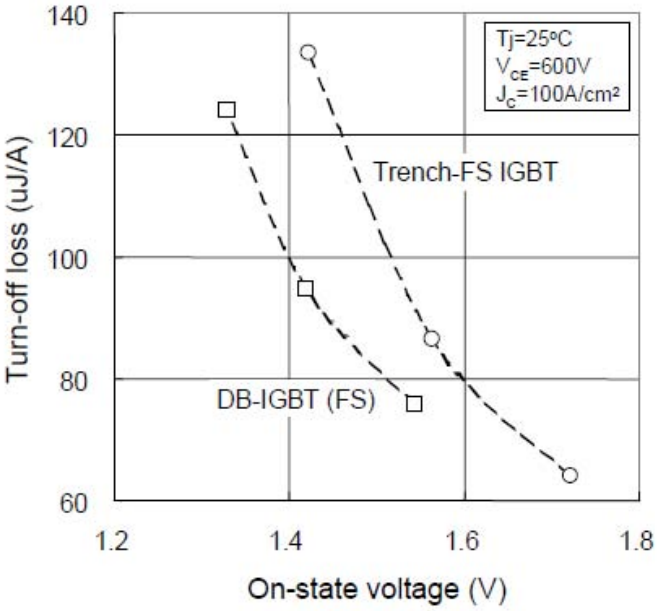


Figure 3. Simulated trade-off relationship between V_{ON} and E_{OFF} of the DB-IGBT and the trench IGBT with FS backside structure

Figure 57. Trede-off relationship between on-state voltage drop and turn-off loss for DB-IGBT [55].

In addition, Mr. Sumitomo showed another concept of the structure with high injection efficiency in ISPSD 2012 [56]. The structure is similar with latest deep trench gate IGBT but very narrow mesa width is realized. Trial fabrication results were also demonstrated.

5.3 IGBT Scaling Principle

In this section, a scaling principle for trench gate IGBT will be proposed toward CMOS process compatibility. The principle is based on general CMOS scaling principle and the formulation of Cathode side injection efficiency described before. Beside high manufacturability, the principle also predicts that scaled down IGBT shows lower *Vce*(*sat*) even with shallower Cathode structure; shallower trench gate and shallower P-base. The principle shows the design trends for shallower Cathode structure with the compatibility for the large diameter wafer process technology, but keeping low on-state voltage drop as current products.

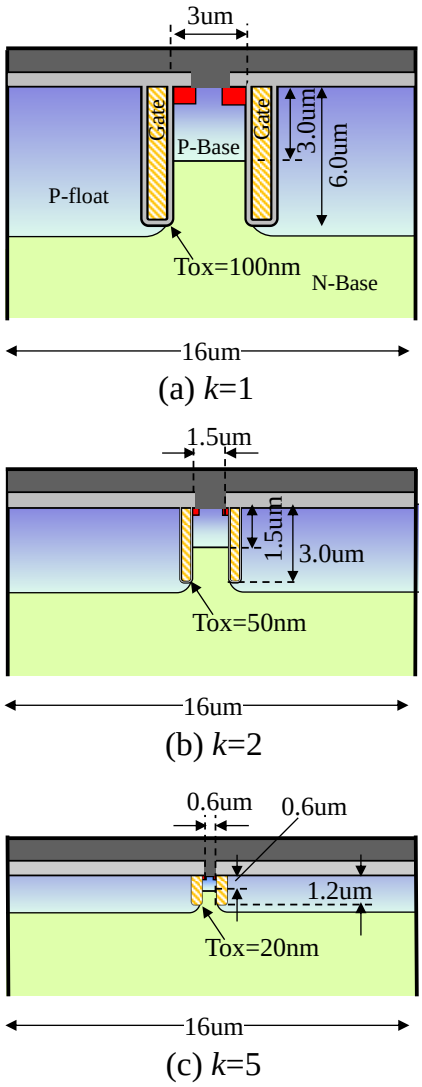


Figure 58. Proposed scaling principle for trench gate IGBT.

Table 5. Proposed scaling principle for trench gate IGBT.

Parameters	Scaling factor
Half cell pitch: *W*	1
Half mesa width: *S*	1/*k*
Trench depth: *DT*	1/*k*
P-Base depth: *Db*	1/*k*
Gate oxide thickness: *Tox*	1/*k*
Gate Voltage: *Vge*	1/*k*, $1/k^2$

The concept of IGBT scaling is shown in Figure 58. Figure 58(a) shows commercially available IGBT that has 6um depth trench gate and 3um depth P-Base. Trench-trench spacing is 3um and cell pitch is 16um. It uses 1000 angstrom gate oxide thickness and P-Base concentration is chosen to give suitable gate threshold voltage *Vth* of around 5V. A unitless scaling factor "*k*" is introduced for some of IGBT structure parameters. Figure 58(b) and (c) show scaled IGBT with *k*=2 and 5 respectively. They have shallower trench gate, shallower P-base, narrower trench-trench spacing and thinner gate oxide scaled by *k*, but keeping unit cell pitch as original to enable same electron injection efficiency from Cathode side. Moreover, scaled IGBT is operated lower gate voltage as "Constant Field" CMOS scaling principle. There are no arrangements in Anode side. Scaled structure parameters are summarized in Table 5.

The basic idea of keeping low on-state voltage drop is that N-Base carrier distribution depends on only Cathode and Anode side injection efficiency. The principle is toward shallower Cathode structure that has same injection efficiency of conventional structure. By applying the principle, the device is scaled by a transformation in two variables: dimension and operation voltage.

About dimension, four parameters are reduced by scaling factor *k*; trench-trench spacing *S*, gate oxide thickness *Tox*, trench depth *DT* and P-base depth *Db*. In the other words, *S*'=*S*/*k*, *Tox*'=*Tox*/*k*, *DT*'=*DT*/*k* and *Db*'=*Db*/*k* where the primed parameters refer to the scaled device. They are toward shallow structure produced by high resolution lithography technique and smaller thermal budget. Unlike CMOS scaling principle, the P-Base doping concentration is unchanged to keep similar saturation current level of conventional structure. As a power device of IGBT needs to conduct large current in MOS channel.

About gate voltage, two type scaling is considered. First, with *Vge*'=*Vge*/*k*, higher electron injection efficiency from Cathode side and performance improvement is estimated. In this case applied electric field for gate oxide is same as conventional structure. Second, with $Vge'=Vge/k^2$, same electron injection efficiency from Cathode side can be obtained.

5.4 Scaling Theory

The theory for the principle is delivered from (19).

$$\frac{\mu_p}{\mu_n}\left(\left(\frac{\varepsilon_{ox}\mu_{acc}V_{ge}}{T_{ox}q\mu_n n(x)S}+1\right)^{-1}+1\right)\gamma_n-1=\frac{2qD_p}{J}\frac{S}{W}\frac{dn(x)}{dx} \qquad (19)$$

Equation 19 indicates that the scaled device has same injection efficiency of original device with following conditions:

$$\frac{\varepsilon_{ox}\mu_{acc}V_{ge}}{T_{ox}q\mu_n n(x)S} = const. \tag{65}$$

$$\frac{S}{W}\frac{dn(x)}{dx} = const. \tag{66}$$

In (65), the gate voltage *Vge*, the gate oxide thickness *Tox* and the trench-trench spacing *S* are scaled by the principle. By applying the scaling principle as Figure 58 and $Vge'=Vge/k^2$ of Table 1, (65) keeps constant with varied *k*. By applying the scaling principle with $Vge'=Vge/k$ of Table 1, (65) becomes smaller with increasing *k*. Thus,

$$\begin{gathered}\frac{\varepsilon_{ox}\mu_{acc}V_{ge}{}'}{T_{ox}{}'q\mu_n n(x)S'} = const.\ \left(V_{ge}{}' = \frac{V_{ge}}{k^2}\right) \\ \frac{\varepsilon_{ox}\mu_{acc}V_{ge}{}'}{T_{ox}{}'q\mu_n n(x)S'} > \frac{\varepsilon_{ox}\mu_{acc}V_{ge}}{T_{ox}q\mu_n n(x)S}\ \left(V_{ge}{}' = \frac{V_{ge}}{k}\right)\end{gathered} \tag{67}$$

In (66), the trench-trench spacing *S* is scaled but cell pitch *W* is not changed by the scaling. And the divergence of carrier concentration in mesa region *dn/dx* is increased by factor *k*, $(dn/dx)'=k(dn/dx)$ as shown in Figure 59. So the right hand side of (19) is unchanged by the scaling principle.

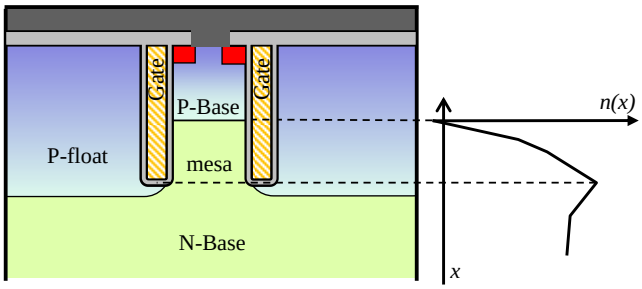
$$\frac{S'}{W}\frac{dn'(x)}{dx} = \frac{S}{W}\frac{dn(x)}{dx} \tag{68}$$

By applying (67) and (68) into (19), following results are obtained.

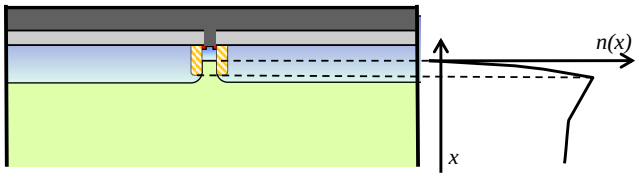
$$\begin{gathered}\gamma_n{}' = const.\ \left(V_{ge}{}' = \frac{V_{ge}}{k^2}\right) \\ \gamma_n{}' > \gamma_n\ \left(V_{ge}{}' = \frac{V_{ge}}{k}\right)\end{gathered} \tag{69}$$

Formulas (69) mean that higher γ_n than original device can be obtained by increasing *k* by applying $Vge'=Vge/k$. It leads higher carrier concentration in N-Base Cathode side and lower on-state voltage drop. It means device characteristic improvement can be done by

scaling down Cathode structure and applying same electric field for gate oxide.



(a) Conventional structure



(b) Shallow structure

Figure 59. Comparison of mesa region carrier distribution.

Other electrical characteristics are changed by introducing scaling factor *k* as Table 2: Gate-emitter capacitance *Cge* is unchanged because *Tox'=Tox/k* and *Db'=Db/k*. Gate charge *Qg* is reduced by factor *k*, *Qg'=Qg/k*. Contact metal current density J_{Metal} is increased by factor *k*, $J_{Metal}=k\ J_{Metal}$ because contact hole width is reduced by factor *k*. Electro migration should be considered for large *k*.

One characteristic that the principle fails to scale is threshold voltage. Threshold voltage *Vth* can be calculated as following

$$V_{th} = \frac{\sqrt{2\varepsilon_0 \varepsilon_{Si} q N_A \varphi_S}}{C_{ox}} + \varphi_S \qquad (70)$$

Where *Cox* is gate capacitance per unit area, N_A is acceptor concentration in P-Base and $\varphi_S$is surface potential of MOS channel. *Vth* is reduced because gate capacitance per unit area is increased by the scaling principle as *Cox'=kCox*. But *Vth* is not scaled by *k* exactly even if N_A and $\varphi_S$are unchanged.

Therefore, saturation current is not also scaled. MOS gate saturation current is formed approximately as following

$$I_{n,sat} = \frac{W_{Channel}}{D_b} C_{ox} \frac{1}{2} \left(V_{ge} - V_{th}\right)^2 \qquad (71)$$

Vge and *Db* are scaled as *Vge'=Vge/k* and *Db'=Db/k*, respectively. From (70) and (71), saturation current is slightly increased by the scaling.

Finally, the scaling factors are summarized in Table 6.

Table 6. Scaling factors by proposed scaling principle.

Parameters	Scaling factor	
Gate voltage: *Vge*	$1/k^2$	1/k
Half cell pitch: *W*	1	
Half mesa width: *S*	1/*k*	
N-Emitter width: *We*	1/*k*	
Trench depth: *DT*	1/*k*	
P-Base depth: *Db*	1/*k*	
N-Emitter depth: *De*	1/*k*	
Half contact width: *Wc*	1/*k*	
Gate oxide thickness: *Tox*	1/*k*	
Gate-Emitter capacitance: *Cge*	1	
Gate-Collector capacitance: *Cgc*	1	
Collector-Emitter capacitance: *Cce*	1/*k*	
Current density in contact hole: J_{Metal}	*k*	
Gate charge: *Qg*	$1/k^2$	1/*k*
Electron injection efficiency: γ_n	1	>1
Stored carrier density: *n=p*	1	>1

5.5 Calculation Results

Established scaling principle was verified by TCAD calculation. Two types of scaling principle were compared as shown in Figure 60. In the "simple scaling" approach, scaling is applied for all structure dimensions including the cell pitch *W*. The channel density is increased in "simple scaling" approach, as Power MOSFET improvement direction. On the other hand, the cell pitch *W* is constant in the proposed scaling principle. The channel density is constant in the proposed scaling principle.

Ic-Vce, *Ic-Vge*, turn-off with inductive load, and short circuit calculation were performed. 1200V PT-IGBT structure was used for the motif. Cross sectional view of base structure i.e., structure for k=1, is shown in Figure 61. Base structure parameters are shown in Table 7. Scaled structure parameters are shown in Table 8. The thickness from trench bottom to Anode electrode is 120um for all devices. Total device thickness is different by the scaling factor k because trench depth depends on k. For example, wafer thickness are 126um and 121.2um for k=1 and k=5, respectively.

As previous section, *Synopsys Sentaurus Device* version E-2010.12 was used for TCAD calculation. In this verification, structure generation tool *Sentaurus Structure Editor* was used to create the FEM structure instead of process simulator. Same physical models as section 4.5 were used and lattice self heating effect was taken into account for short circuit calculation.

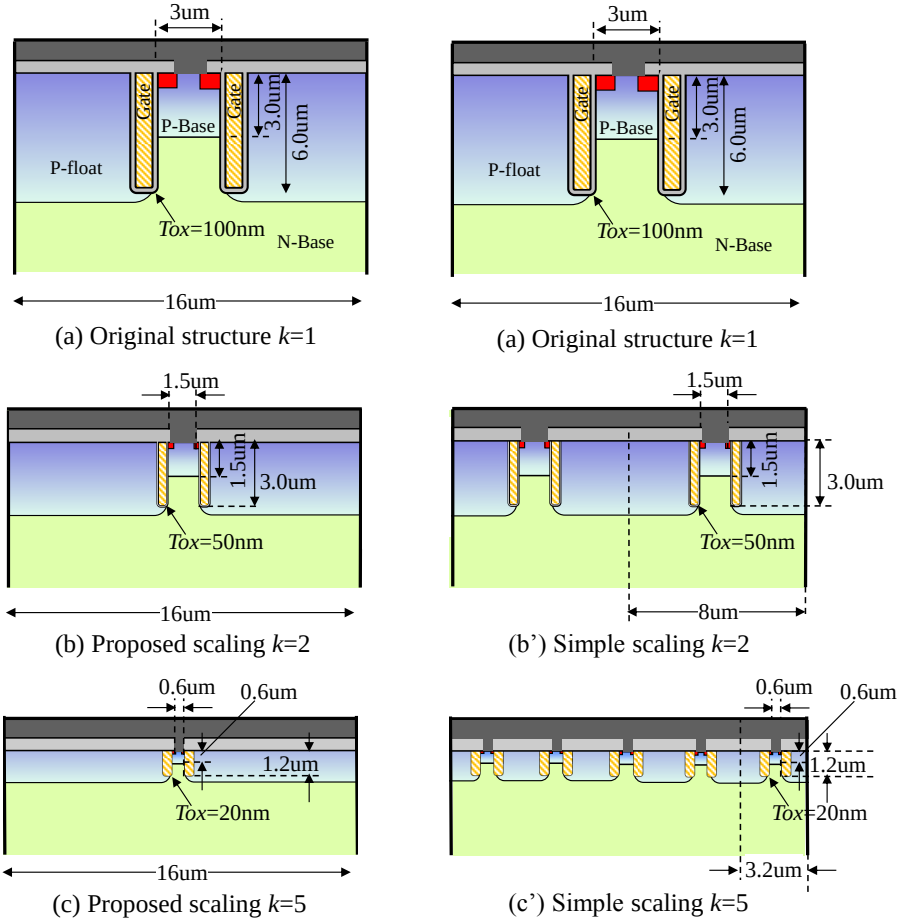


Figure 60. Proposed scaling (Left side) and Simple scaling (Right side). In proposed scaling, cell pitch is constant. In simple scaling, cell pitch is also scaled.

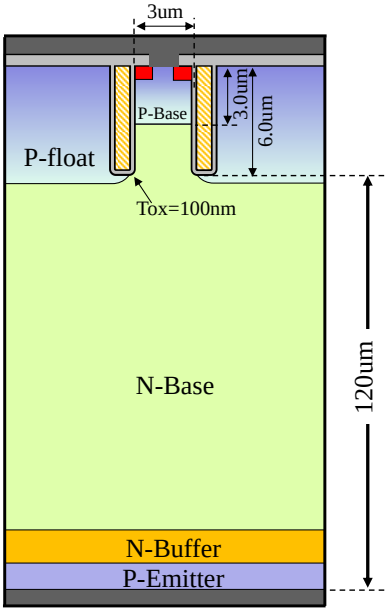


Figure 61. Base structure for scaling principle verification. 1200V PT-IGBT structure is used for the motif.

Table 7. Base structure parameters used for the verification.

Parameters	
N-base concentration	$8x10^{13}/cm^3$
N-base thickness	120um
Half cell pitch: *W*	8.0um
Half mesa width: *S*	1.5um
P-base surface concentration	$1x10^{17}/cm^2$
P-base thickness: *Dp*	3.0um
Trench depth: *DT*	6.0um
Gate oxide thickness: *Tox*	1000angstrom
P-emitter concentration	$1x10^{17}/cm^3$
P-emitter thickness	1.0um
N-buffer concentration	$9x10^{16}/cm^3$
N-buffer thickness	1.0um

Table 8. Structure parameters used for the scaling principle verification.

	k =1	k =2	k =3	k =4	k =5
Half cell pitch: *W*[um] (Half cell pitch for simple scaling[um])	8.0	8.0 (4.0)	8.0 (2.67)	8.0 (2.0)	8.0 (1.6)
Half mesa width: *S*[um]	1.5	0.75	0.5	0.375	0.3
Trench depth: *DT*[um]	6.0	3.0	2.0	1.5	1.2
Gate oxide thickness: *Tox*[angstrom]	1000	500	333	250	200
Gate Voltage: *Vge*[V] for $1/k^2$ scaling	15.0	3.75	1.67	0.94	0.60
Gate Voltage: *Vge*[V] for $1/k$ scaling	15.0	7.5	5.0	3.75	3.0

Ic-*Vge* characteristics of scaled devices are shown in Figure 62. *Vth* is decreased by scale down. *gm* is increased due to thinner gate oxide and shorter channel length.

Ic-*Vc* characteristics of scaled devices with scaled gate voltage $Vge'=Vge/k^2$, i.e. scaled electric field in gate oxide $Eox'=Eox/k$, are shown in Figure 63. In proposed scaling, the curves for k=1 and 2 show complete agreement but more scaled devices show smaller saturation current. It is due to scaling induced *Vth* shift as (70) and saturation current drop as (71). On the other hand, in simple scaling, *Vce*(*sat*) becomes higher with scale down.

In proposed scaling, N-Base carrier distribution for k=2 is kept as k=1 as shown in Figure 64. Without saturation current drop, proposed scaling rule is proved very well. In simple scaling, Cathode side carrier concentration becomes lower with scale down.

Ic-*Vc* characteristics with scaled gate voltage $Vge'=Vge/k$, i.e. constant electric field in gate oxide $Eox'=Eox$, are shown in Figure 65 and Figure 66. In proposed scaling, lower *Vce(sat)* is obtained by scale down. On the other hand, in simple scaling, *Vce*(*sat*) becomes higher with scale down. In proposed scaling, *Vce(sat)* improvement is observed especially under high temperature condition.

On-state carrier distribution in N-Base region is shown in Figure 67 and Figure 68. In proposed scaling, N-Base carrier distribution is improved, so that Cathode side carrier concentration is increased, by scale down. Higher γ_n and lower *Vce(sat)* are achieved by scale down even with shallower trench, as mentioned in previous section. In simple scaling, Cathode side carrier concentration becomes lower with scale down.

Turn-off waveforms of scaled devices with constant electric field in gate oxide as $Eox'=Eox$, are shown in Figure 69. External gate resistance is constant. Scaled devices show slight delays because the difference of gate voltage and threshold voltage, *Vge*-*Vth*, is not scaled by k exactly. Because of *Cge* and *Cgc* are constant, the length of miller plateau is constant too.

Short-circuit waveforms of scaled devices are shown in Figure 70. In this calculation,

half of rated gate voltage was applied to avoid thermal runaway. Scaled device shows slightly higher saturation current because *Vge-Vth* is not scaled by *k* exactly. Oscillation is observed in larger *k*.

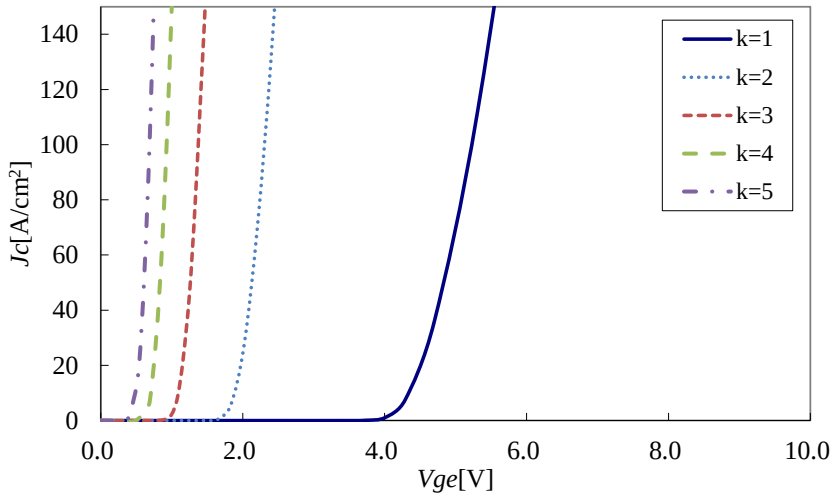


Figure 62. *Ic-Vge* characteristics for scaled devices. Scaled devices show lower *Vth* and higher *gm*.

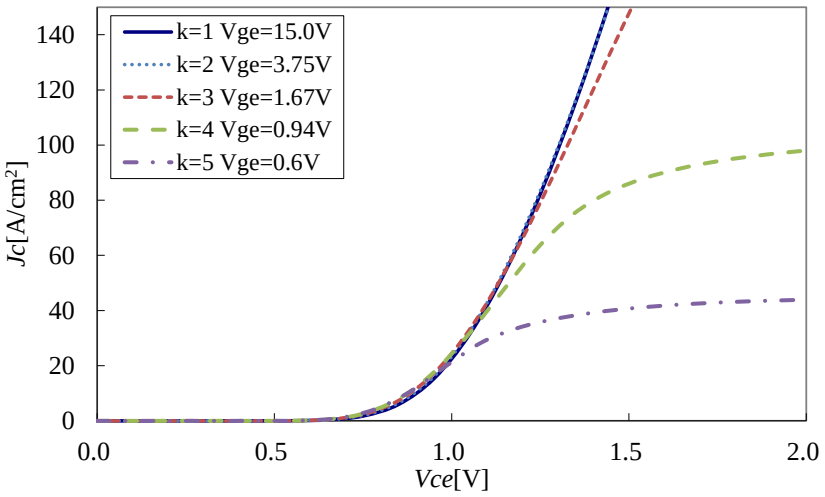
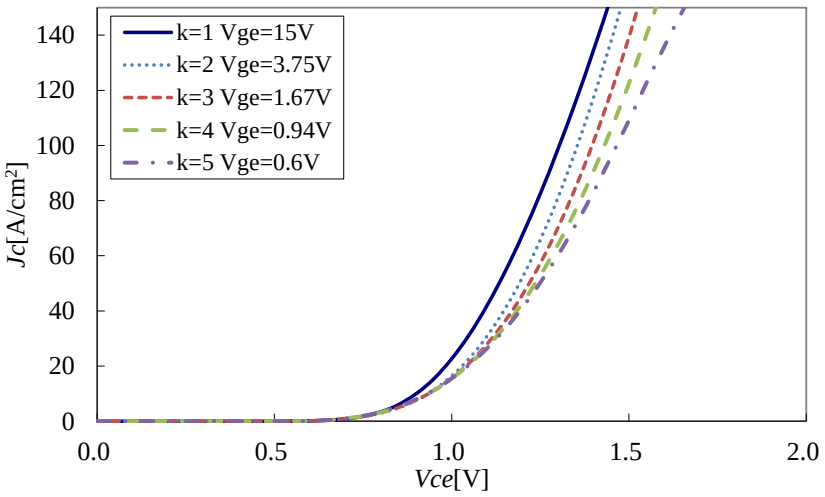
$Vge'=Vge/k^2$	
Proposed scaling T=300K	
Simple scaling T=300K	

Figure 63. Calculated *Ic*-*Vc* characteristics of scaled devices with scaled electric field in gate oxide as *Eox*'=*Eox*/*k*. In proposed scaling, *k*=1 and 2 show good agreement but more scaled devices show lower saturation current. In simple scaling, *Vce*(sat) becomes higher with increasing scaling factor *k*.

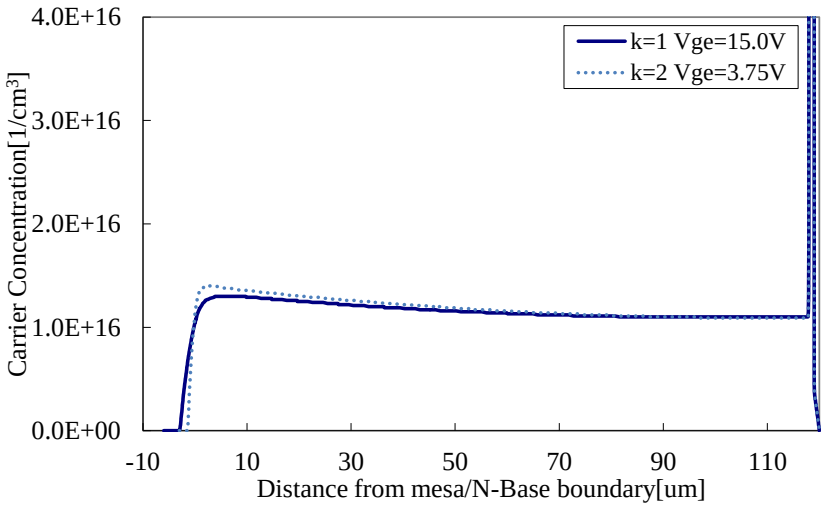
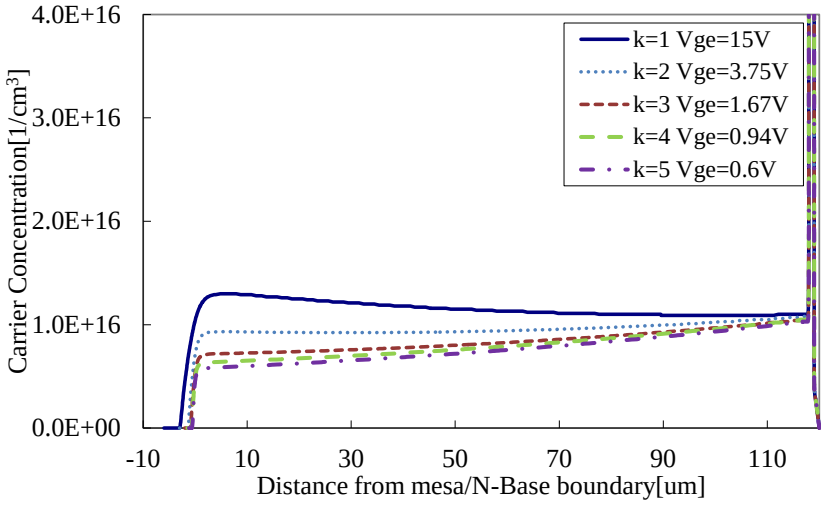
$Vge'=Vge/k^2$	
Proposed scaling T=300K	
Simple scaling T=300K	

Figure 64. Calculated carrier distribution in N-Base region of scaled devices with scaled electric field in gate oxide as *Eox*'=*Eox*/*k*. The zero point of horizontal scale is set to mesa/N-Base boundary. In proposed scaling, similar carrier distribution is obtained instead of scale down. In simple scaling, Cathode side carrier concentration becomes lower with increasing scaling factor *k*.

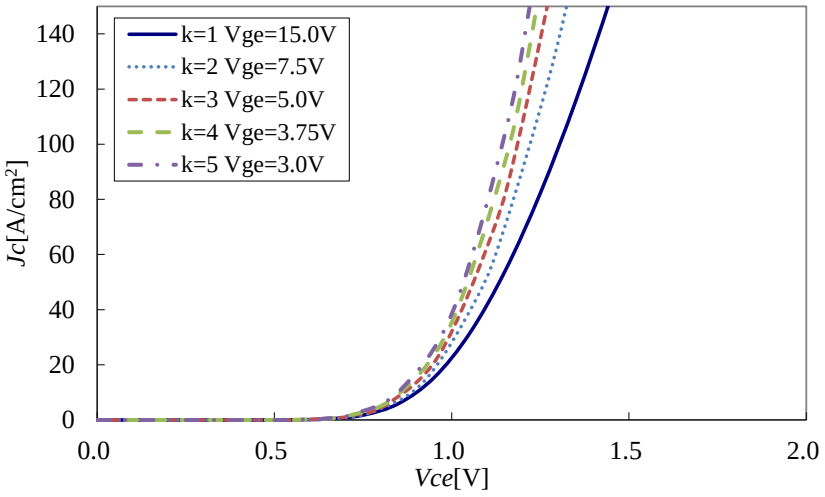
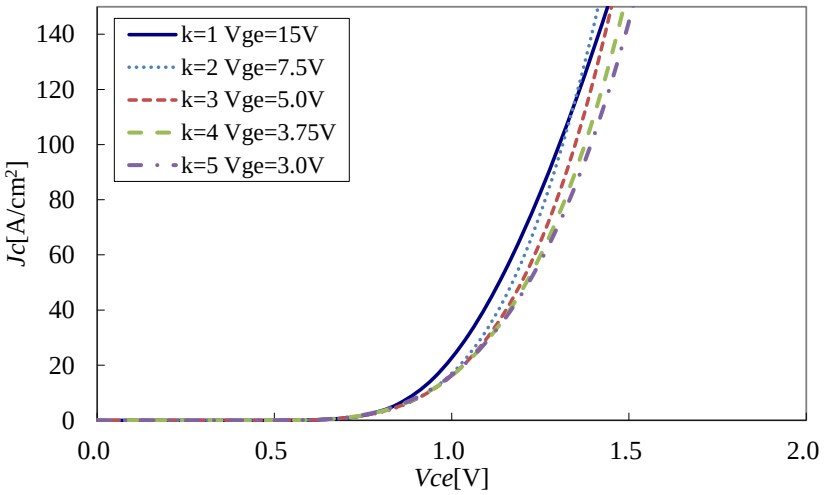
Vge'=Vge/k	
Proposed scaling T=300K	
Simple scaling T=300K	

Figure 65. Calculated *Ic-Vc* characteristics of scaled devices with constant electric field in gate oxide as *Eox'=Eox*. In proposed scaling, *Vce*(*sat*) is improved by increasing scaling factor *k*. In simple scaling, *Vce*(sat) becomes higher with increasing scaling factor *k*.

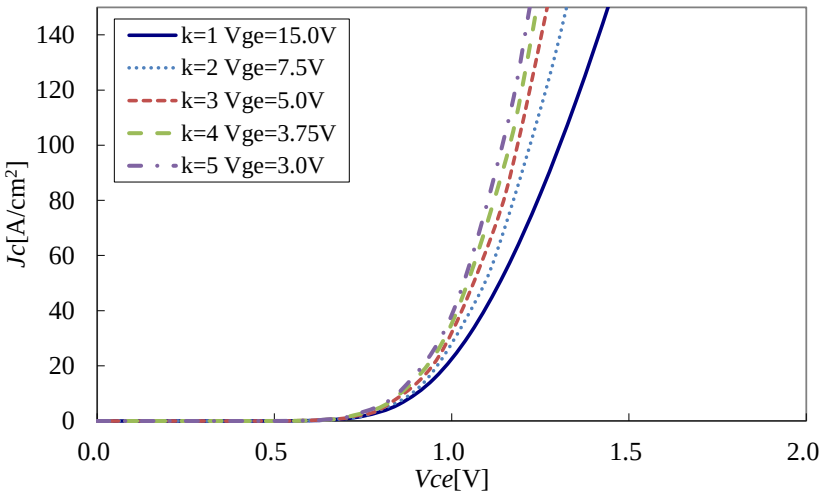
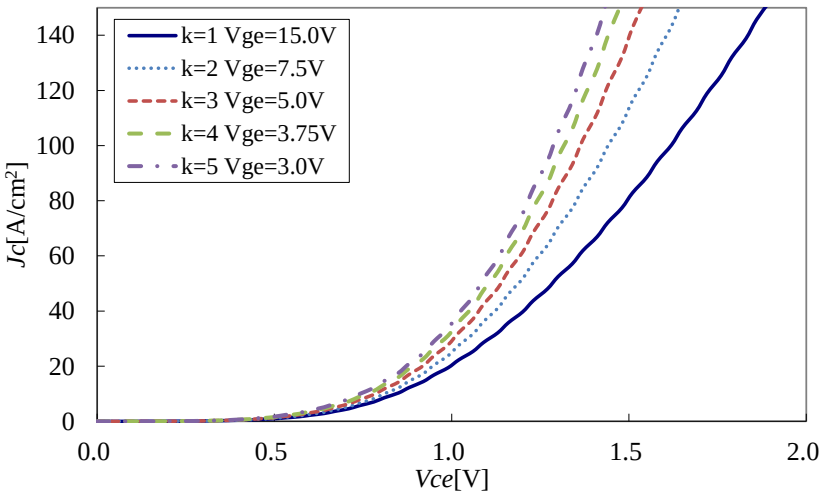
Vge'=Vge/k	
Proposed scaling T=300K	
Proposed scaling T=450K	

Figure 66. Calculated *Ic*-*Vc* characteristics of proposed scaling devices with constant electric field in gate oxide as *Eox*'=*Eox*. In higher temperature condition, *Vce*(*sat*) improved especially.

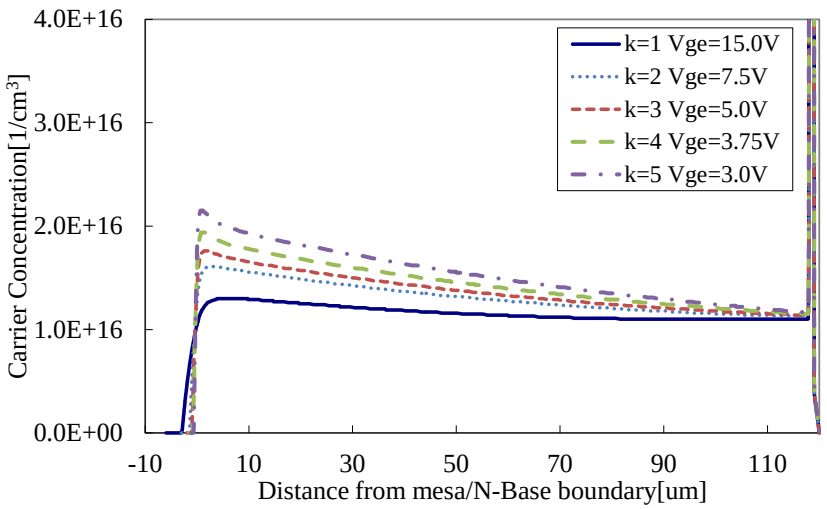
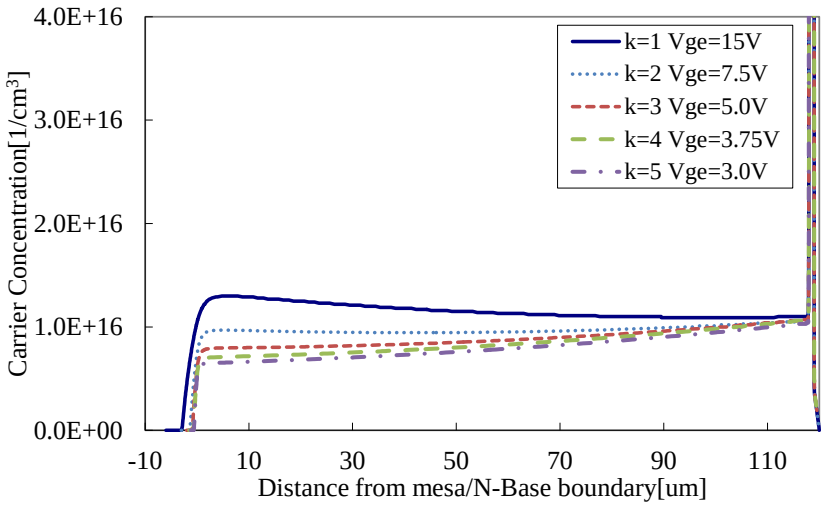
Vge'=Vge/k	
Proposed scaling T=300K	
Simple scaling T=300K	

Figure 67. Calculated carrier distribution in N-Base region for scaling factor *k*=1 to 5. The zero point of horizontal scale is set to mesa/N-Base boundary. In proposed scaling, Cathode side carrier concentration is increased by scale down. In simple scaling, Cathode side carrier concentration becomes lower with increasing scaling factor *k*.

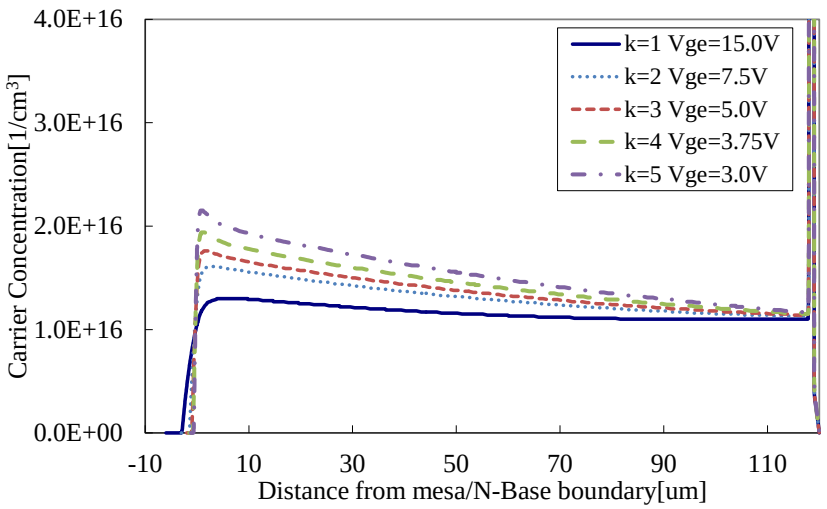
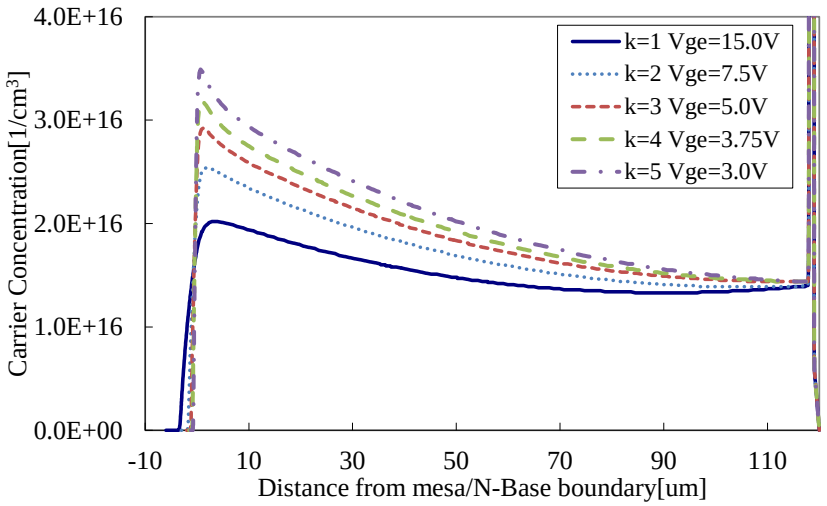
Vge'=Vge/k	
Proposed scaling T=300K	
Proposed scaling T=450K	

Figure 68. Calculated carrier distribution in N-Base region for proposed scaling device with T=300K and 450K. The zero point of horizontal scale is set to mesa/N-Base boundary. In proposed scaling, Cathode side carrier concentration is increased by scale down especially in high temperature condition.

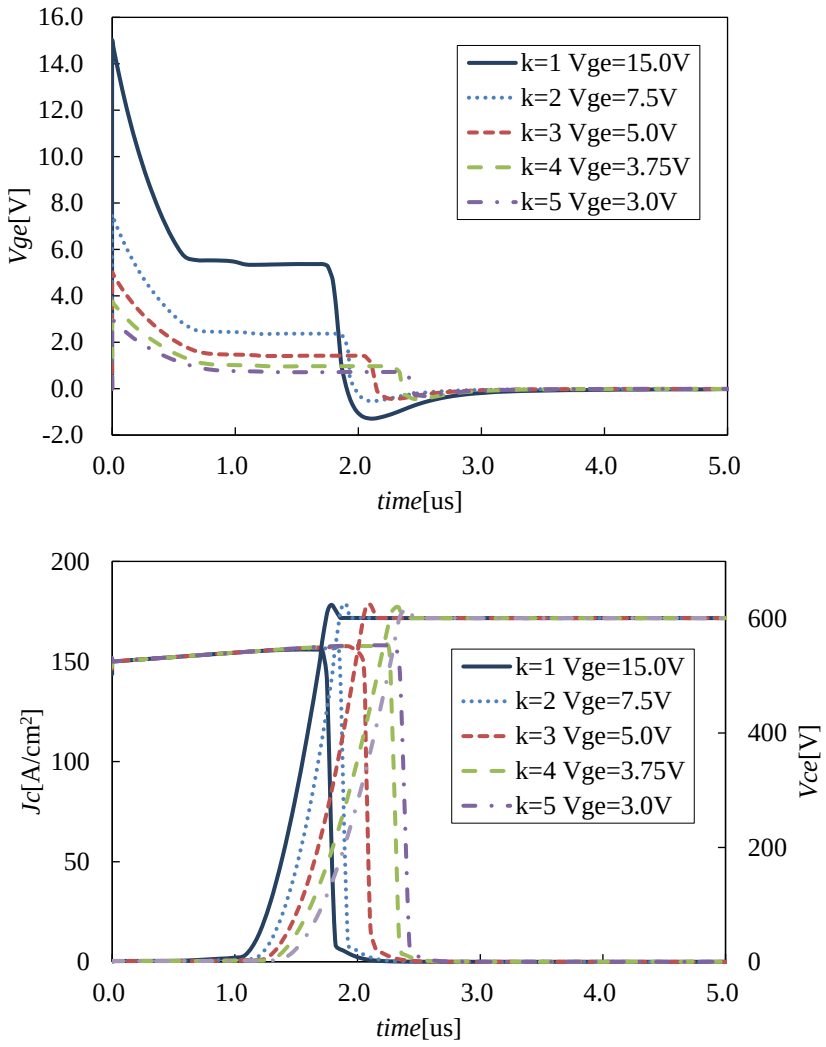


Figure 69. Calculated Turn-off characteristics of proposed scaling devices with constant electric field in gate oxide as *Eox*'=*Eox*. Device active area is 1cm^2. Same external gate resistance of 10ohm is used.

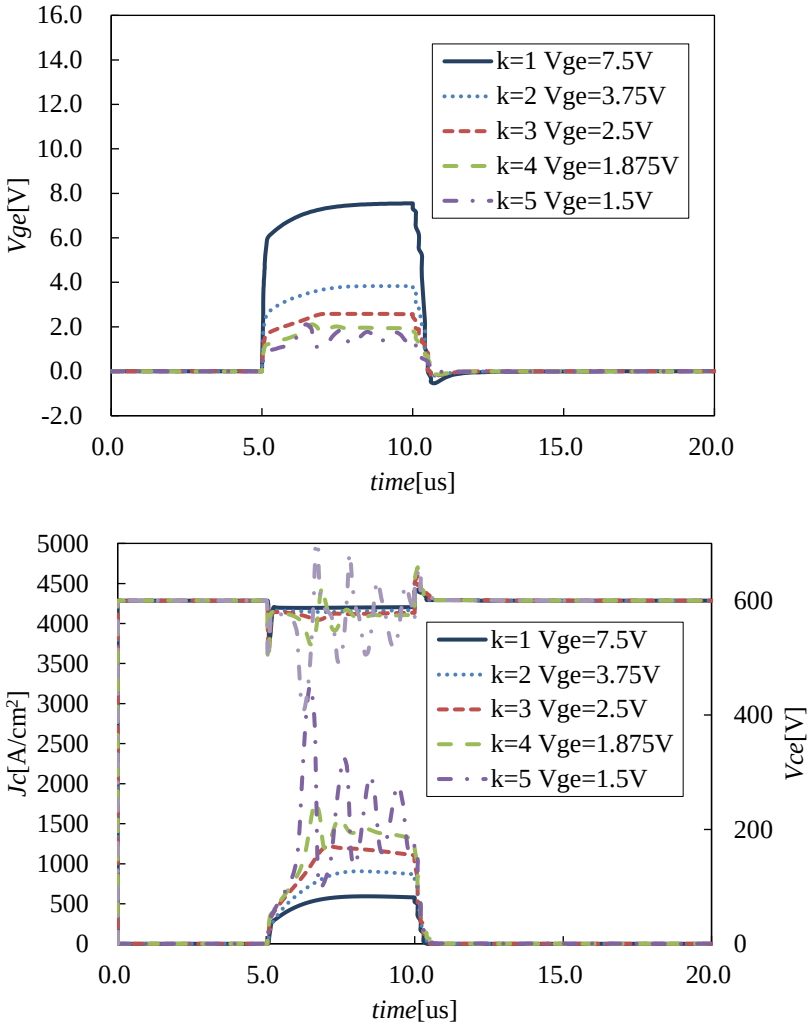


Figure 70. Calculated short-circuit waveforms of proposed scaling devices with constant electric field in gate oxide as *Eox*'=*Eox*. Lower gate voltage was applied to avoid thermal runaway in this calculation.

5.6 Discussion

5.6.1 Saturation current optimization

In previous calculation, *Vth* was set to lower than usual to confirm the scaling principle with scaled electric field in gate oxide as *Eox*'=*Eox*/*k* as Figure 63. Moreover, *Vth* is reduced as less than *Vth*/*k* due to surface potential φ_S. In result, saturation currents were higher especially scaled devices and rated short-circuit calculation could not be finished without thermal runaway. To apply the proposed scaling principle to actual device, *Vth* should be set to limit saturation current but not increase channel resistance for rated current.

Vth can be scaled by following calculation from (70).

$$V_{th} = \frac{\sqrt{2\varepsilon_0\varepsilon_{Si}qN_A\varphi_S}}{C_{ox}} + \varphi_S \tag{70}$$

$$N_A = \frac{{C_{ox}}^2(V_{th} - \varphi_S)^2}{2\varepsilon_0\varepsilon_{Si}q\varphi_S} \tag{72}$$

By applying the scaling rule,

$$N_A{}' = \frac{(kC_{ox})^2(V_{th}/k - \varphi_S)^2}{2\varepsilon_0\varepsilon_{Si}q\varphi_S} \tag{73}$$

Another calculation was performed with adjusted *Vth* to realize optimized saturation current around 1000-1500A/cm^2. Optimized P-Base surface concentration is shown in Table 9.

Table 9. P-Base surface concentration for *Vth* adjustment.

	k =1	*k* =2	*k* =3	*k* =4	*k* =5
P-Base surface concentration[1/cm^3]	2.8x10^{17}	3.5x10^{17}	4.0x10^{17}	4.4x10^{17}	4.8x10^{17}

Ic-*Vge* characteristics of scaled devices are shown in Figure 71. *Vth* is just scaled as scaling factor *k*. *gm* is still higher due to thinner gate oxide and shorter channel length.

Ic-*Vc* characteristics with scaled gate voltage *Vge'=Vge/k*, i.e. constant electric field in gate oxide *Eox'=Eox*, are shown in Figure 72. Lower *Vce(sat)* is achieved by scale down even with higher and just scaled *Vth*.

Turn-off waveforms of scaled devices with constant electric field in gate oxide as *Eox'=Eox*, are shown in Figure 73. External gate resistance is constant. All devices show almost same turn-off characteristics by *Vth* adjustment.

Short-circuit waveforms of scaled devices are shown in Figure 74. Same saturation current is realized among all scaled devices, and no oscillation is appeared even for higher scaled devices.

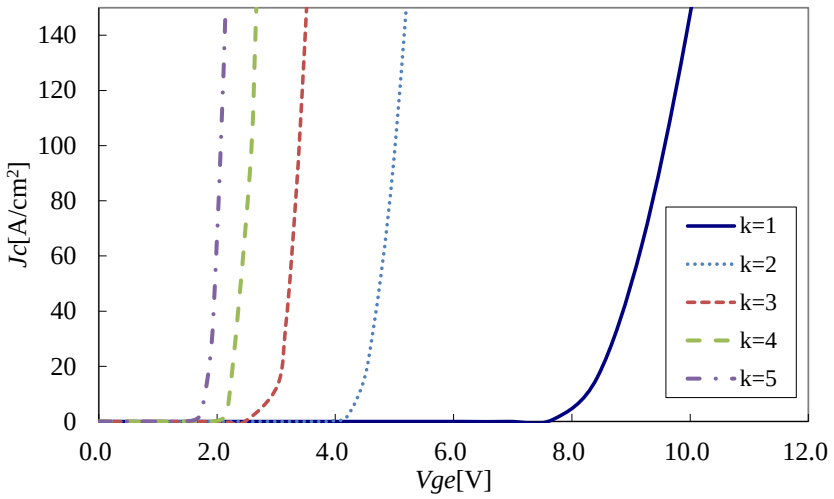


Figure 71. *Ic-Vge* characteristics for scaled devices with *Vth* adjustment. Scaled devices show higher *gm*.

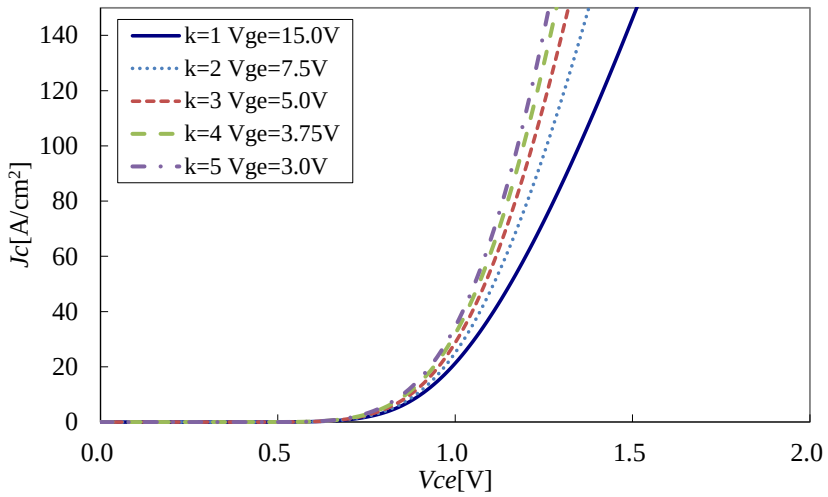


Figure 72. Calculated *Ic-Vc* characteristics of scaled devices with *Vth* adjustment and constant electric field in gate oxide as *Eox'=Eox*. *Vce*(*sat*) is improved by increasing scaling factor *k*.

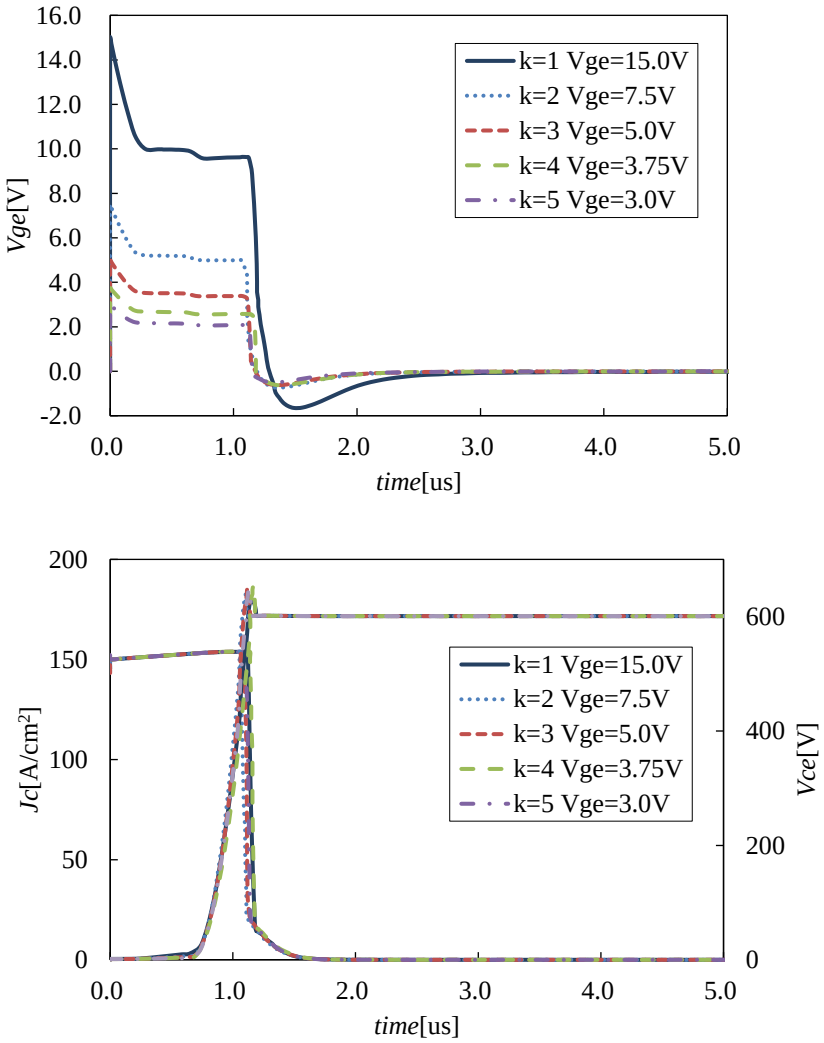


Figure 73. Calculated Turn-off characteristics of scaled devices with *Vth* adjustment. Device active area is 1cm^2. Applied gate voltage is scaled by keeping constant electric field in gate oxide as *Eox*'=*Eox*. All devices show almost same turn-off characteristics by *Vth* adjustment.

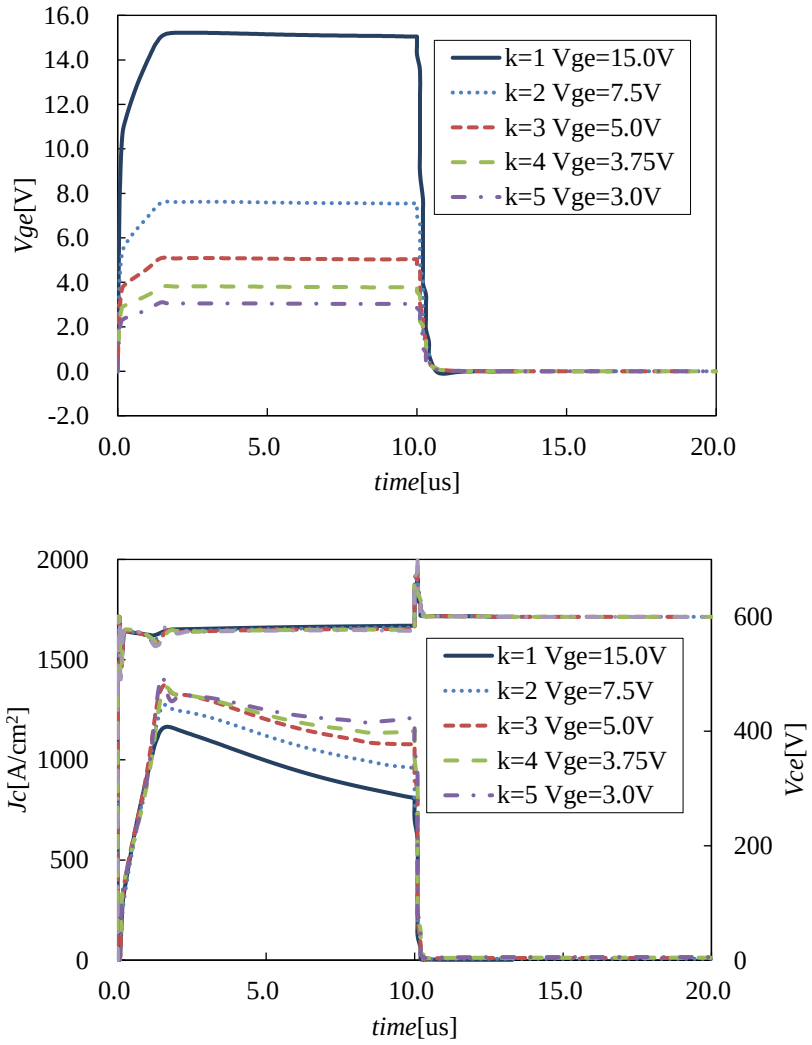


Figure 74. Calculated short-circuit waveforms of scaled devices with *Vth* adjustment. Applied gate voltage is scaled by keeping constant electric field in gate oxide as *Eox*'=*Eox*. Lower and similar saturation current are realized. No thermal runaway was occurred.

5.6.2 Electric Field in Gate Oxide

One concern for the scaled device is the reliability of thinner gate oxide. To confirm it, maximum electric field values were measured with static breakdown simulation between Anode and Cathode as shown in Figure 75. No critical increasing for the electric field was observed.

Another scaling option keeping gate oxide thickness as original can be applied as discussed in the next paragraph.

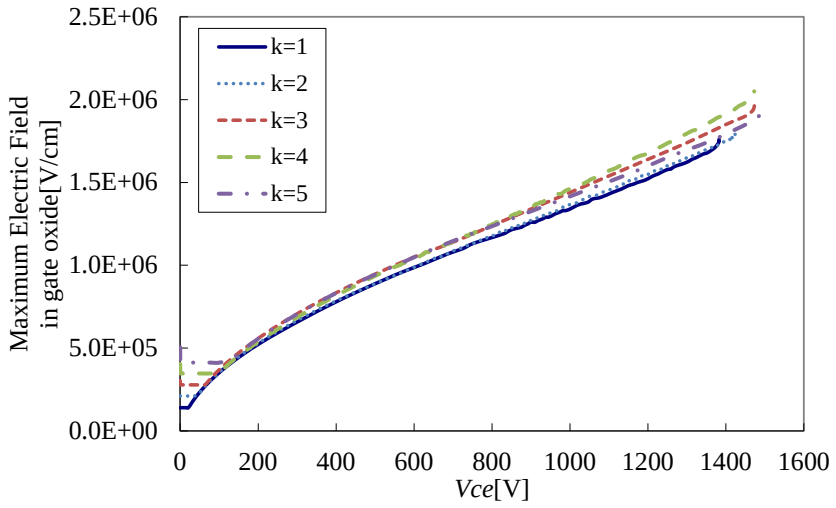


Figure 75. Simulated maximum electric field in gate oxide for static breakdown.

5.6.3 Another Scaling Option

In highly scaled device, thinner gate oxide and lower gate voltage could be issues of reliability. For example, tunneling current must be concerned via very thin gate oxide less than 5nm. And lower gate voltage could cause malfunction due to parasitic capacitances and external noise. Another scaling option might be effective to avoid these issues. By Quasi-2D MOS-ADE model of (19), another scaling principle can be delivered without decreasing gate oxide thickness and gate voltage.

$$\frac{\mu_p}{\mu_n}\left(\left(\frac{\varepsilon_{ox}\mu_{acc}V_{ge}}{T_{ox}q\mu_n n(x)S}+1\right)^{-1}+1\right)\gamma_n - 1 = \frac{2qD_p}{J}\frac{S}{W}\frac{dn(x)}{dx} \qquad (19)$$

With keeping gate oxide thickness and gate voltage, the left hand side of (19) is changed by scaled trench-trench spacing S.

$$\frac{\varepsilon_{ox}\mu_{acc}V_{ge}}{T_{ox}q\mu_n n(x)S'} > \frac{\varepsilon_{ox}\mu_{acc}V_{ge}}{T_{ox}q\mu_n n(x)S} \qquad (74)$$

By applying (74) into (19), following results are obtained.

$$\gamma_n{}' > \gamma_n \qquad (75)$$

This scaling principle is summarized in Table 10.

Table 10. Another scaling factors by proposed scaling principle.

Parameters	Scaling factor
Gate voltage: *Vge*	1
Half cell pitch: *W*	1
Half mesa width: *S*	1/*k*
N-Emitter width: *We*	1/*k*
Trench depth: *DT*	1/*k*
P-Base depth: *Db*	1/*k*
N-Emitter depth: *De*	1/*k*
Half contact width: *Wc*	1/*k*
Gate oxide thickness: *Tox*	1
Gate-Emitter capacitance: *Cge*	1
Gate-Collector capacitance: *Cgc*	1
Collector-Emitter capacitance: *Cce*	1/*k*
Current density in contact hole: J_{Metal}	*k*
Gate charge: *Qg*	1/*k*
Electron injection efficiency: γ_n	>1
Stored carrier density: *n*=*p*	>1

5.6.4 Process Flow

By applying the scaling principle, the trench gate and doping layers become shallower. It enables to eliminate thermal budget. For *k*=5 or more, P-Float layer and P-Base layer can be formed by ion implantation and very short thermal process such as laser anneal or flash anneal. Following list and Figure 76 show an example of “cell first” process flow.

1. Preparing N- doped wafer. Resistivity is chosen by the rated voltage.
2. Oxidation to protect contamination by next deposition.
3. (Edge termination structure formation)
4. Deposition thick oxide as masking material for trench etching.
5. Photolithography for trench gate pattern.
6. Masking layer formation by anisotropic etching for oxide.
7. Stripping photoresist.

8. Trench formation by anisotropic etching for Silicon.
9. Stripping mask oxide.
10. (If required) Sacrificed oxidation to remove etching damage.
11. Gate oxidation.
12. Gate electrode formation by PolySilicon deposition.
13. Removing surface PolySilicon by etching or CMP (Chemical Mechanical Polishing).
14. Photolithography for P-Float pattern.
15. P-Float layer formation by Boron implantation (High energy).
16. Stripping photoresist.
17. Photolithography for P-Base pattern.
18. P-Base layer formation by Boron implantation (Medium energy).
19. Stripping photoresist
20. P-Float and P-Base activation by RTA (Rapid Thermal Anneal), flash anneal, or laser anneal.
21. Photolithography for N-Emitter pattern.
22. N-Emitter formation by Arsenic or Phosphorus implantation.
23. N-Emitter activation by RTA (Rapid Thermal Anneal), flash anneal, or laser anneal.
24. Deposition BPSG or PSG for inter layer.
25. (If required) Gettering to recover the bulk carrier lifetime.
26. Photolithography for contact pattern.
27. Contact hole formation by anisotropic etching.
28. Stripping photoresist
29. P+ layer formation by Boron or BF2 implantation (Low energy).
30. P+ activation by RTA (Rapid Thermal Anneal), flash anneal, or laser anneal.
31. Front metal formation.
32. Photolithography for metal pattern.
33. Etching metal to divide Gate, Emitter electrode and edge termination.
34. Passivation formation.
35. Wafer thinning by backside grinding, polishing and/or etching.
36. N-Buffer formation by Phosphorus implantation for backside (High energy).
37. P-Emitter formation by Boron implantation for backside.
38. N-Buffer and P-Emitter activation by RTA (Rapid Thermal Anneal), flash anneal, or laser anneal.
39. Back metal formation.

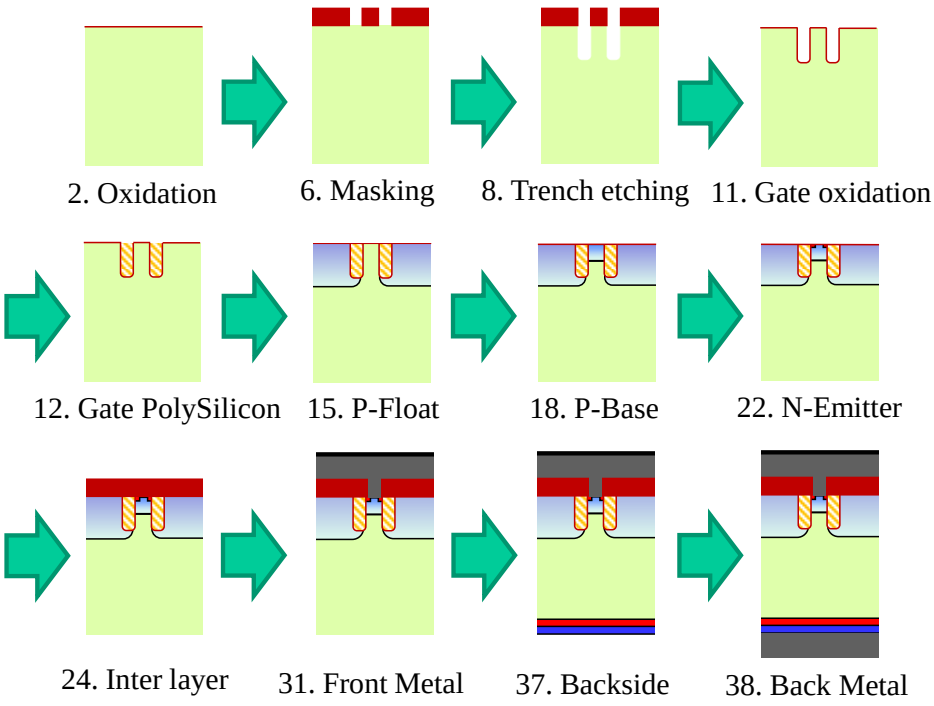


Figure 76. An example of “cell first” process flow.

Because of smaller thermal budget for cell formation process, P-Emitter and N-Buffer can be formed in advance. Following list and Figure 77 show an example of “cell last” process flow.

1. Preparing N- doped wafer. Resistivity is chosen by the rated voltage.
2. Wafer thinning by backside grinding, polishing and/or etching.
3. N-Buffer formation by Phosphorus implantation for backside (High energy).
4. P-Emitter formation by Boron implantation for backside.
5. N-Buffer and P-Emitter activation by RTA (Rapid Thermal Anneal), flash anneal, or laser anneal.
6. (Flip the wafer for cell formation process. If needed, supporting material is attached to backside.)
7. Oxidation to protect contamination by next deposition.
8. (Edge termination structure formation)
9. Deposition thick oxide as masking material for trench etching.
10. Photolithography for trench gate pattern.
11. Masking layer formation by anisotropic etching for oxide.

12. Stripping photoresist.
13. Trench formation by anisotropic etching for Silicon.
14. Stripping mask oxide.
15. (If required) Sacrificed oxidation to remove etching damage.
16. Gate oxidation.
17. Gate electrode formation by PolySilicon deposition.
18. Removing surface PolySilicon by etching or CMP (Chemical Mechanical Polishing).
19. Photolithography for P-Float pattern.
20. P-Float layer formation by Boron implantation (High energy).
21. Stripping photoresist.
22. Photolithography for P-Base pattern.
23. P-Base layer formation by Boron implantation (Medium energy).
24. Stripping photoresist
25. P-Float and P-Base activation by RTA (Rapid Thermal Anneal), flash anneal, or laser anneal.
26. Photolithography for N-Emitter pattern.
27. N-Emitter formation by Arsenic or Phosphorus implantation.
28. N-Emitter activation by RTA (Rapid Thermal Anneal), flash anneal, or laser anneal.
29. Deposition BPSG or PSG for inter layer.
30. (If required) Gettering to recover the bulk carrier lifetime.
31. Photolithography for contact pattern.
32. Contact hole formation by anisotropic etching.
33. Stripping photoresist
34. P+ layer formation by Boron or BF2 implantation (Low energy).
35. P+ activation by RTA (Rapid Thermal Anneal), flash anneal, or laser anneal.
36. Front metal formation.
37. Photolithography for metal pattern.
38. Etching metal to divide Gate, Emitter electrode and edge termination.
39. Passivation formation.
40. Back metal formation.

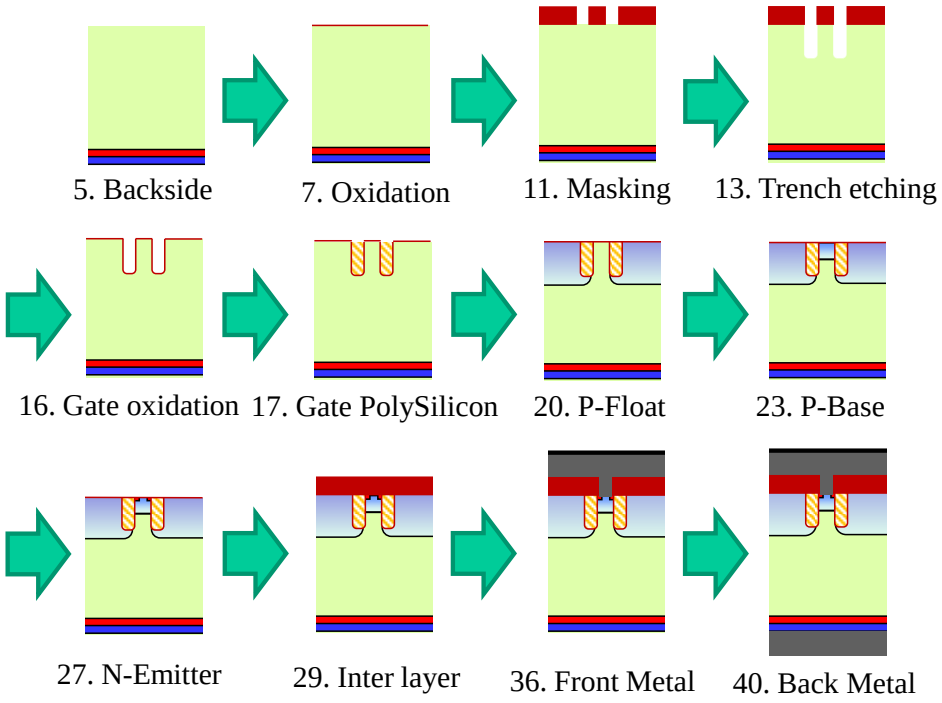


Figure 77. An example of “cell last” process flow.

5.7 Summary

New scaling principle for Trench gate IGBT was proposed. The structure oriented analytical model previously discussed in this dissertation was extended to the scaling principle. The principle is theoretically established and can apply to wide range of device structures. By the principle, IGBT cell structure becomes shallow so that its diffusion layers and trench depths is diminished to 1/*k* where current depths are several microns. The principle was proved by two-dimensional TCAD simulation. Same on-state characteristic as conventional design can be obtained even by shallow structure except lower saturation current. On-state characteristic can be also improved by applying higher gate voltage where electric field is same as conventional design. After adjusting *Vth*, turn-off and short circuit characteristics are not affected by scale down at all.

The principle has large impact for new IGBT development. Scaled IGBT can be aligned for CMOS wafer process with highly reduced thermal budget, and mass produced in CMOS manufacturing line with high productivity.

6 The Future: Shallow Trench IGBT Advantages and Related Issues

In this section, further performance improvement of IGBT is discussed with aiming higher power density. A design methodology based on the proposed compact model and the scaling principle will be shown.

6.1 Cathode Side Structure Optimization

Ic-*Vce* characteristic of 1200V PT-IGBT calculated by the proposed compact model is shown in Figure 78. Currently the rated current density of 1200V IGBT is about 100-150A/cm^2. With aiming higher current density, for example 450A/cm^2, higher voltage drop should be a problem. Higher on-state voltage drop generates large heat and it have to be exhausted toward ambient via heat sink.

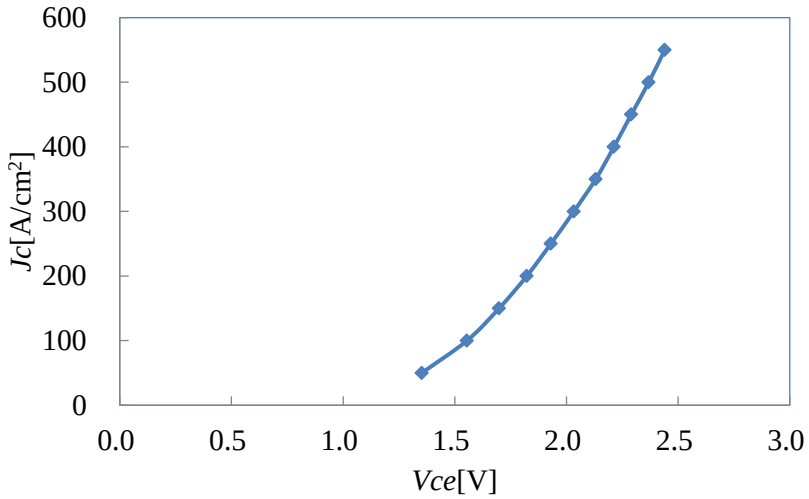


Figure 78. *Ic*-*Vce* characteristic for 1200V PT-IGBT calculated by the proposed compact model. To improve power density, *Vce*(*sat*) must be reduced in high current density region.

As described in section 4, on-state voltage drop consists of four portions, N-Base, mesa region, MOS channel, and built-in potential. The potions depend on the current density as shown in Figure 79. N-Base voltage drop is dominant in high current density region.

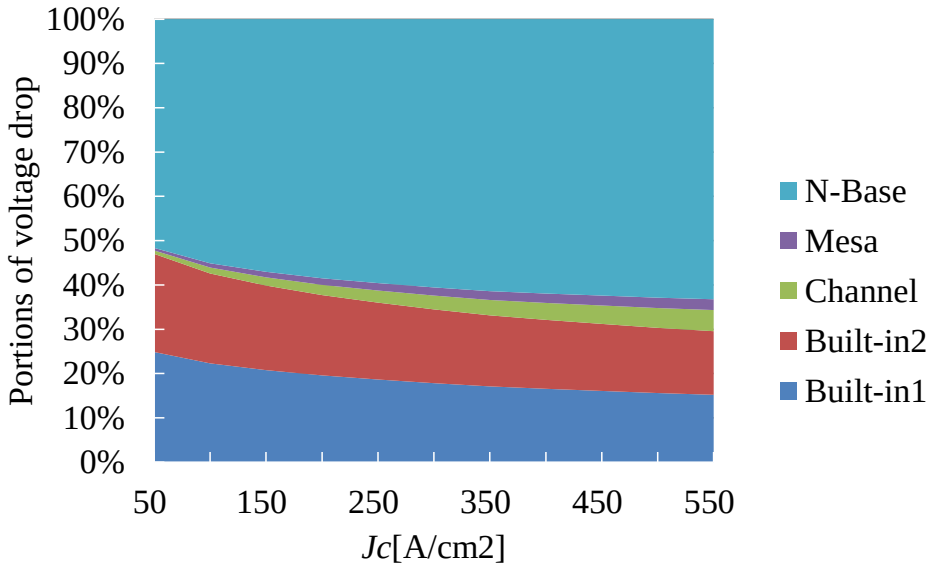


Figure 79. Portions of voltage drop at 300K for 1200V PT-IGBT calculated by the proposed compact model. N-Base voltage drop is dominant in high current density region.

For example, at 450A/cm^2, the total voltage drop is 2.29V and the N-Base voltage drop is 1.43V. The portion of the N-Base voltage drop is 62% of the total voltage drop. Now, let's consider reducing the N-Base voltage drop as half as current structure. Higher stored carrier concentration should be required. The estimated carrier concentration can be calculated by following sequence.

$$J_n = q\mu_n nE + qD_n \frac{dn}{dx} \tag{3}$$

$$J_p = q\mu_p pE - qD_p \frac{dp}{dx} \tag{4}$$

In high current region, carrier distribution profile becomes to be flat. So,

$$\frac{dn}{dx} = \frac{dp}{dx} = 0 \tag{76}$$

$$J = J_n + J_p = q(\mu_p + \mu_n)nE = q(\mu_p + \mu_n)n\frac{V_{N-Base}}{t_{N-Base}} \tag{77}$$

By (77), n=2.51x10^{16}cm^{-3} is delivered to obtain $V_{N\text{-}Base}$=0.715V for J=450A/cm^2 at

300K.

Next, move to design the Cathode structure. In high current region, γ_p and γ_n can be assumed to 0.25 and 0.75 respectively. By Quasi-2D MOS-ADE model, estimated carrier concentration at N-Base edge can be calculated comprehensively with various values of *W* and *k* because the model formulation is simple. Following graphs can be drawn.

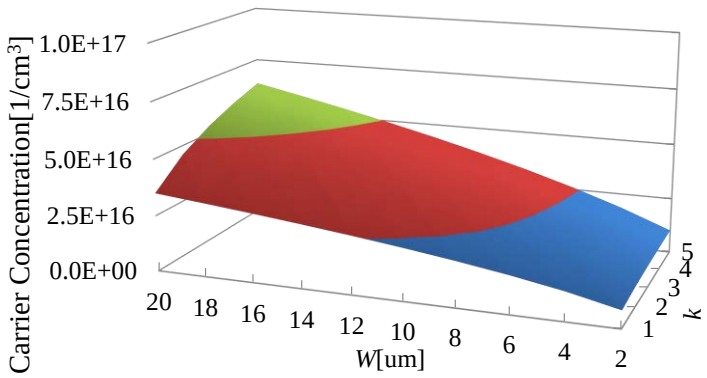
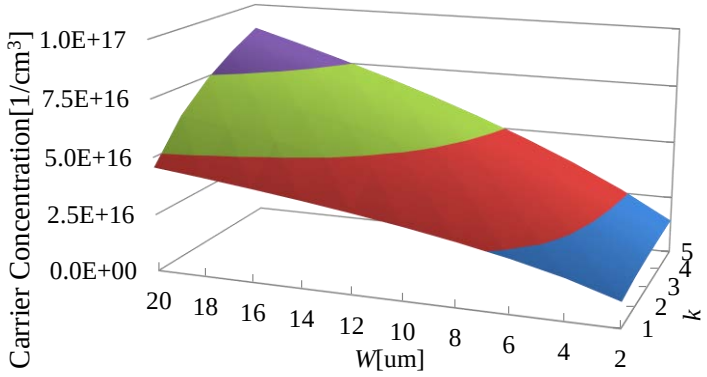
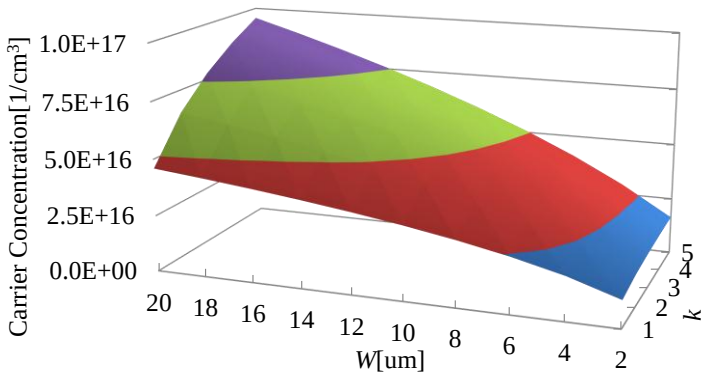
T=300K	
T=400K	
T=450K	

Figure 80. Relationship between cell pitch *W*, scaling factor *k* and carrier concentration n at N-Base/mesa boundary for 450A/cm^2. The electron injection efficiency is assumed as 0.75.

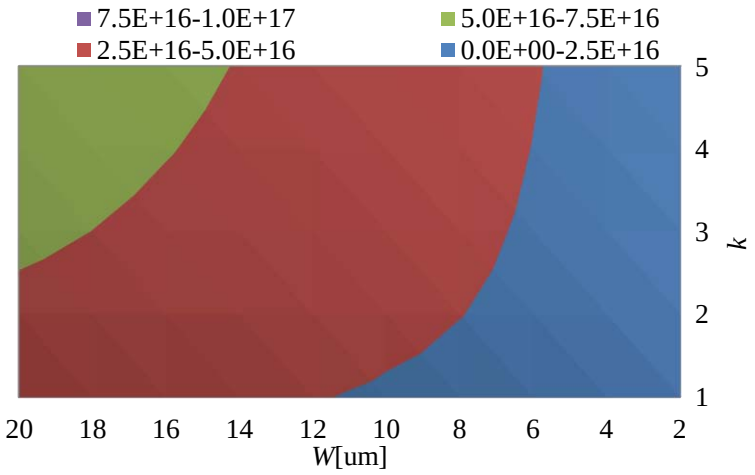
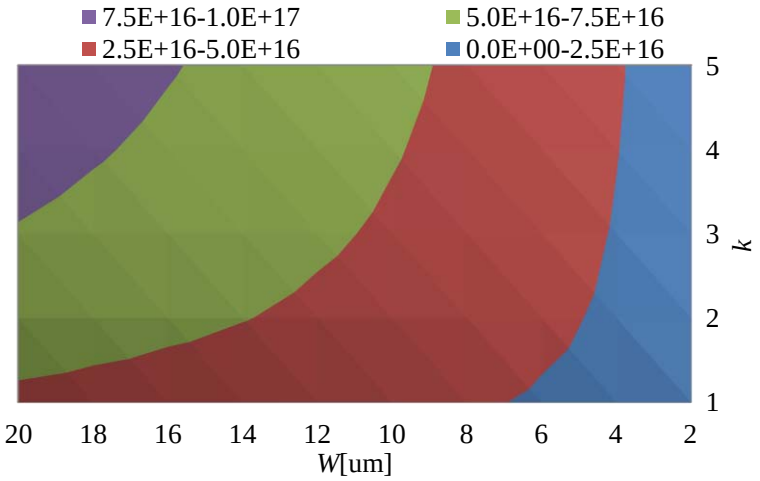
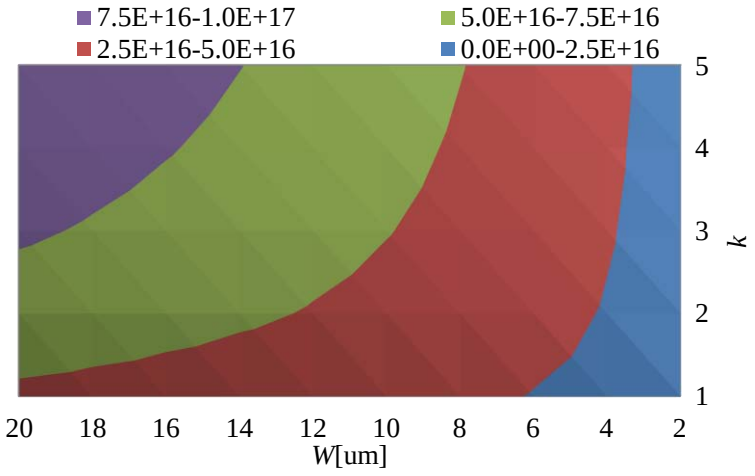
T=300K	
T=400K	
T=450K	

Figure 81. Relationship between cell pitch *W*, scaling factor *k* and carrier concentration n at N-Base/mesa boundary for 450A/cm^2. The electron injection efficiency is assumed as 0.75.

The graphs show clear designing guidelines. By Figure 80 and Figure 81, Cathode structure parameter relationship for n=2.51x10^{16}cm^{-3} can be delivered. The line is about the boundary between blue area (less than 2.5 x10^{16}cm^{-3}) and brown (more than 2.5 x10^{16}cm^{-3}) area. For example, with scaling factor k=1, W should be more than 12um. With scaling factor k=5, W should be more than 6um.

6.2 High Temperature Advantage of Shallow Trench IGBT

By Figure 80 and Figure 81, a relationship between carrier concentration and temperature, i.e., injection efficiency and temperature is observed. Higher injection efficiency can be obtained by higher temperature, especially with large k. The temperature dependency is summarized in Figure 82. The phenomena can be explained by Quasi-2D MOS-ADE model.

$$\frac{\mu_p}{\mu_n}\left(\left(\frac{\varepsilon_{ox}\mu_{acc}V_{ge}}{T_{ox}q\mu_n n(x)S}+1\right)^{-1}+1\right)\gamma_n-1=\frac{2qD_p}{J}\frac{S}{W}\frac{dn(x)}{dx} \qquad (19)$$

S is trench-trench spacing which is scaled as $S'=S/k$. For large k, (19) can be modified as follows.

$$\gamma_n=\frac{\mu_n}{\mu_p}\left(1+\frac{2qD_p}{J}\frac{S}{W}\frac{dn(x)}{dx}\right) \qquad (78)$$

Equation (73) leads that Cathode side electron injection efficiency γ_n depends on hole diffusion constant Dp. The thermal coefficient of Dp is negative (Dp is degraded by higher temperature). In result higher γ_n can be obtained by higher temperature, especially with large k.

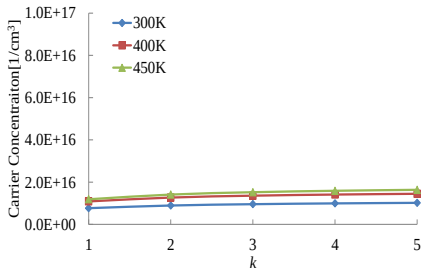
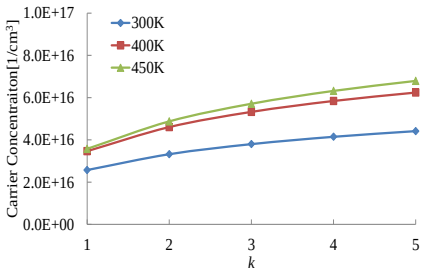
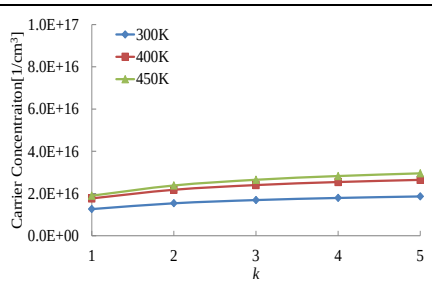
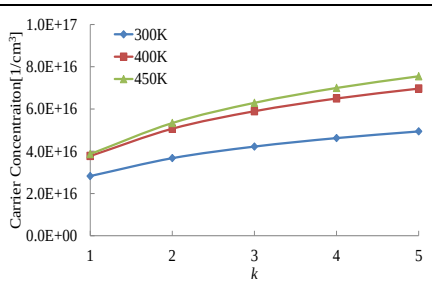
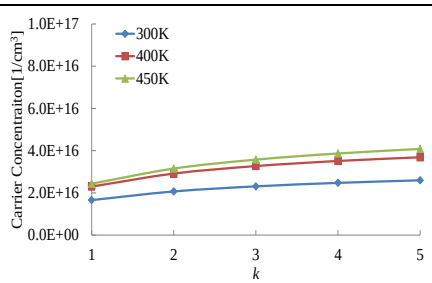
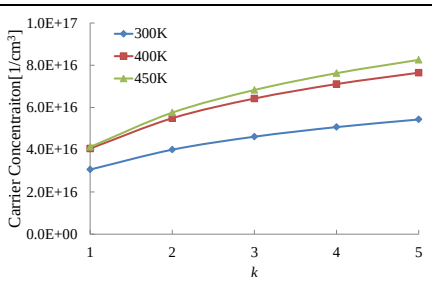
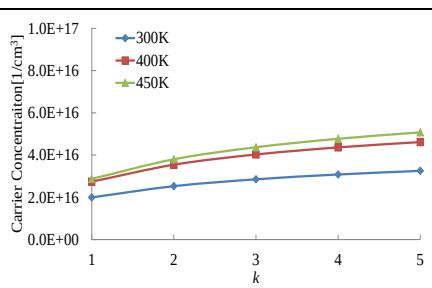
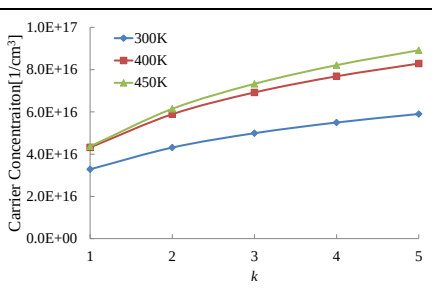
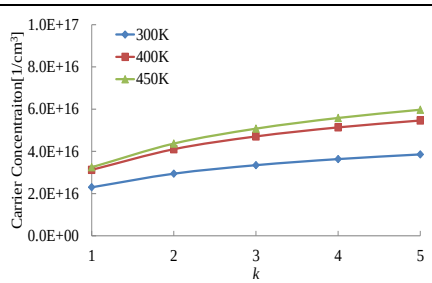
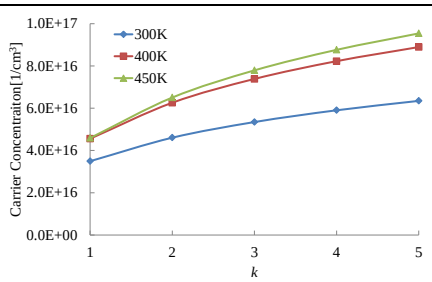
W [um]		*W* [um]	
2		12	
4		14	
6		16	
8		18	
10		20	

Figure 82. Relationships between carrier concentraion and scaling factor *k*. higher temperature makes higher injection efficiency especially with large *k*. The electron injection efficiency is assumed as 0.75.

6.3 Wafer Thickness Optimization

Scaled devices show higher breakdown voltages as shown in Figure 83. In this calculation, as previous section, the thickness from Anode to trench bottom was set to 120um for all devices. The reason for higher breakdown voltage is larger curvature of equipotential line as shown in Figure 84. Narrow trench-trench spacing and shallower trench improves potential distribution such that the electric field is relaxed around trench bottom.

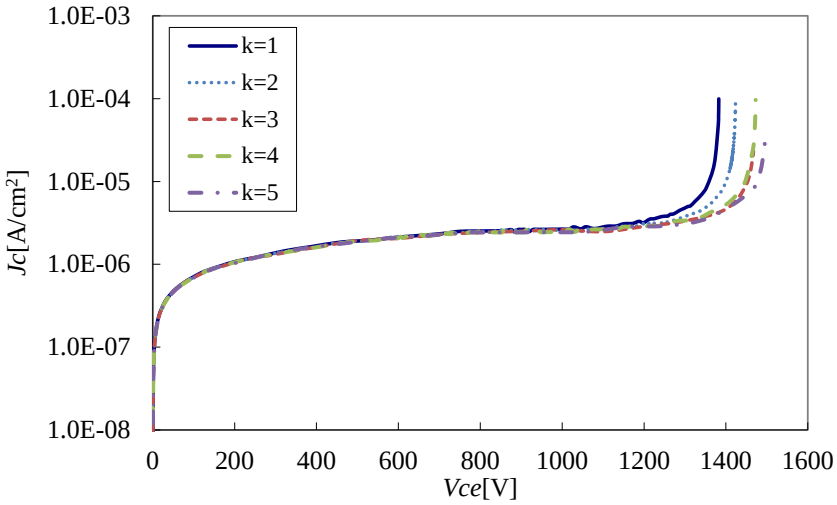


Figure 83. Breakdown characteristics for scaled devices.

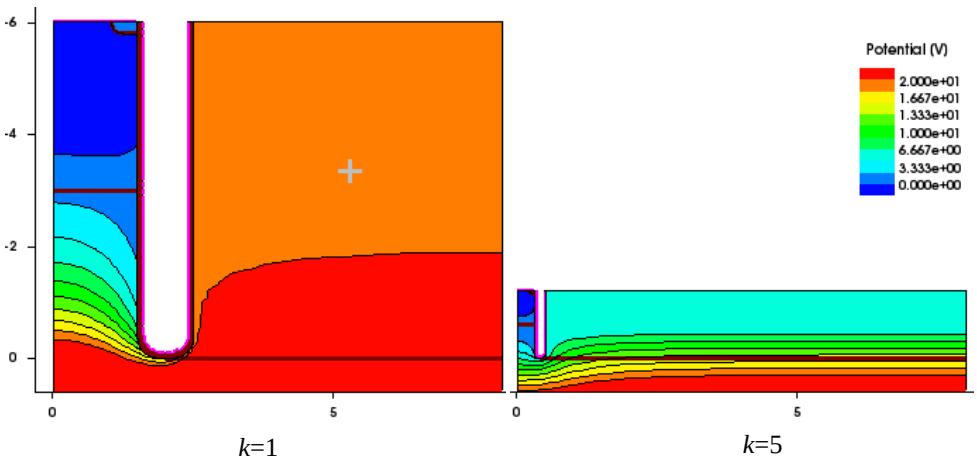


Figure 84. Potential distribution comparison between original device (k=1) and scaled device (k=5) at breakdown.

By this improvement, the wafer thickness should be reduced for scaled devices. It leads to reduce on-state voltage drop. Further scaled devices should have diode-like junction structure. It also contributes to improve Diode characteristics of RC (Reverse Conductive)-IGBT [57].

6.4 Latest Silicon Process Technology

In this dissertation, the scaling principle toward high productivity and high performance was found out. The principle predicts that shrinking mesa width is mandatory to apply shallower trench.

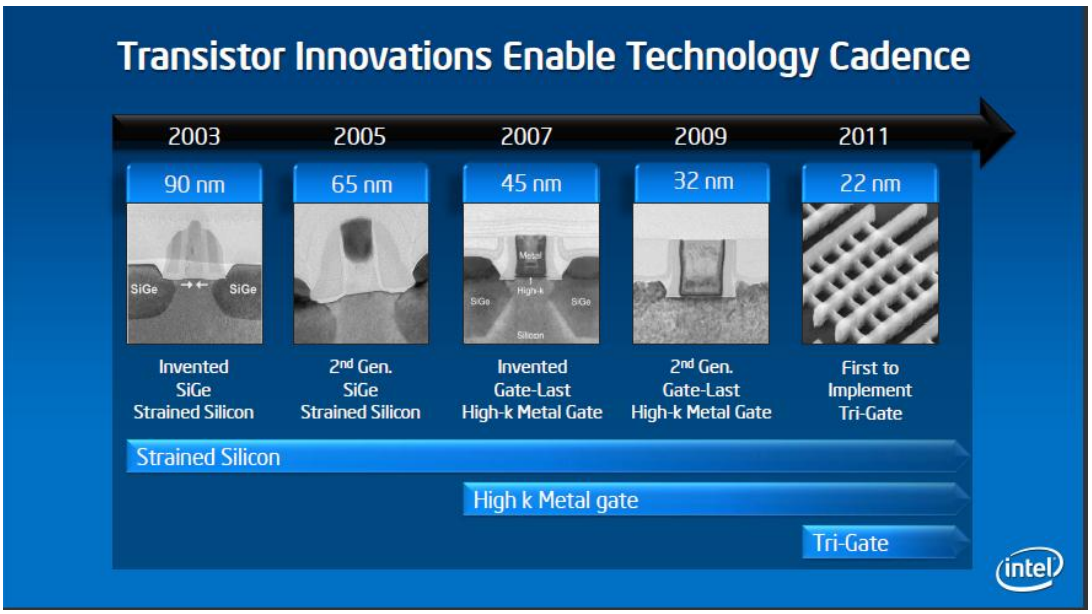


Figure 85. Transistor innovations in “More Moore” field [52].

In 2012, the latest transistor cell structure in CMOS world is FinFET. Intel just starts mass production of FinFET, named “Tri-Gate”, first of the world. The cell structure is three dimensional. The current flows from front to back in Figure 86. The minimum width of the Silicon pillar “Fin” is 22nm. According to the Dr. Nakagawa’s theoretical prediction for IGBT performance limit reviewed in section 5.2, the proposed design has 40nm of mesa width. Therefore, the ultimate performance IGBT design can be realistic in terms of the dimension.

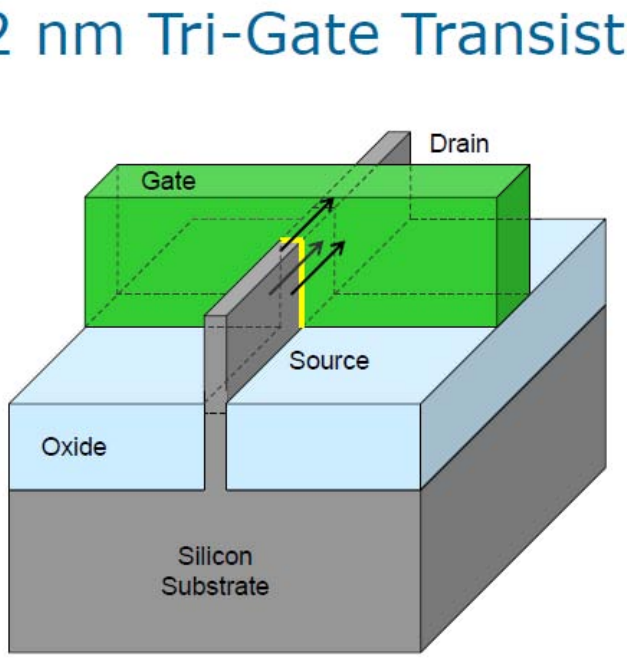


Figure 86. Latest transistor cell in 2012 [52]. Three dimensional structure, called "Tri-Gate", is used to prevent off-state leakage current, keeping enough on-state current level.

One issue which would prevent IGBT's scale down is current density around Cathode contact. At Cathode contact, the metal needs to contact to both N-Emitter and P-Base. Planar contact and trench contact are used as illustrated in the left side of Figure 87. There are two issues to be considered. First, the contact area between metal and Silicon becomes so limited. It causes high contact resistance between them and increases on-state voltage drop. Second, electro migration can be occurred in the narrow width metal layer with high current density. It can cause reliability problem.

One idea to solve the issues is independently designing mesa width and contact area as illustrated in the right side of Figure 87. According to the proposed principle, P-Base and contact layer don't need to be shrank, where mesa width must be decreased. Similar idea was proposed by Mr. Sumitomo in ISPSD 2012 [56].

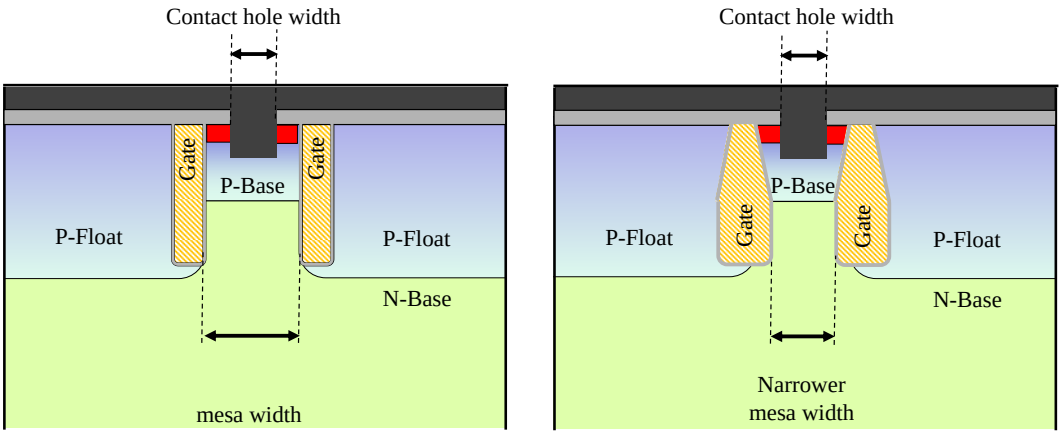


Figure 87. A structure to keep lower contact resistance and avoid electro migration (right side). Mesa width limitation is exist in conventional cell design (left side).

6.5 Packaging

One of the restrictions for IGBT operations is temperature limit. Joule heating by carrier conduction rises chip temperature. Once the temperature exceeds a limit, carriers are generated due to higher intrinsic carrier density than N-Base doping concentration. It is called thermal breakdown. Even with lower temperature than thermal limit, many kinds of degradations can be occurred. So the heat has to exhaust to ambient via package and heat sink, effectively.

One movement toward effective heat spreading is double sided cooling as illustrated in Figure 88. For extra high voltage applications, such as power plants and electrical trains, double sided cooling package has been used as called “press pack”. However the package is not used in general industrial equipment or home appliances because it requires expensive parts and very tough structure. Recently some companies proposed double sided cooling packages as extension from conventional package. And they are already produced for HEV (Hybrid Electric Vehicle).

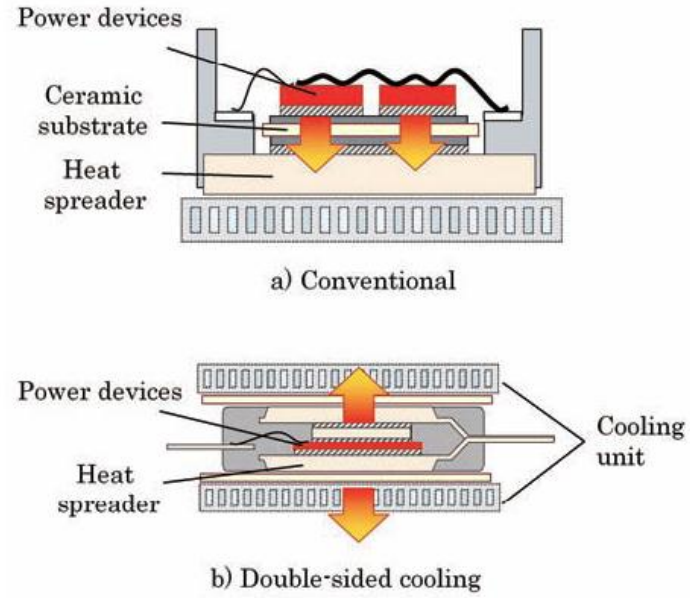


Fig. 3 Cross sectional view of a conventional power module and a double sided power module

Figure 88. Double sided cooling pakage [58].

6.6 Integration

In latest IGBT products, vertical device is major than lateral device due to its handling larger current per chip. Vertical device can integrate only a few components on a chip such as current sensing cell and temperature detector diode, where lateral device is embedded onto large scale integrated circuit as called Power IC. In currently produced IGBT modules, some functions such as gate drive, over current protection, and over temperature protection, are implemented by additional IC chips installed in the modules as illustrated in Figure 89. However, shorter distance between IGBT and IC is preferable to decrease parasitic elements, prevent malfunction by noise and save the footprint. Especially, noise should be taken care for highly scaled IGBT which has higher *gm* as simulated in previous section. An oscillation example is shown in Figure 90. The waveform shows that less than 0.5V oscillation for gate voltage can cause collector current oscillation.

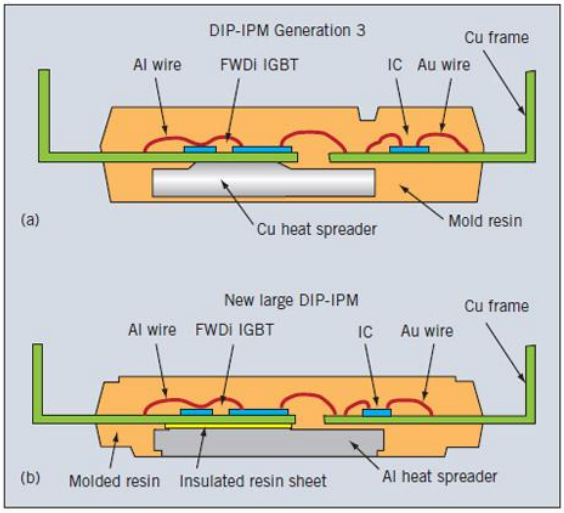


Fig. 1. Cross-sections of the a) previous Generation 3 DIP-IPM and b) the new Generation 4 DIP-IPM.

Figure 89. Cross sectional view of IPM (Intelligent Power Module) [1]. IC chip is installed separatelly.

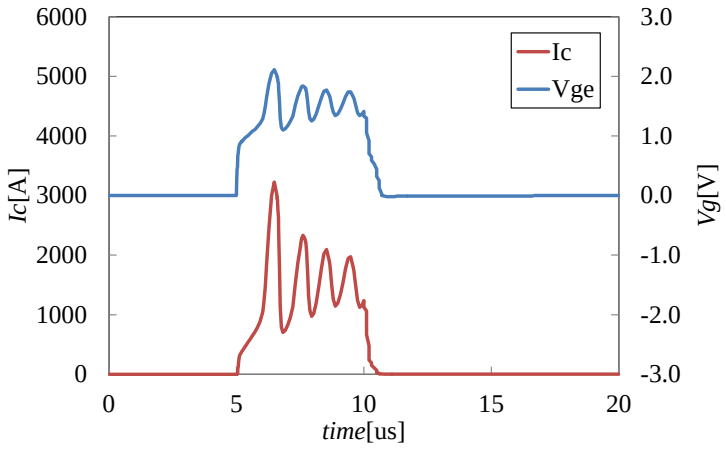


Figure 90. Oscillation waveform during short circuit for scaled device of k=5. Applied gate voltage=1.5V. Collector current oscillation is caused by the gate voltage.

One solution is proposed as illustrated in Figure 91. In this idea, firstly a lamination film is formed covering IGBT chip. Then contact holes are formed by laser drilling. Finally metal layer is formed by electro-plating. After the technology established, some IC chips can be embedded on IGBT chip. Wire bonding will be used to connect IC chips and IGBT chips.

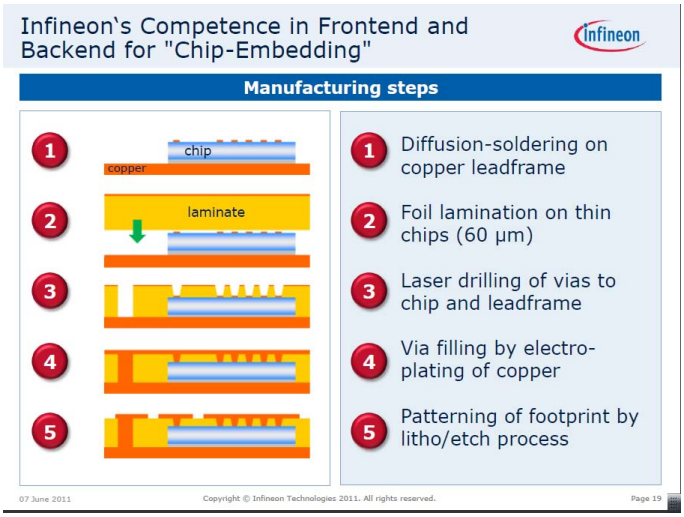


Figure 91. One approach for integration [59].

Another solution can be introduced from TSV (Through Silicon Via) technology. TSV technology is under developing for three dimensional LSI stack integration. Connection lines are formed inside Silicon vertically and connected to another LSI chip as illustrated in Figure 92. To form TSV, firstly via holes are formed by RIE (Reactive Ion Etching), then oxide layers are formed the surfaces of the via holes, finally the via holes are filled by a metal. TSV technology has advantages to suppress parasitic inductance than wire bonding method.

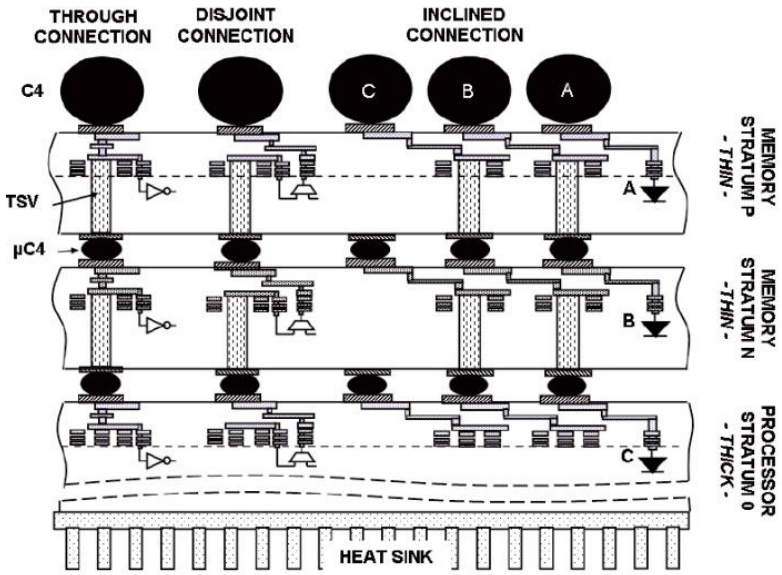


Figure 92. TSV (Through Silicon Via) technology [60].

6.7 Summary: Scaled device advantages and issues to be solved

As described above, proposed scaling principle gives great potential for further performance improvement to Silicon IGBT. On the other hand, several issues to be considered are alive. The advantages and issues are summarized in Table 11 and Table 12.

Table 11. Advantage of scaled device.

Device Performance	
On state voltage drop	Improved. Power loss is reduced. More improved in high temperature than room temperature.
Gate charge	Decreased as 1/*k*. The power consumption of gate drive is decreased. The capacity of gate drive circuit can be smaller.
Manufacturability	
Gate etching	Improved. Etching time can be reduced and the uniformity should be improved for shallower trench.
Gate oxidation	Improved. Oxidation time can be reduced by thinner oxide.
P-Base formation	Improved. Diffusion time can be reduced by shallower depth. Process controllability should be improved because final profile can be close to as-implantation profile.
N-Emitter formation	Improved. Diffusion time can be reduced by shallower depth. Process controllability should be improved because final profile can be close to as-implantation profile.
Backside processing	Improved. The warpage of the wafers can be reduced by shallower trench.

Table 12. Issues to be solved for scaled device.

Device Performance	
On state voltage drop	Low contact resistance techniques are required between Cathode electrode and P-Base/N-Emitter because contact current density becomes higher.
Malfunction	Higher stability for Gate-Emitter voltage is required to suppress oscillation and malfunction. The potential variation of Cathode electrode should be reduced.
Reliability	Electro-migration must be considered for Cathode electrode due to higher current density. Reliability of thinner gate oxide must be checked under severe conditions such as breakdown and short-circuit.
Manufacturability	
Wafer	300-450mm diameter FZ (Floating Zone) wafer must be developed.
Gate oxide	High-k material should be applied for highly scaled design to prevent tunneling current. The process uniformity applied for trench gate structure is unknown.

7 Conclusion

IGBT is widely used in middle to larger capacity power electronics system by higher rated voltage capability than MOSFET, and easier gate drive than Thyristor. The market size is about 2.5 billion dollars annually, and forecasted to expand about 10% by a year. Performance improvements for the whole systems and IGBT are continuously required. This dissertation targets two topics that obstruct to the improvements.

First, the issue about the limitation of existing compact models was discussed. In typical usage for three phase inverter circuit, six IGBTs and diodes are used to convert DC to three phase AC power. Compact models are used for such system simulation for performance improvement or failure analysis. It enables to simulate many cycle of switching with short calculation time. With existing compact model, as far as the models are used within the predetermined validity confirmed operation range of the models, the circuit

simulators effectively show the sufficiently accurate results. Once the condition exceeds the validity confirmed range, such as high temperature condition, the model requires re-fitting of the parameters so as to extend the validity range.

Second, the issue about poor process compatibility between IGBT and CMOS device was discussed. “More Moore” field semiconductor technology based on high resolution lithographic techniques enhances significant performance and mass-productivity improvements in digital integrated circuits by Moore’s Law as a scaling by a factor of 0.7 every 2 years. On the other hand, IGBTs introduce rather deeper trench structure to obtain lower on-state voltage drop and turn-off loss. The technology trend continues for more than 10 years and miniaturization has not been believed to contribute IGBT performance improvement. In result, currently process compatibility between CMOS and IGBT is limited. IGBT mass production in CMOS factory is difficult.

For the first issue, a device structure based compact model for advanced trench gate IGBTs was proposed for the first time. The compact model has superior characteristics so that the model doesn’t need fitting parameters and parameter extractions, and can adapt for extreme conditions such as under very low or high temperatures. The model should have large impact to be used for system analysis under wide range temperature condition.

For the second issue, a scaling principle for IGBT toward shallower structure and smaller thermal budget was also proposed for the first time by extension of the first topic. The scaling principle shows a possibility of technology direction and roadmap for future IGBT. It predicts the device performance improvement with high volume productivity with alignment for CMOS wafer process. The principle should have large impact to be used for new IGBT development designed for CMOS compatible wafer process, and mass produced in CMOS manufacturing line.

The most important topics required to achieve higher efficiency power electronics system were discussed and the solutions were provided. This dissertation contributes to design the systems and IGBT chips by providing new compact model and new scaling principle.

8 List of Tables

9 List of Figures

10 References

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11 Research History

Publication

1. M. Tanaka and I. Omura, "Structure Oriented Compact Model for Advanced Trench IGBTs without Fitting Parameters for Extreme Condition: part I", *Microelectronics Reliability* 51, pp. 1933-1937, 2011.

International Conferences

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