

Novel 600 V Low Reverse Recovery Loss Vertical PiN Diode with Hole Pockets by Bosch Deep Trench

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Abstract— The performance of a novel diode with characteristic trench shape is predicted by TCAD simulation. A novel 600 V vertical PiN diode with hole pockets by the Bosch deep trench process is proposed for a better trade-off curve between reverse recovery loss and forward voltage. The reverse recovery loss is reduced to a half. In addition, the active chip size of the novel diode is reduced to two-thirds that of the conventional PiN diode in the same forward voltage. The novel diode structure is a strong candidate when the simple fabrication process under development is established.

Keywords— diode; vertical; trench; Bosch; hole; reverse recovery loss

I. Introduction: Requirement for novel vertical diode

Efficiency improvement and the prevalence of high efficiency power electronics apparatus are key factors for efficient energy usage in our more electric-oriented society [1]. For these key factors, reverse recovery loss reduction (fast reverse recovery) at certain forward voltage and low cost are required for diodes in the power electronics apparatus.

To meet these demands, diodes have made remarkable progress in recent decades and many technologies have been continuously studied to enable next-generation power electronics.

Silicon diodes are superior to wide-bandgap diodes in the aspect of low cost (mass production technology). On the other hand, it was believed that the physical properties of silicon make it difficult to reduce reverse recovery loss any lower. To overcome the limitations of this silicon device, many researchers have endeavored to reduce reverse recovery loss by novel diode structure with hole pockets or deep trench [2-12]. However, there is no simple and fast fabrication process for the diodes at present.

We previously proposed a lateral SOI PiN diode with hole pockets as a novel diode structure to revise recovery loss reduction [13, 14]. Thanks to the waveform oscillation suppression with hole pockets, the diode successfully reduces reverse recovery loss to a half by the short current path (see Fig. 1). On the other hand, the cost of the lateral diode is predicted to be high because the diode with the thin Si layer

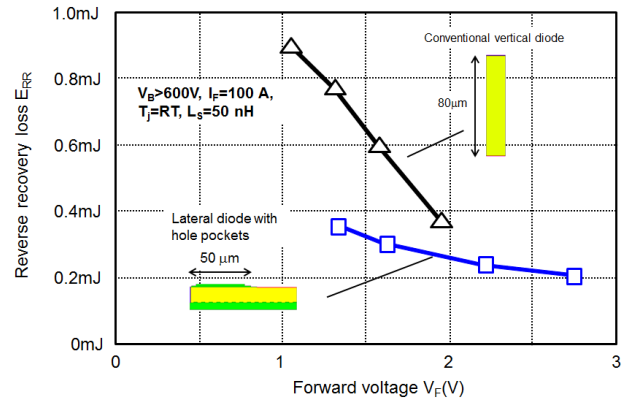


Fig. 1. Simulated trade-off curves between reverse recovery loss and forward voltage of lateral PiN diode and conventional diode without oscillation waveform.

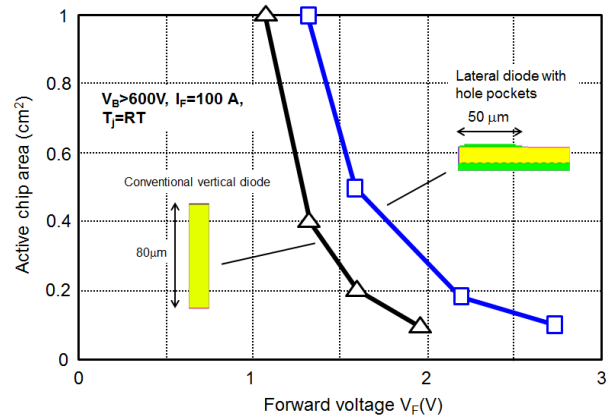


Fig. 2. Simulated trade-off curves between active chip size and forward voltage of lateral PiN diode and conventional diode without oscillation waveform.

requires a large chip size at a certain forward voltage (see Fig. 2). It is about three times larger than conventional vertical diodes. Therefore, a vertical PiN diode with hole pockets is proposed with novel technology of the Bosch deep trench process [15].

II. Hole pocket shape by Bosch deep trench process

The Bosch deep trench process enables high aspect ratio etching by the alternation of passivation and etching cycles. In each cycle a chemically inert polymer layer is uniformly deposited. This passivation layer prevents the sidewalls from being attacked in the subsequent etching step. By feeding high frequency plasma with etching gases, the passivation layer at the bottom of the trench is rapidly removed. After that, the silicon substrate is chemically etched.

In the passivation and etching cycles of the Bosch process, the characteristic convexo-concave shape called scallop is naturally shaped. The scallop shape can be controlled by the etching process. Basically, a larger scallop is formed by the larger amount of silicon etching per 1 cycle with longer etching time. And the etching speed is comparatively high. For example, the process time is around 4 minutes per 40 μm deep

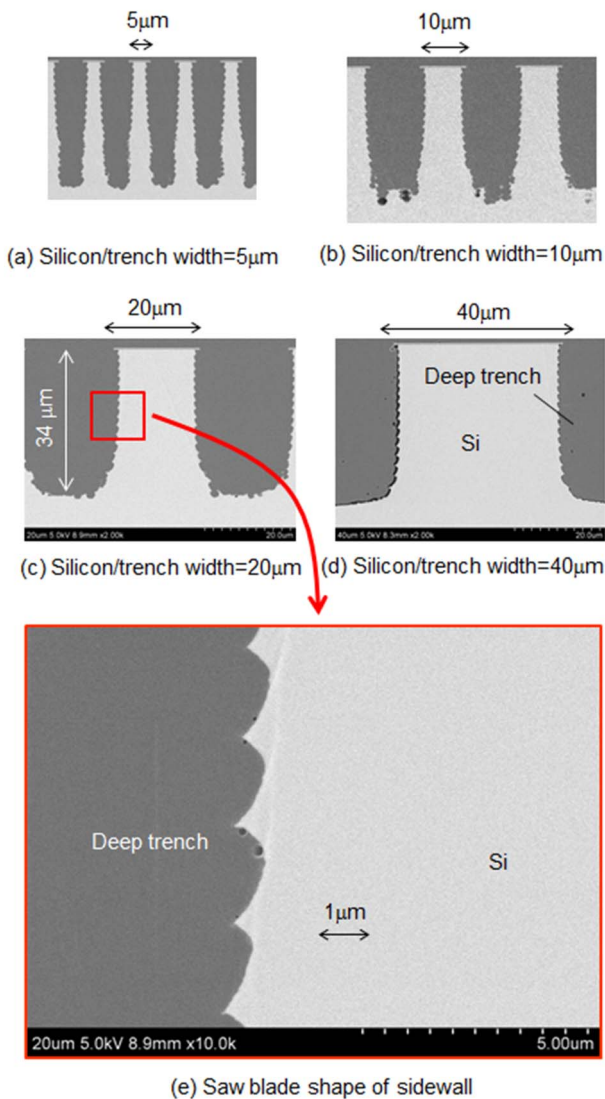


Fig. 3. Cross-section SEM image of as-etched silicon substrate with scallop by Bosch deep trench process.

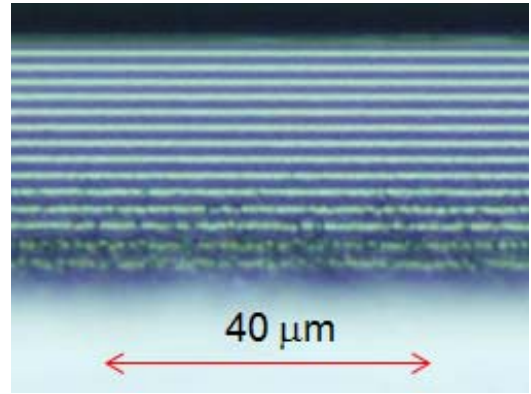


Fig. 4. Sidewall AFM image of as-etched silicon substrate with continuous scallop in the back by the Bosch process deep trench.

trench with a sufficiently larger scallop (see Fig. 3). Therefore, the Bosch process is utilized to create the hole pocket rapidly. We made deep trenches of 5 μm , 10 μm , 20 μm and 40 μm line and space (L/S) on a trial basis. The difference in the level of the scallops was successfully shaped for all L/S deep trenches. The difference was about 0.5 μm regardless of the L/S size and continues in the back (see Fig. 4). The crystal defects in the sidewall are not observed by TEM analysis. Another process for thickening the SiO_2 layer and electrode in the deep trench will be developed next.

III. Performance prediction of novel diode by TCAD simulation

The as-etched trench shape of the Bosch process was revealed by trial silicon etching in Chapter 2. The features of the trench shape are as follows (see Fig. 5).

- The bottom shape has roundness.
- The sidewall shape is a saw blade.
- The pitch of the saw blade shape is about 2 μm .
- The difference in the level of the saw blade shape is about 0.5 μm .

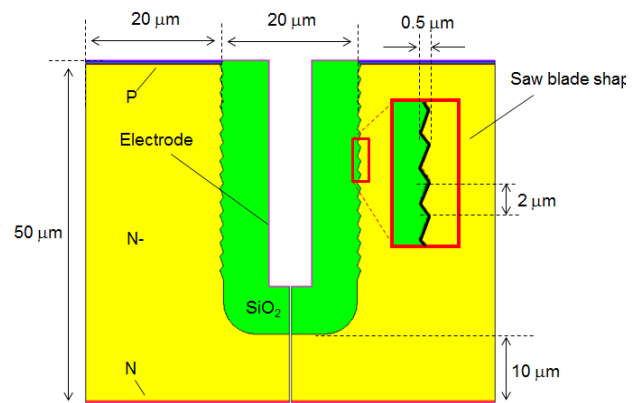


Fig. 5. Simulated novel diode structure with hole pockets.

The performance of the novel diode with the characteristic trench shape is predicted by TCAD simulation. The novel diode has a higher doping concentration of the N- layer. The

trench and the higher doping concentration equalize the electric field to maintain high blocking voltage in the off state and eventually the requisite thinner N-(base) layer thickness. The simulation results indicate a better trade-off curve of reverse recovery loss and chip size. Thanks to the waveform oscillation suppression with hole pockets, the diode with the thin N-base layer successfully reduces the reverse recovery loss to a half (see Fig. 6). Furthermore, the active chip size of the novel diode is reduced to two-thirds that of the conventional PiN diode at the certain forward voltage (see Fig. 7).

The surge voltage with noise is dramatically suppressed by the novel structure compared with the waveform of conventional punch-through structure and the simple deep trench diode without hole pockets (see Fig. 8). After reverse recovery, the stored carrier is swept out from the N-base layer. In this reverse recovery process, when the stored carrier is swept out rapidly, the surge voltage and noise are generated intensely [16, 17]. The stored carrier of the novel diode successfully remained for a long time after reverse recovery because the hole pockets lose hole drift velocity (see Fig. 9 and Fig. 10).

Conventional and proposed applicable diode structures for the PiN diode are non punch-through, punch-through, superjunction, and lateral PiN diode with hole pockets [18] (see Fig. 11). In the three subjects of the reverse recovery loss and active chip size at a certain forward voltage, and surge voltage with noise during reverse recovery, no diode structure satisfies the three subjects. The novel vertical PiN diode structure with hole pockets is a strong candidate for when the simple fabrication process is established.

The diode structure and fabrication process can be applied to all bipolar devices such as PiN diode and IGBT.

iv. Conclusion

The performance of the novel diode with the characteristic trench shape is predicted by TCAD simulation. A novel 600 V vertical PiN diode with hole pockets by the Bosch deep trench process was proposed for a better trade-off curve between reverse recovery loss and forward voltage. The reverse recovery loss is reduced to a half. In addition, the active chip size of the novel diode is reduced to two-thirds that of the conventional PiN diode. The novel diode structure is a strong candidate for when the simple fabrication process under development is established. The diode structure and fabrication process can be applied to all bipolar devices such as PiN diode and IGBT.

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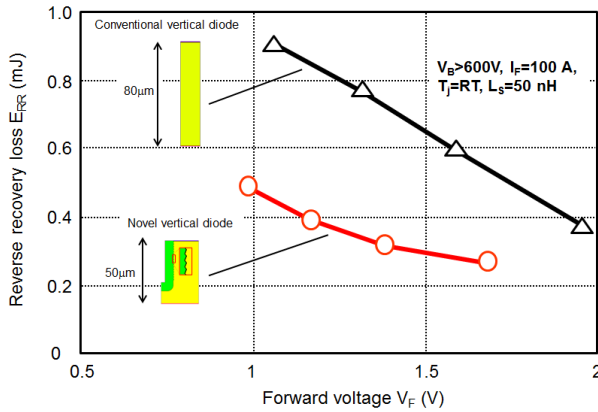


Fig. 6. Simulated trade-off curves between reverse recovery loss and forward voltage of novel vertical PiN diode and conventional diode without oscillation waveform.

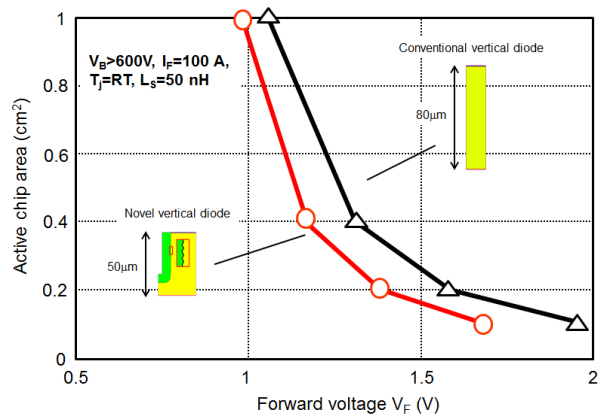


Fig. 7. Simulated trade-off curves between active chip size and forward voltage of novel vertical PiN diode and conventional diode without oscillation waveform.

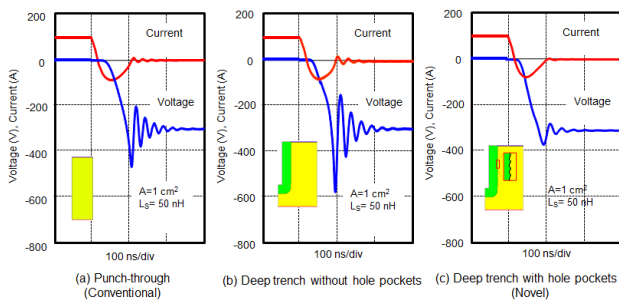


Fig. 8. Simulated reverse recovery waveform during reverse recovery (The thickness of all structures is 50 µm).

References

- [1] H. Ohashi, "Power devices now and future, strategy of Japan - Role of power electronics for a low carbon society," Proc. of ISPSD, pp. 9-12, 2012.
- [2] R. Plikat, D. Silber, and W. Wondrak, "Very high voltage integration' in SOI based on a new floating channel technology," Proc. of IEEE International SOI Conference, pp. 59-60, 1998.
- [3] I. Omura, and A. Nakagawa, "Silicon on Insulator semiconductor device with increased withstand voltage," United States Patent, 6049109, 2000.
- [4] H. Kapels, R. Plikat, and D. Silber, "Dielectric charge traps: a new structure element for power devices," Proc. of ISPSD, pp. 205-208, 2000.
- [5] X. Luo, B. Zhang, and Z. Li, "A novel E-SIMOX SOI high voltage device structure element for power devices," Proc. ICCAS 2005, 2005.
- [6] I. Omura, and A. Nakagawa, Japanese patent, No.3950105, 2007.
- [7] I. Omura, and A. Nakagawa, Japanese patent, No.3959125, 2007.
- [8] X. Luo, B. Zhang, Z. Li, Y. Guo, X. Tang, and Y. Liu, "A novel 700 V SOI LDMOS with double-sided trench," IEEE Electron Dev Lett, pp. 422-424, 2007.
- [9] X. Luo, B. Zhang, and Z. Li, "New high-voltage (>1200 V) MOSFET with the charge trenches on partial SOI," IEEE Trans. on ED, Vol. 55, No. 7, pp. 1756-1761, 2008.
- [10] S. Shiraki, Y. Ashida, S. Takahashi, and N. Tokura, "Analysis of Transient Characteristics of Lateral IGBTs and Diodes on Silicon-on-Insulator Substrates with Trenched Buried Oxide Structure," Proc. of ISPSD, pp. 261-264, 2010.
- [11] X.M. Yang, B. Zhang, and XR. Luo, "Double Enhance Dielectric Layer Electric Field High Voltage SOI LDMOS," Proc. of EDSSC, pp. 1-2, 2011.
- [12] K. Kobayashi, T. Nishiguchi, S. Katoh, T. Kawano, and Y. Kawaguchi, "100 V class multiple stepped oxide field plate trench MOSFET (MSO-FP-MOSFET) aimed to ultimate structure realization," Proc. of ISPSD, pp. 141-144, 2015.
- [13] M. Tsukuda, H. Imaki, and I. Omura, "Ultra-fast Lateral 600 V Silicon PiN Diode Superior to SiC-SBD," Proc. of ISPSD, pp. 31-34, 2014.
- [14] M. Tsukuda, H. Imaki, and I. Omura, "Ultrafast lateral 600 V silicon SOI PiN diode with geometric traps for preventing waveform oscillation," Solid-State Electronics, Vol. 104, pp. 61-69, 2015.
- [15] A. Baba, N. Uryu, and S. Sumi, "Fabrication of pn junction at the wall of deep trench for near-infrared sensor," Digest of Papers MNC2011, 26P-7-135, 2011.
- [16] M. Tsukuda, I. Omura, Y. Sakiyama, M. Yamaguchi, K. Matsushita, and T. Ogura, "Critical IGBT design regarding EMI and switching losses," Proc. of ISPSD, pp. 185-188, 2008.
- [17] M. Tsukuda, Y. Sakiyama, H. Ninomiya, and M. Yamaguchi, "Dynamic punch-through design of high-voltage diode for suppression of waveform oscillation and switching loss," Proc. of ISPSD, pp. 128-131, 2009.
- [18] T. Fujihira, and Y. Miyasaka, "Simulated superior performances of semiconductor superjunction devices," Proc. of ISPSD, pp. 423-426, 1998.

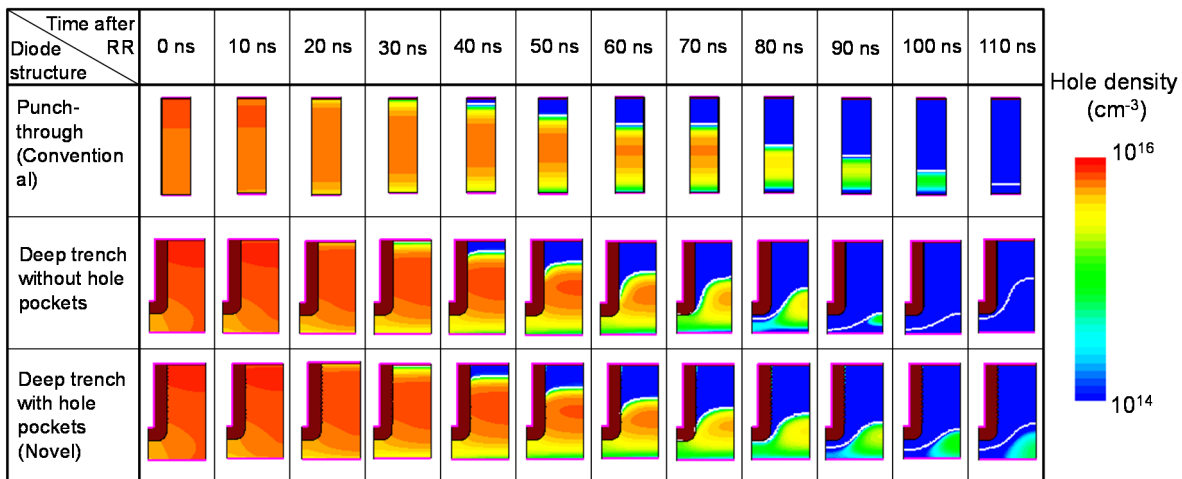


Fig. 9. Hole density during reverse recovery (The thickness of all structures is 50 μm).

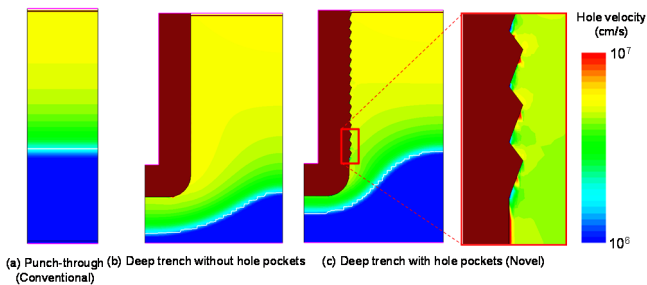


Fig. 10. Hole drift velocity during reverse recovery.

Structure of vertical diode	Non punch-through	Punch-through	Superjunction	Lateral and hole pockets	Deep trench with hole pockets (Novel)
Structure					
Reverse recovery loss	☹ Large	😊 Small	😊 Small	😊 Small	😊 Small
Active chip size	😊 Small	😊 Small	😊 Small	☹ Large	😊 Small
Surge voltage with noise	😊 Small	☹ Large	☹ Large	😊 Small	😊 Small

Fig. 11. Conventional and applicable structures for high voltage diode with merit and drawback.