Structure Oriented Compact Model for Advanced Trench IGBTs without Fitting Parameters for Extreme Condition: part I

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Abstract

A device structure based compact model for advanced trench gate IGBTs is proposed. The model is formulated only with device structure parameters so that no fitting parameters are required. The model is applicable to extreme conditions such as under very low or high temperatures. The validity of the model formulation is confirmed with two-dimensional TCAD simulation for voltage range of 1.2kV and 3.3kV IGBTs, and for temperature range of 300K and 450K. In this paper conduction mode formulation is proposed which has the potential to be used for system level failure analysis.

Keywords: IGBT, compact model, fitting parameters, high temperature

1. Introduction

IGBT compact models, such as Hefner model [1], have been widely used in power electronics system and circuit design as the device has expanded the application from small appliances to EV/HEV and tractions etc.[2][3]. The compact models enable to simulate large scale IGBT inverters and systems for many cycle of switching, where TCAD simulation cannot cover.

Most of the IGBT compact models have been formulated based on the combination of physics based simplified analytical equations, equivalent circuits and behavior models with a number of fitting parameters. As far as the models are used within the predetermined validity confirmed operation range of the models, the circuit simulators effectively show the sufficiently accurate results. Once the condition exceeds the validity confirmed range, such as high temperature condition, the model requires re-fitting of the parameters so as to extend the validity range.

A novel formulation of IGBT compact model proposed in this paper eliminates the fitting parameters from the model equations and only uses the device structure parameters as the model parameters. This concept enables the new model to be used in extreme condition such as very low or high temperature and expands the compact model function from circuit optimization to circuit – device coupled optimization since the model can applicable for wide range of device structure thanks to eliminating fitting parameters. In result, for example, the model can be also applied to analyze current imbalance in a chip due to the lack of process uniformities.

The proposed model is designed to cover the advanced IGBT structures with the injection-enhancement structure with trench gate structure on

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the Cathode side [4] and low injection structure on the Anode side [5], which are called the thin wafer IGBTs or the field stop (FS) IGBTs with the improved tradeoff between on-state voltage drop and turn-off loss.

In this paper, we show the modeling approach and verification results. We compare calculation results between the model and two-dimentional TCAD simulation. The result shows that the model can represent latest improvement of IGBTs accurately. It would be able to apply for system level failure analysis with complicated control sequences and severe temperature condition.

2. Structure Oriented Model Formulation

2.1. N-base Carrier Distribution

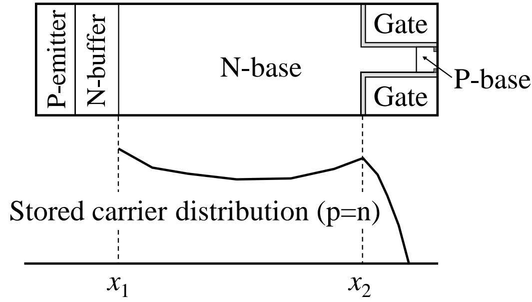

Fig. 1. Cross sectional view of Trench gate IGBT

Fig.1 shows cross-sectional view of Trench gate IGBT. N-base carrier concentration $n(x)$ can be formulated with carrier lifetime τ and diffusion length L_A of high injection condition [6].

$$L_A^2 \frac{d^2 n(x)}{dx^2} = n(x) + \tau \frac{dn(x)}{dt} \tag{1}$$

For the steady state conditions, time dependent term is omitted and the solution can be formed as

$$n(x) = L_A \frac{-\frac{dn}{dx}(x_1)\cdot\cosh\left(\frac{x_2 - x}{L_A}\right) + \frac{dn}{dx}(x_2)\cdot\cosh\left(\frac{x - x_1}{L_A}\right)}{\sinh\left(\frac{x_2 - x_1}{L_A}\right)}$$

(2)

where x_1 and x_2 are positions of anode edge and cathode edge of N-base region as shown in Fig. 1. Eq.2 means that N-base carrier distribution is decided by the differentials of the carrier distribution at both edges.

Following differential equation of carrier density can be also formulated in N-base region.

$$\mu_p J_n - \mu_n J_p = 2\mu_p \mu_n kT \frac{dn}{dx} \tag{3}$$

We can obtain the differentials of the carrier distribution at both edges of N-base.

$$\frac{dn}{dx}(x_1) = -\frac{J\left(\gamma_p - \frac{\mu_p}{\mu_p + \mu_n}\right)}{2\frac{\mu_p \mu_n}{\mu_p + \mu_n}kT} \tag{4}$$

$$\frac{dn}{dx}(x_2) = \frac{J\left(\gamma_n - \frac{\mu_n}{\mu_p + \mu_n}\right)}{2\frac{\mu_p \mu_n}{\mu_p + \mu_n}kT} \tag{5}$$

where γ_p and γ_n are hole injection efficiency at Anode side and electron injection efficiency at Cathode side, respectively.

$$\gamma_p = \frac{J_p(x_1)}{J} \tag{6}$$

$$\gamma_n = \frac{J_n(x_2)}{J} \tag{7}$$

The voltage drop in the N-base can be calculated based on the above stored carrier concentration.

$$V_{N-base} = -\frac{(\mu_n - \mu_p)\cdot kT}{(\mu_n + \mu_p)\cdot q}\int_{x=x_1}^{x_2} \frac{1}{n}\frac{dn}{dx}dx + \frac{J}{q(\mu_n + \mu_p)}\int_{x=x_1}^{x_2} \frac{1}{n}dx$$

(8)

2.2. Hole Injection from P-emitter

The low injection efficiency Anode structure with thin P-emitter layer and thin N-buffer layer is modeled for the advanced IGBTs. Fig. 2 shows schematic figure of the Anode structure and carrier distributions. N_A, L_p, N_D and L_n are P-emitter concentration, thickness, N-buffer concentration and

thickness, respectively. p_p, p_1, p_1', n_1 and n_p are internal variables as shown in Fig.2. In this model, charge neutrality inside the P-emitter and N-buffer are considered for model accuracy under high current density conditions.

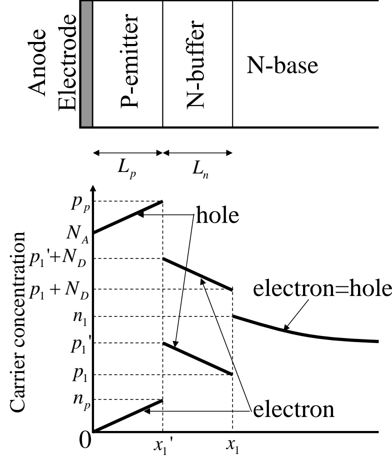

Fig. 2. Carrier distribution in P-emitter and N-buffer

The current densities J_n and J_p at N-base edge can be calculated by

$$J_n(x_1) = qD_n \frac{n_p}{L_p} \tag{9}$$

$$J_p(x_1) = qD_p \frac{p_1' - p_1}{L_n} \tag{10}$$

where D_p and D_n are diffusion coefficients for hole and electron, respectively. They can be calculated by carreir lifetimes.

Following boundary conditions can be obtained by p-n power continuity across the junctions.

$$(p_1 + N_D)p_1 = n_1^2 \tag{11}$$

$$p_p n_p = (N_A + n_p)n_p = (p_1' + N_D)p_1' \tag{12}$$

We can modify Eq. 9-12 with process parameters as following:

$$J_p(x_1) = qD_p \frac{1}{2L_n}\left(\sqrt{N_D^2 + 4(N_A + n_p)n_p} - \sqrt{N_D^2 + 4n_1^2}\right) \tag{13}$$

where

$$n_p = \frac{L_p}{q \cdot D_n} J_n(x_1) \tag{14}$$

This formulation can be also applied to low injection type NPT-IGBT by omitting N-buffer layer.

2.3. Electron Injection from Trench Gate Structure

The proposed model for electron injection from trench gate structure is simple, very accurate and stable for wide range of structure parameters. The carrier concentration in the mesa region is solved considering electron current along the accumulation layer in the trench interface as a function of position. It dramatically improves the accuracy. Fig.3 shows current elements under the P-base region. *W* and *S* are half of cell pitch and half of mesa width, respectively.

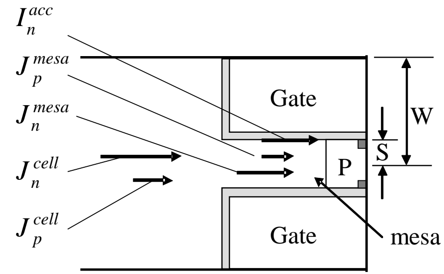

Fig. 3. Current elements in Trench structure

$$W \cdot J_p^{cell} = S \cdot J_p^{mesa} \tag{15}$$

$$W \cdot J_n^{cell} = I_n^{acc} + S \cdot J_n^{mesa} \tag{16}$$

Eq. 15 and 16 can be combined with using the conductance of accumulation layer, σ_{acc} , and the conductance of mesa region $\sigma_{mesa}(n)$ as following,

$$J_n^{mesa} = \frac{\sigma_{mesa}(n)}{\sigma_{acc} + \sigma_{mesa}(n)} \frac{W}{S} J_n^{cell} \tag{17}$$

σ_{acc} can be calculated by the electron mobility and the accumulated carrier density of MOS-gate. The electron mobility is degraded by normal electric field and can be calculated by [7].

Following differential equation of carrier density can be formulated in the mesa region.

$$\mu_p J_n^{mesa} - \mu_n J_p^{mesa} = 2\mu_p \mu_n kT \frac{dn}{dx} \tag{18}$$

In result we obtain the Cathode side carreir distribution equation with process parameters as

$$\left(\frac{\mu_p}{\mu_n} \frac{\sigma_{mesa}(n)}{\sigma_{acc} + \sigma_{mesa}(n)} + 1 \right) \gamma_n - 1 = \frac{2qD_p}{J} \frac{S}{W} \frac{dn}{dx} \tag{19}$$

The voltage drop in mesa region can be calculated by

$$V_{mesa} = \frac{J\gamma_n}{-q\mu_n} \frac{W}{S} \int_{x_2}^{x_3} \frac{1}{n(x)} \frac{\sigma_{mesa}(n)}{\sigma_{acc} + \sigma_{mesa}(n)} dx \tag{20}$$

2.4. Channel Conductance of MOSFET Region

The voltage drop of the channel can be calculated by power of electron current via MOS gate, which is calculated by (16), and. channel conductance, which can be calculated by surface potential along the channel.

We assume strong inversion condition for the channel region. Surface potential $\phi_S(x)$ can be calculated by

$$\phi_s(x) = 2\phi_P(x) + V_{DS}(x) \tag{21}$$

Where $\phi_P(x)$ is the difference of intrinsic Fermi potential and P-base Fermi potential. $V_{DS}(x)$ is the potential drop from source side. The charge concentration of gate oxide can be calculated by

$$Q_G(x) = C_{ox}(V_{GE} - \phi_s(x)) \tag{22}$$

Where C_{ox} is the capacitance per unit area of gate oxide, and V_{GE} is gate-emitter voltage. The charge concentration of channel region can be calculated by

$$Q_C(x) = -(Q_G(x) + Q_A(x)) = -C_{ox}(V_{GE} - \phi_s(x)) - Q_A(x)$$
(23)

Where $Q_A(x)$ is acceptor concentration of P-base region. We can modify it to

$$Q_C(x) = -C_{ox}(V_{GE} - (2\phi_P(x) + V_{DS}(x))) + \sqrt{2\varepsilon_{si}\varepsilon_0(2\phi_P(x) + V_{DS}(x))qN_A(x)} \tag{24}$$

where $N_A(x)$ is acceptor concentration of P-base region. Finally the channel conductance can be calculated by

$$\sigma_{channel}(x) = \mu_{channel}(x) \cdot Q_C(x) \tag{25}$$

$\mu_{channel}(x)$ is the electron mobility in the channel which is degraded by normal electric field and can be calculated by [7].

2.5. Built-in Potential

The built-in potential is the difference between quasi-Fermi potential and electro static potential as shown in Fig. 4. For Anode side, it can be calculated by

$$V_{built-in}(x_1) = \frac{kT}{q} \log \frac{n(x_1)}{n_i} \tag{26}$$

It can be calculated for Cathode side by

$$V_{built-in}(x_2) = \frac{kT}{q} \log \frac{n(x_2)}{n_i} \tag{27}$$

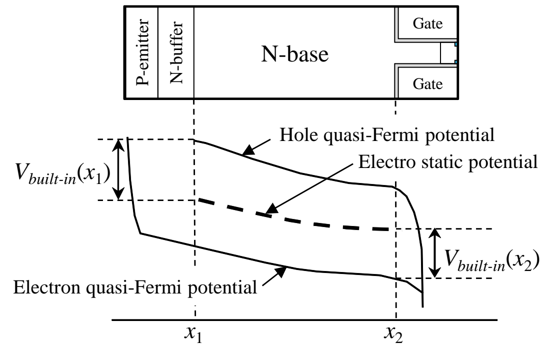

Fig. 4. Built-in potential

3. Model Validation for Variety of Structure and Temperature

The established model was verified by comparing with two-dimensional TCAD calculation results. We

used two types of IGBTs; 1.2kV thin wafer PT-IGBT and 3.3kV IEGT for model validation. Table 1 shows physical constants used for the calculations by the established model and TCAD. Temperature dependence is considered for all three constants [8][9]. Doping concentration dependence is also considered for carrier mobility and lifetime [10][11]. Electron mobility degradation by normal electric field is evaluated to calculate electron current through MOS channel and mesa region.

Table 1. Physical constants for 300K

Constants	For electron	For hole
Carrier mobility	$1417cm^2/Vs$	$470.5cm^2/Vs$
Carrier lifetime	10.0usec	3.0usec
Intrinsic carrier density	$1.18x10^{10}/cm^3$	

Table 2. Parameters using model verification

Parameters	1.2kV thin PT-IGBT	3.3kV IEGT
N-base concentration	$8x10^{13}/cm^3$	$2x10^{13}/cm^3$
N-base thickness	112um	342um
Half cell pitch: W	2.0um	8.0um
Half mesa width: S	1.5um	1.5um
P-base surface concentration	$2x10^{17}/cm^2$	$2x10^{17}/cm^2$
P-base thickness	3.0um	3.0um
Trench depth	6.0um	6.0um
Gate oxide thickness	0.1um	0.1um
P-emitter concentration	$1x10^{17}/cm^3$	$2x10^{17}/cm^3$
P-emitter thickness	1.0um	1.0um
N-buffer concentration	$9x10^{16}/cm^3$	$9x10^{16}/cm^3$
N-buffer thickness	1.0um	1.0um

Table 2 shows twelve parameters to represent these IGBTs by proposed model. Fig. 5 and 6 show calculated Ic-Vc characteristics of 1.2kV thin wafer PT-IGBT and 3.3kV IEGT, respectively. Fig. 7 and 8 shows on-state carrier distribution of 1.2kV thin wafer PT-IGBT and 3.3kV IEGT, respectively. They indicate the model can represent forward characteristic accurately under extreme temperature condition.

Fig. 9 shows Trench depth-Vce(sat) relationship for 3.3kV IEGT with 8.0um of half cell pitch. Fig. 10 shows cell pitch-Vce(sat) relationship for 3.3kV IEGT with 6.0um of trench depth. They indicate the model can predict device improvement accurately.

4. Conclusion

We proposed new compact model for Trench gate IGBT. The model is formulated by only physical parameters. The bipolar equation is formulated with injection efficiencies of anode and cathode side. Anode injection efficiency is formulated by doping concentration and junction depth of P-emitter and N-buffer. Cathode injection efficiency is formulated with trench gate structure dimensions and carrier mobility. Modeling should be easier because fitting parameters don't need to be adjusted. The model is validated by comparing with two-dimensional TCAD simulation results. The forward characteristics and the internal carrier distributions of 1.2kV and 3.3kV IGBT show good agreement with TCAD results with temperature range from 300K to 450K. The model should have large impact to be used for system level failure analysis under wide range temperature condition.

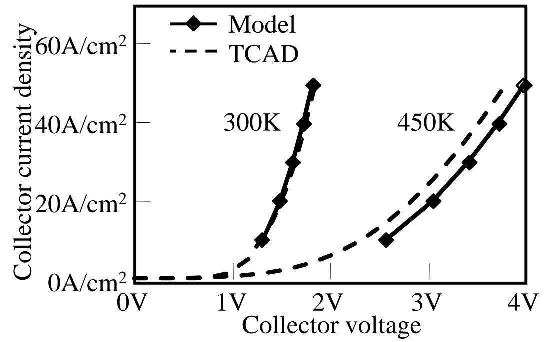

Fig. 5. Ic-Vc comparison between proposed model and TCAD for 1.2kV thin wafer PT-IGBT

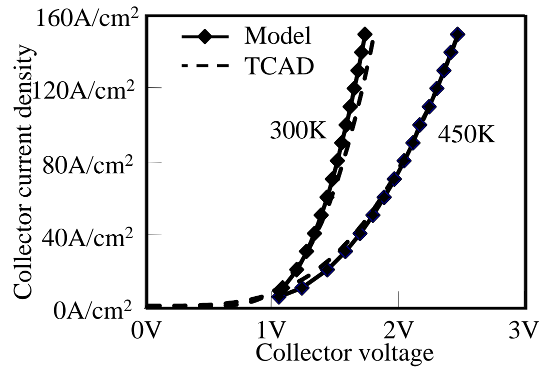

Fig. 6. Ic-Vc comparison between proposed model and TCAD for 3.3kV IEGT

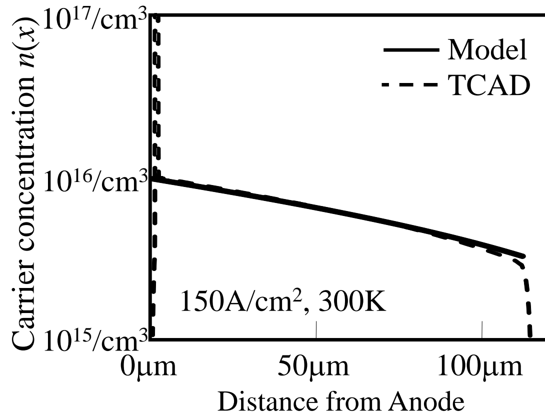

Fig. 7. N-base carrier distribution comparison between proposed model and TCAD for 1.2kV ThinPT-IGBT

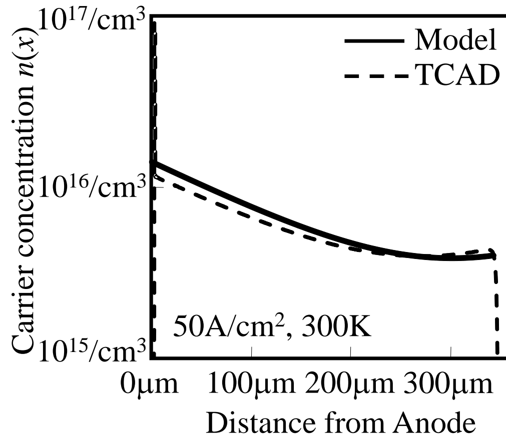

Fig. 8. N-base carrier distribution comparison between proposed model and TCAD for 3.3kV IEGT

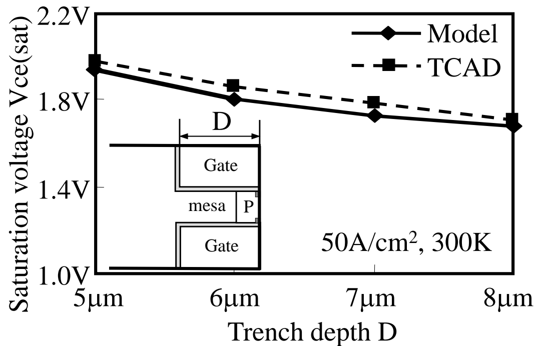

Fig. 9. Trench depth-Vce(sat) relationship comparison between proposed model and TCAD for 3.3kV IEGT

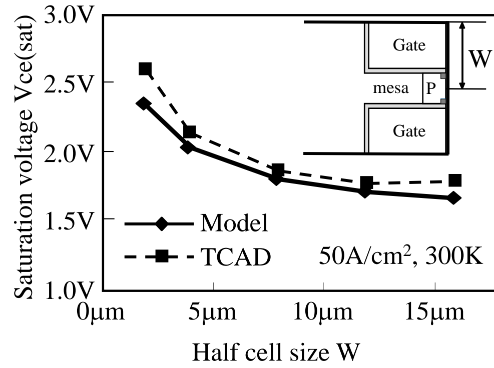

Fig. 10. Cell pitch-Vce(sat) relationship comparison between proposed model and TCAD for 3.3kV IEGT

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