

A New Evaluation Circuit with a Low-Voltage Inverter Intended for Capacitors Used in a High-Power Three-Phase Inverter

Kazunori Hasegawa

Department of Biological Functions and Engineering
Kyushu Institute of Technology
Kitakyushu, Fukuoka, Japan

Ichiro Omura

Department of Electrical Engineering and Electronics
Kyushu Institute of Technology
Kitakyushu, Fukuoka, Japan

Shin-ichi Nishizawa

National Institute of Advanced Industrial Science and Technology
Tsukuba, Ibaraki, Japan
Department of Biological Functions and Engineering
Kyushu Institute of Technology
Kitakyushu, Fukuoka, Japan

Abstract— DC-link capacitors in power electronic converters are a major constraint on improvement of power density as well as reliability. Evaluation of the dc-link capacitors in terms of power loss, ageing, and failure rate will play an important role in design stages of the next-generation power converters. This paper proposes a new evaluation circuit for dc-link capacitors used in a high-power three-phase inverter, which is intended for testing power loss, failure rate, ageing, and so on. The evaluation circuit produces a practical ripple current waveform and a dc bias voltage into a capacitor under test, in which the ripple current is equivalent to that generated by the three-phase inverter on the dc link. The evaluation circuit employs a full-scale current-rating and downscaled voltage-rating inverter for producing the ripple current, so that the power rating of the evaluation circuit is much smaller than that of a full-scale current rating and full-scale voltage rating inverter.

Keywords—DC-link capacitors, high-power density, reliability, three-phase inverters.

I. INTRODUCTION

Power density of power electronic converters are continuously becoming higher and higher as their market size is getting larger and larger, which is accompanied by smaller power loss, lower volume, and lower weight in the converter. The market size growth also requires improvement of reliability not only in power semiconductor devices but also in passive components [1]. Hence, the next-generation power converters will be designed with managing both power density and reliability.

DC-link capacitors in power electronic converters are a major constraint on improvement of power density [2]. They tend to include a design margin of size or capacitance due to power loss. Thus, the minimum design margin of the capacitors is desirable, which should be considered in design

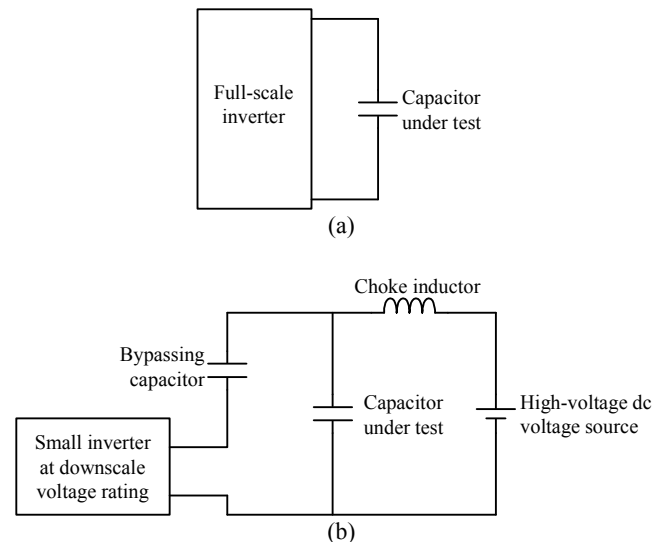


Fig. 1 Basic concepts of an evaluation circuit for a high-power capacitor. (a) Using full-scale inverter. (b) Using full-scale current-rating and downscale voltage-rating inverter.

stages of the converters. Furthermore, a lifetime of the capacitors is usually shorter than that of semiconductor devices or magnetic devices, which would degrade reliability of the power converters. Evaluation of the capacitors in terms of power loss, ageing, and failure rate will play an important role in design stages of the next-generation power converters [3-12]. However, characteristics of the capacitors are usually evaluated by a single sinusoidal current such as 120 Hz, 1 kHz, and so on [7, 8, 12-14]. There are some kinds of “ripple current tester” instruments that provide a sinusoidal ripple current as well as a dc-bias voltage into the capacitor [14]. Actual current flowing out of the converter into the capacitor

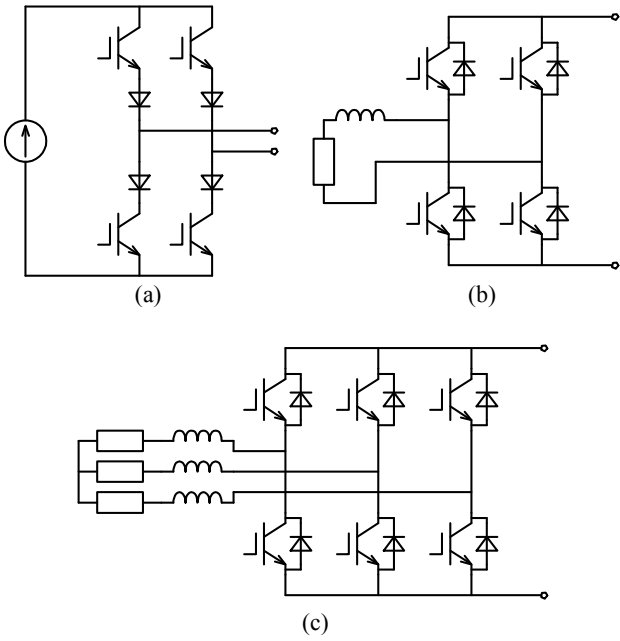


Fig. 2 Possible configurations of the small inverter. (a) Single-phase CSI. (b) Single-phase VSI. (c) Three-phase VSI

contains multiple frequency components [15], so that characteristics of the capacitors cannot be exactly estimated. Although the so-called fast Fourier transform (FFT) can extract the multiple frequency components from the actual current, a power loss of the capacitor cannot be estimated using the multiple frequency components because power loss in general has a nonlinear characteristic. In addition, the dc bias voltage across the capacitors affects power loss and ageing [1, 5, 11, 12]. Thus, existing power converters often employ more capacitors than necessary.

It is important to develop an evaluation circuit for component testing of capacitors, which will be utilized in design stages or in tests before shipment of the converters. Note that the system should behave as an existing inverter in terms of the dc bias voltage and ripple current waveform of the capacitor.

This paper proposes a new evaluation circuit with a low-voltage inverter intended for dc-link capacitors used in a high-power three-phase inverter, which presents a practical ripple current waveform that is equivalent to that of the existing inverter. The circuit will be utilized for evaluating the capacitor by electric or thermal measurement such as the followings:

1. Electrical measurement of ESR and capacitance [6, 9].
2. Power loss measurement by electrical or calorimetric measurement [10, 16].
3. Accelerated aging [12].

Although this paper does not pay attention to measuring characteristics of the capacitor under test, it just focuses on circuit configurations and design of the evaluation circuit. In addition, this paper discusses power rating of the evaluation circuit.

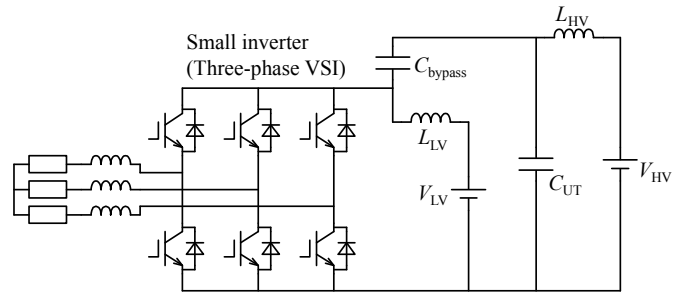


Fig. 3 Proposed evaluation circuit using a three-phase VSI.

II. BASIC CONCEPT

A. Evaluation circuit for capacitors

The most effective way to evaluate dc-link capacitors is measuring their characteristics with an existing converter in operation. For example, references [4, 6, 9] discuss real-time monitoring for capacitor condition using equivalent series resistance (ESR) and capacitance. Therefore, a basic idea of the evaluation circuit would utilize an existing power-rating inverter. Fig. 1 (a) shows the basic idea of the evaluation circuit, in which a full-scale current-rating and full-scale voltage-rating inverter is connected to a capacitor under test, CUT. The inverter provides a practical ripple current and dc bias voltage for the capacitor.

There are some special circuits that evaluate the capacitors [8, 12]. Reference [8] presents a simple circuit to evaluate an electrolytic capacitor, which consists of a combination of a dc-voltage supply providing a dc bias voltage, and a line-frequency transformer injecting a sinusoidal ripple current. The circuit is useful for estimating the capacitance and equivalent series resistance (ESR). Reference [12] presents a test circuit for accelerated aging of metalized film capacitors, which consists of a combination of a resonant inverter producing a sinusoidal ripple current and a dc voltage supply providing a dc bias voltage. Although both the two combinations contribute to reducing the overall power rating of the evaluation circuit, the ripple current waveform is different from the practical one generated by the inverter.

Fig. 1 (b) shows the basic concept of the proposed evaluation circuit that employs a small inverter, the capacitor under test, a bypassing capacitor, a choke inductor, and a high-voltage dc supply. The concept is similar to the circuits proposed in [8] and [12] in terms of the combination of a ripple current source and a dc voltage supply, whereas it presents a practical ripple current waveform, i.e., the same current waveform as that generated by the inverter. Current rating of the small inverter is full-scale, while voltage rating of that is downscale. The high-voltage dc supply keeps the capacitor voltage a desired dc bias voltage. The bypassing capacitor is used for circulating the ripple current generated by the inverter through the capacitor under test. The choke inductor is used for blocking the ripple current, through which only dc current flows. Hence, the proposed circuit operates as a full-scale voltage-rating and full-scale current-rating inverter from the standpoint of the dc bias voltage and ripple current. Thus,

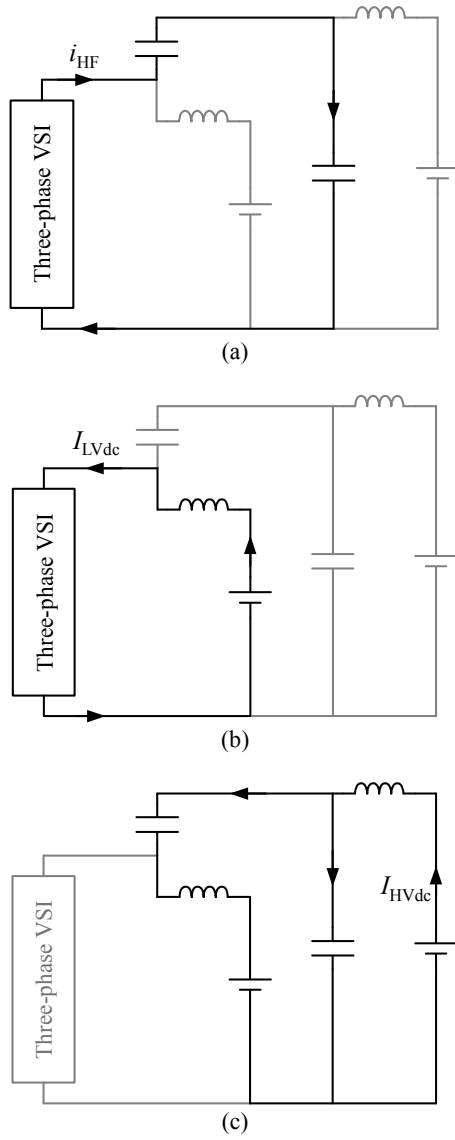


Fig. 4 Current paths of the proposed circuit. (a) AC current flowing out of the VSI. (b) DC current flowing out of the low-voltage dc supply. (c) DC current flowing out of the high-voltage dc supply.

power-rating of the small inverter is much smaller than that of the full-scale inverter.

B. Possible configurations of the small inverter

Candidates for the small inverter can be classified into the followings:

1. Single-phase current-source inverter (CSI) (Fig. 2 (a))
2. Single-phase voltage-source inverter (VSI) (Fig. 2 (b))
3. Three-phase voltage-source inverter (VSI) (Fig. 2 (c))

The evaluation circuit using the single-phase CSI behaves as a full-scale three-phase or single-phase inverter if it can provide the same ripple current waveform as the current generated by the full-scale single-phase or three-phase inverter, respectively. However, not only pulse width but also amplitude should be modulated to synthesize the ripple current

waveform. In practice, therefore, quite complex control would be required for the CSI.

The single-phase VSI can be used for an evaluation circuit for the full-scale single-phase inverter. DC-link terminal of the VSI is connected to the bypassing capacitor and capacitor under test, so that the voltage across the bypassing capacitor is slightly lower than that across the capacitor under test by the dc-link voltage. Since instantaneous power in a single-phase circuit fluctuates at double the fundamental frequency, a ripple amplitude of the dc-link voltage in the single-phase VSI tends to be large. It will be a constraint on the voltage rating of the VSI because the dc-link voltage should be larger than the ripple amplitude.

The three-phase VSI is a candidate for an evaluation circuit for the full-scale three-phase inverter. DC-link terminal of the three-phase VSI is connected to the bypassing capacitor and capacitor under test like the single-phase VSI. On the other hand, a ripple amplitude of the dc-link voltage in the three-phase VSI is much lower than that in the single-phase VSI because the instantaneous power of the three-phase inverter is constant in a steady state [17].

This paper deals with the three-phase VSI as the small inverter because of the following reasons:

1. The three-phase inverter is widely used.
 2. Lower dc-link voltage allows smaller power rating.
 3. General-purpose inverters are available as the small inverter.
 4. No special control is required to the ripple current
- Note that the three-phase VSI has only to control its output voltage, i.e., open-loop PWM control is applicable.

III. PROPOSED CIRCUIT CONFIGURATION

A. Circuit Configuration

Fig. 3 shows the proposed evaluation circuit consisting of the three-phase VSI, a low-voltage dc supply V_{LV} with a choke inductor L_{LV} , the high-voltage dc supply V_{HV} with a choke inductor L_{HV} , the bypassing capacitor C_{bypass} , and the capacitor under test, C_{UT} . The low-voltage dc supply is used for driving the three-phase VSI. The high-voltage dc supply provides a dc bias voltage to C_{UT} .

Fig. 4 shows current paths flowing out of the two dc voltage supplies and the three-phase VSI. The high-frequency ripple current generated by the VSI, i_{HF} circulates through C_{bypass} and C_{UT} because it does not flow into the two choke inductors L_{LV} and L_{HV} as shown in Fig. 4(a). The low-voltage dc supply V_{LV} provides a dc current I_{LVdc} to the VSI through L_{LV} as shown in Fig. 4(b). The high-voltage dc supply charges C_{UT} and C_{bypass} to their operating voltages, and then supplies a small amount of leakage dc current flowing into the capacitors, I_{HVdc} as shown in Fig. 4(c). Hence, the power rating of the high-voltage dc supply is quite small.

B. Power rating of the small inverter

Since the current rating of the small inverter is the same as that of the full-scale inverter, the relation between the power

Table I Rating and circuit parameters of the proposed circuit used in experiment.

Power rating of the system	P	6400 VA
Power rating of the inverter	P_{inv}	640 VA
AC current rating	I_O	5 A
AC voltage rating	V_O	73 V
Low-voltage dc source	V_{LV}	120 V
High-voltage dc source	V_{HV}	1200 V
Load inductor	L_O	27 mH (100%)
Load resistor	R_O	80 m Ω (1%)
Switching frequency	f_{sw}	6.1 kHz
Output frequency	f_o	50 Hz
High-voltage choke inductor	L_{HV}	10 mH
Low-voltage choke inductor	L_{LV}	10 mH
Capacitor under test	C_{UT}	320 μ F
Unit capacitance constant of the capacitor under test [22]	H	36 ms
Bypassing capacitor	C_{bypass}	320 μ F
Damping resistor	R_{damp}	3.3 Ω

() is based on 640 VA, 73 V, 5 A, and 50 Hz

Table II Rating and circuit parameters of the full-scale inverter used in simulation.

Power rating	P	6400 VA
AC current rating	I_O	5 A
AC voltage rating	V_O	730 V
DC link voltage	V_{dc}	1.2 kV
Switching frequency	f_{sw}	6.1 kHz
Output frequency	f_o	50 Hz
Load inductor	L_O	270 mH (100%)
Load resistor	R_O	780 m Ω (1%)

() is based on 6400 VA, 730 V, 5A, and 50 Hz

rating of the small inverter, P_{small} and that of the full-scale inverter, P_{FS} is given by

$$\frac{P_{small}}{P_{FS}} = \frac{V_{Dlink-S}}{V_{Dlink-FS}} = \frac{V_{LV}}{V_{HV}}, \quad (1)$$

where $V_{Dlink-FS}$ and $V_{Dlink-S}$ are dc-link voltages of the full-scale inverter and the small inverter, respectively, and P_{FS} is the power rating of the full-scale inverter. As the dc-link voltage of the small inverter, $V_{Dlink-S}$ contains ripple voltages of C_{UT} and C_{bypass} , the dc mean of $V_{Dlink-S}$ should be designed to be more than the ripple voltages. The low-voltage dc supply should provide the dc mean voltage according to the ripple voltages. Since the instantaneous power of the three-phase inverter is constant, dc-link voltage of the three-phase inverter contains only switching ripple component. Thus, one can pay attention to the switching frequency, the current rating, and capacitance of C_{UT} . In practice, however, attention should also be paid to imbalance of the three-phase load of the inverter because it would cause ripple voltage on the dc link. This paper introduces a condition that the dc-link voltage of the small inverter is 1/20 to 1/10 of that of the full-scale inverter.

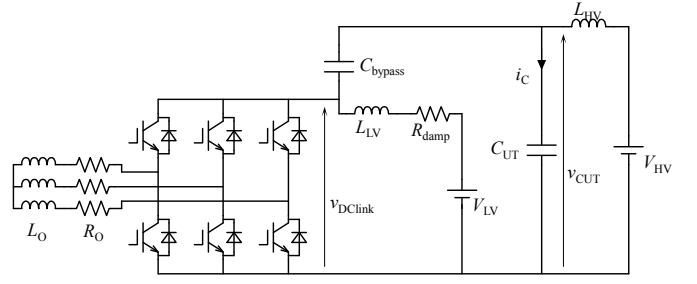


Fig. 5 Experimental circuit configurations of the proposed circuit.

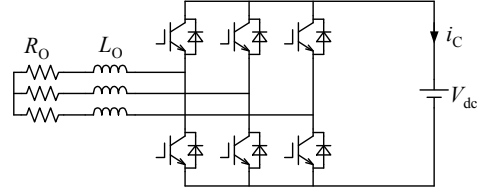


Fig. 6 Full-scale three-phase inverter used for simulation.

C. Design of Choke Inductors

Reactances of the two choke inductors should be much larger than that of capacitors C_{UT} and C_{bypass} .

$$\omega L_{choke} \gg \frac{1}{\omega C_{dc}}, \quad (2)$$

where $\omega = 2\pi f_{sw}$, f_{sw} is the switching frequency of the inverter, L_{choke} indicates a choke inductor of L_{HV} or L_{LV} , and C_{dc} stands for C_{UT} or C_{bypass} . The current rating of L_{choke} is determined by the leakage dc current of C_{dc} . Since volume of inductor is in proportion to 3/4th power to the maximum stored energy of $\frac{1}{2}LI^2$ [18], the volumes of the choke inductors are quite small.

D. Example of practical use

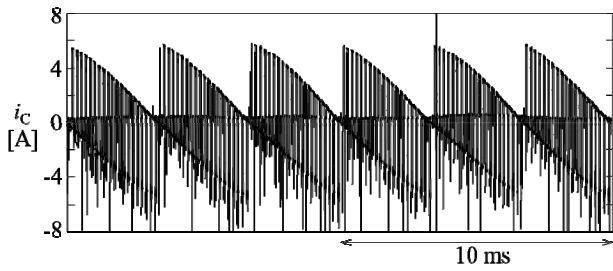
Low-voltage (200 or 400 V) general-purpose inverters are available to the small inverter, so that medium-voltage capacitors are suitable for the proposed circuit. The current rating of the general-purpose inverters are up to 1000 A [19, 20]. Thus, the proposed circuit using the general-purpose inverter can evaluate capacitors used in a high-power inverter with power rating up to 1-10 MVA.

IV. EXPERIMENT AND SIMULATION

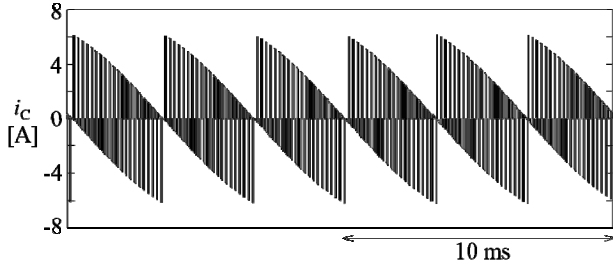
This section presents experimental results of the proposed circuit with comparing to the full-scale three-phase inverter by simulation, where a software package of the ‘‘PLECS’’ is carried out [21].

A. Circuit configurations

Fig. 5 illustrates experimental circuit configuration of the proposed evaluation circuit. Sinusoidal pulse-width modulation (SPWM) is applied to the inverter. Table I summarizes ratings and circuit parameters of the experiment. The damping resistor R_{damp} prevents an oscillation caused by the capacitors and the choke inductors. The power

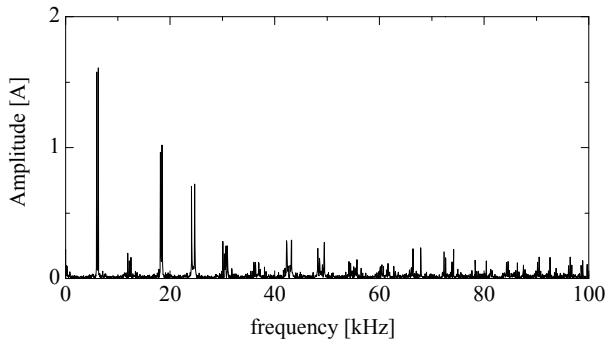


(a) Proposed circuit by experiment.

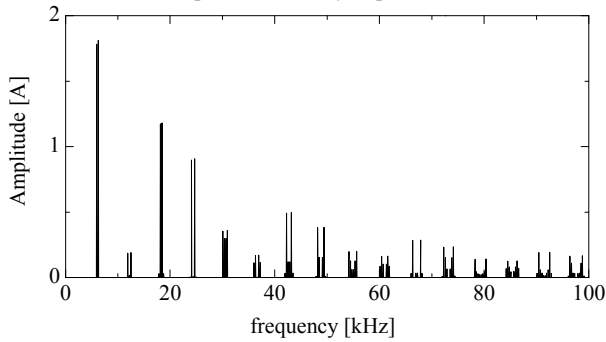


(b) Full-scale inverter by simulation.

Fig. 7 Current waveforms flowing into the capacitor under test.



(a) Proposed circuit by experiment.



(b) Full-scale inverter by simulation.

Fig. 8 FFT results of Current waveforms flowing into the capacitor under test.

consumption of the damping resistor is only 0.1% of the supplied power from the high-voltage dc supply. Note that the proposed circuit can also supply a ripple current in case the load power factor is changed although the low-voltage dc supply has to provide an amount of active power to the small inverter.

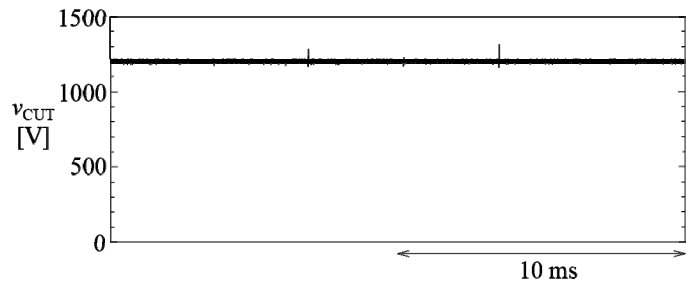


Fig. 9 Experimental waveform of the voltage across C_{UT} , v_{CUT} .

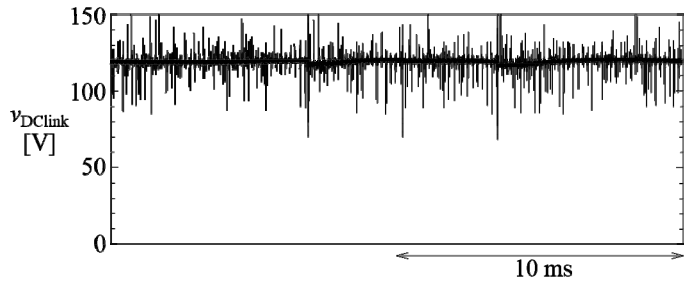


Fig. 10 Experimental waveform of the voltage across C_{UT} , v_{CUT} .

Fig. 6 shows the full-scale three-phase inverter for simulation, where a dc voltage source is connected instead of the capacitor under test on the dc link. Table II summarizes the ratings and circuit parameters of the full-scale inverter.

B. Results

Fig. 7 shows waveforms of the capacitor current i_C . The waveforms of the proposed circuit almost agree with that of the full-scale inverter. In addition, fig. 8 illustrates FFT results of the capacitor current, in which the FFT result of the proposed circuit almost agree with that of the full-scale inverter.

Fig. 8 shows the voltage across the capacitor under test, v_{CUT} in the proposed circuit. They stay at 1.2 kV that is the dc bias voltage applied by the high-voltage dc supply. Fig. 9 shows the dc-link voltages of the small inverter in the proposed circuit, v_{dlink} , which looks a constant dc current except for switching ripple components.

CONCLUSION

This paper has proposed a new evaluation circuit for dc-link capacitors used in a high-power three-phase inverter. The proposed circuit is characterized by combining a small three-phase inverter and a small voltage supply, where an existing low-voltage inverter would be applicable to the small inverter.

Experimental results obtained from a 1200-V 6.4-kVA prototype verifies that the evaluation circuit produces a practical ripple current waveform and a dc bias voltage into a capacitor under test, in which the ripple current is almost equivalent to that generated by the full-scale inverter. Moreover, the results confirms that the power rating of the evaluation circuit can be less than 1/10 of that of the full-scale inverter.

REFERENCES

- [1] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters—an overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569-3578, 2014.
- [2] J. W. Kolar, U. Drofenik, J. Biela, M. Heldwein, H. Ertl, T. Friedli, and S. Round, "PWM converter power density barriers," *IEE Japan Trans. Ind. Appl.*, vol. 128, no. 4, pp.468-480, 2008.
- [3] K. Harada, A. Katsuki, and M. Fujiwara, "Use of ESR for deterioration diagnosis of electrolytic capacitor," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 355-361, Oct. 1993.
- [4] P. Venet, F. Perisse, M. H. El-Husseini, and G. Rojat, "Realization of a smart electrolytic capacitor circuit," *IEEE Ind. Appl. Mag.*, vol. 8, no. 1, pp. 16–20, Jan./Feb. 2002.
- [5] O. Ondel, E. Boutleux, and P. Venet, "A decision system for electrolytic capacitors diagnosis," in *Proc. of IEEE Power Electronics Specialist Conference (PESC)*, pp. 4360-4364, 2004.
- [6] E. C. Aeloiza, J. H. Kim, P. Ruminot, and P. N. Enjeti, "A Real Time Method to Estimate Electrolytic Capacitor Condition in PWM Adjustable Speed Drives and Uninterruptible Power Supplies," *IEEE Power Electronics Specialists Conference (PESC)*, pp. 2867-2872, 2005.
- [7] A. M. R. Amaral, and A. J. M. Cardoso, "A Simple Offline Technique for Evaluating the Condition of Aluminum–Electrolytic–Capacitors," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3230-3237, Aug. 2009.
- [8] A. M. R. Amaral, and A. J. M. Cardoso, "Estimating aluminum electrolytic capacitors condition using a low frequency transformer together with a dc power supply," in *Proc. of IEEE ISIE*, pp. 815-820, 2010.
- [9] K. Abdennadher, P. Venet, G. Rojat, J. M. Retif, and C. Rosset, "A Real-Time Predictive-Maintenance System of Aluminum Electrolytic Capacitors Used in Uninterrupted Power Supplies," *IEEE Trans. Ind. Appl.* vol. 46, no. 4, pp. 1644-1652, Jul./Aug., 2010.
- [10] J. M. Miller, C. W. Ayers, L. E. Seiber, and D. B. Smith, "Calorimeter evaluation of inverter grade metalized film capacitor ESR," in *Proc. of IEEE ECCE*, pp. 2157-2163, 2012.
- [11] M. Makdessi, A. Sari, and P. Venet, "Metalized polymer film capacitors ageing law based on capacitance degradation," *ELSEVIER Microelectronics Reliability*, vol. 54, pp. 1823-1827, 2014.
- [12] M. Makdessi, A. Sari, P. Venet, P. Bevilacqua, and C. Joubert, "Accelerated Ageing of Metalized Film Capacitors Under High Ripple Currents Combined With a DC Voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2435-2444, May 2015.
- [13] NICHICON CORPORATION. "General Description of Aluminum Electrolytic Capacitors," [Online]. available: <http://www.nichicon.co.jp/english/products/pdf/aluminum.pdf>
- [14] RIPPLE CURRENT TESTER MODEL 11800/11801/11810, Chroma ATE Inc. 2014. [Online]. available: <http://www.chromaate.com/File/Download/42014>
- [15] B. P. McGrath and D. G. Holmes, "A general analytical method for calculating inverter DC-link current harmonics," *IEEE Trans. Ind. Appl.* vol. 45, no. 5, Sep./Oct. 2009
- [16] D. Christen, U. Badstuebner, J. Biela, and J.W. Kolar, "Calorimetric power loss measurement for highly efficient converters," in *Conf. Rec. of International Power Electronics Conference (IPEC)*, pp. 1438-1445, 2010.
- [17] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Trans. Ind. Appl.*, vol. IA-20, no. 3, pp. 625-630, 1984.
- [18] W. T. McLyman, *Transformer and inductor design handbook*. New York: Marcel Dekker, 1988.
- [19] *High Performance Vector Control Inverter FRENIC-VG Series*, Fuji Electric Co., Ltd., Tokyo, Japan, 2014. [Online]. available: <https://felib.fujielectric.co.jp/download/index.htm?site=global&lang=en>
- [20] *F700 Series Brochure*, Mitsubishi Electric Automation, Inc. 2011. [Online]. available: <https://us.mitsubishielectric.com/fa/en/support/technical-support/knowledge-base/getdocument/?docid=3E26SJWH3ZZR-38-1348>
- [21] [Online]. available: <http://www.plexim.com/plecs>
- [22] H. Fujita, S. Tominaga, and H. Akagi, "Analysis and design of a dc voltage-controlled static var compensator using quad-series voltage-source inverters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 4, pp. 970–977, 1996.