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Ultrafast lateral 600 V silicon SOI PiN diode with geometric traps for preventing waveform oscillation

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Abstract

An ultrafast lateral silicon PiN diode with traps is proposed using a silicon-on-insulator (SOI) substrate with traps. The proposed diode successfully suppresses waveform oscillation because the trapped hole suppresses electric field penetration and prevents the oscillation trigger known as “dynamic punch-through.” Because of the short current path caused by the oscillation prevention, the reverse recovery speed was higher and the reverse recovery loss was strongly reduced. The proposed trap structure and design method would contribute to performance improvement of all power semiconductor devices including IGBTs and power MOSFETs.

1. Introduction

Efficiency improvement and the prevalence of power electronics apparatus are key factors for efficient energy usage in our more electric-oriented society [1,2]. For these key factors, fast switching, low forward voltage drop, and low cost are required for power semiconductor devices, because fast switching and low forward voltage drop increase the saved energy, while low cost reduces the system cost of power electronics.

To meet these demands, power semiconductor devices have made remarkable progress in recent decades and many technologies have been continuously studied to enable next-generation power electronics. These technologies are divided into three major areas: “more silicon (breakthrough in silicon power technology),” “beyond silicon (heterogeneous integration technology),” and “more than silicon (wide-bandgap power technology)”.

Silicon devices are superior to wide-bandgap power devices in the aspect of low cost (mass production technology). On the other hand, it was believed that the physical properties of silicon make it difficult to make switching any faster. Therefore, many researchers have challenged the ultrafast reverse recovery and proposed a novel diode structure with a trap concept in silicon power technology [3–13].

2. Potential and problems for faster reverse recovery

The reverse recovery speed and forward voltage drop are the main characteristics of diode performance. The forward voltage drop of the Si-PiN diode is determined by the sum of the built-in potential at the PN junction and the voltage drop in the N-layer. Similarly, the forward voltage drop of the SiC Schottky barrier diode (SBD) is determined by the sum of the Schottky barrier height at the metal–Si junction and the voltage drop in thin N-layer. The forward voltage drop of the Si-PiN diode is almost the same as that of the SiC-SBD. However, the reverse recovery speed of the Si-PiN diode is extremely slow because it takes a long time for the electric field to sweep the hole out of the N-layer.

Faster reverse recovery (faster switching) has a large impact not only on diodes but also on switching devices including IGBTs. This is because the reverse recovery current due to stored carrier of diode pass through switching device during turn-on and increase current peak of the switching device. So the turn-on loss of the switching device is strongly reduced with a fast reverse recovery diode (Fig. 1) [14,15].

The authors calculated the reverse recovery speed by a bipolar device model and investigated the reverse recovery time of a state-of-the-art Si-PiN diode from a data sheet and TCAD simulation. The applied voltage is 300 V, current density is 250 A/cm², and stray inductance is 50 nH for TCAD simulation. It was found that there was a large potential for faster reverse recovery between the state-of-the-art commercialized diode and the theoretical limit (Fig. 2). The theoretical reverse recovery time limit is calculated with flat carrier distribution, so it's assumed that only drift current flows in the N- layer [16]. The potential reverse recovery speed was much higher than that of the state-of-the-art diode and was almost the same as the commercialized SiC-SBD [17]. Please note that the forward voltage drop (V_F) of electrode metal and bonding wires is not considered in this paper.

On the other hand, it was also revealed by the TCAD simulation that the fast reverse recovery of the Si-PiN diode having a thin N-layer induces a hard waveform oscillation during the reverse recovery time, as shown in Table 1. The waveform oscillation causes serious problems of conduction noise and emission noise. Because of the the noises induced by the oscillation, the Si-PiN diode has not achieved ultrafast reverse recovery until now.

The phenomenon of oscillation trigger has been clarified in previous work [18–21]. When the carrier injection of the diode is stopped, the stored carrier is swept out from both sides of the thin N-layer (Fig. 3). At the same time, the high electric field penetrates from both sides and finally reaches the other high electric field. This phenomenon is the trigger for the waveform oscillation known as “dynamic punch-through.” After the dynamic punch-through, the waveform is continuously oscillated by LC resonance with a stray inductance and a junction capacitance, because the hole as a resistance is completely swept out of the N-layer. Therefore, elimination of the dynamic punch-through is indispensable for the prevention of oscillation. The PiN diode having a thick N-layer is one of the typical methods to prevent the oscillation, because the hole remains throughout the reverse recovery and prevents the dynamic punch-through (Fig. 4). As a result, the waveform does not oscillate, although the reverse recovery speed becomes slower.

Previously proposed diodes for the oscillation suppression are roughly divided into two types; one type prompts reinjection of the carrier by the partial doping layer and the other prevents hard dynamic punch-through by an additional N layer in the N- layer [22–26]. However, these structures cannot achieve dramatic fast reverse recovery because the reinjection carrier or the additional N-layer slows reverse recovery.

3. Proposed ultrafast silicon PiN diode with traps

This section describes the proposed diode structure and the fabrication process. The proposed diode shows the strong oscillation suppression effect with the unique mechanism. In addition, the authors propose a simplified design and arrangement method for the traps. Because of the oscillation suppression effect, the ultrafast reverse recovery was achieved as noted in section 3.4.

3.1. Proposed diode structure and fabrication process

We propose a completely different diode, namely the lateral silicon-on-insulator (SOI) diode with traps, as shown in Fig. 5. It has convexo-concave-shaped traps with Si and oxide on top of the buried oxide. The average

thickness of the silicon and buried SiO₂ is 10 μm and 5 μm, respectively. The trap pitch and height are 5 μm and 0.5 μm, respectively.

The example of the fabrication process for convexo-concave-shaped traps had the following steps: local oxidation of Si (LOCOS) or oxidation after Si dry-etching, chemical mechanical polishing (CMP), and bonding. The fabrication process was similar to the conventional SOI structure. The fabrication process for the P emitter and anode electrode was adequately considered by a combination of boron diffusion and a deep reactive ion etching-like trench gate process. And about junction termination, dielectric separation technology like power IC can be applied for this proposed structure.

3.2. Oscillation suppression effect of the proposed diode

As shown in Fig. 6, the waveform oscillation was suppressed by the proposed diode, unlike other diodes. In the conventional vertical diode, the hole is completely swept out of the N- layer by the electric field during reverse recovery. Thus, the dynamic punch-through occurred and the waveform oscillated strongly. The dynamic phenomenon of the lateral SOI diode was almost the same as that of the vertical diode. The hole of the lateral SOI diode was also completely swept out of the N- layer by the electric field during the reverse recovery with impact ionization. Consequently, the dynamic punch-through occurred and the waveform oscillated. The case of the proposed diode is completely different with the hole remaining throughout the reverse recovery. Thus, dynamic punch-through was prevented and the waveform did not oscillate. In particular, the hole under the cathode remained for a long time.

The dynamic phenomena are explained by the point of the hole with electric field penetration (Fig. 7). The electric fields of the vertical diode penetrated from both sides; therefore dynamic punch-through occurred easily. At 80 ns, the electric field penetration reduced because of voltage lowering by the oscillation. For the lateral SOI diode, the early electric field penetration from the cathode was suppressed, but eventually the dynamic punch-through occurred. Unlike these diodes, the proposed diode suppressed the electric field penetration from the anode and also stopped the electric field penetration from the cathode; thus, the dynamic punch-through was prevented.

The advantage of the proposed diode is clearly indicated from the aspect of the Reverse Recovery Softness Factor (RRSF) [27] (also called “soft factor [21]). A higher value of RRSF means softer reverse recovery characteristics. The proposed diode indicates high soft reverse recovery characteristics on the wide current range compared with other typical diodes (Fig. 8).

3.3. Design and arrangement method for traps

The electric field of the vertical diode has a linear slope, corresponding to the doping concentration of the N-layer. At high blocking voltage, the electric field spreads all over the N-layer (Fig. 9(a)). Therefore, dynamic punch-through easily occurs with high voltage during reverse recovery. The lateral SOI diode has two electric field peaks at the borders of layers (Fig. 9(b)). The electric field spreads all over the N-layer, so that dynamic punch-through occurs. The proposed diode also had the two electric field peaks, but because of the trapped hole in the concave part of the Si, there was an electric field room under the cathode (Fig. 9(c)). Eventually, the dynamic punch-through of the proposed diode is most suppressed in these three diodes. For oscillation suppression, an electric field room with designed and arranged traps is required.

The trap design to maintain the blocking voltage was considered by the TCAD simulation. The trap design was complex because the pitch and height could be designed separately. Under this complex situation, we propose a simplified design method with the ratio of trap pitch to trap height. The breakdown voltage and electric field distribution are approximately determined by the ratio and each doping concentration of the N-layer (Fig. 10).

Room is required for oscillation suppression. However, a large room lowers the breakdown voltage. Therefore, there is a trade-off between the breakdown voltage and the oscillation suppression effect. To meet the blocking voltage and the oscillation suppression effect, an optimized electric field distribution is acquired by a combination of trap ratio and doping concentration of the N-layer. The optimized distribution has an electric field

room and sufficient spreading space of the electric field (Fig. 11). Theoretically, a high trap ratio is required for a high doping concentration of the N-layer. The dependence between the oscillation suppression effect and the trap design was confirmed by TCAD simulation. The suppression effect was enhanced with a narrow trap pitch and a tall trap height, because the trapped hole increased and the electric field room became larger (Fig. 12).

3.4. Impact of oscillation prevention on reverse recovery time and reverse recovery loss

The proposed diode successfully achieved ultrafast reverse recovery without the oscillation (Fig. 13). For example, the proposed diode was two times faster at the forward voltage drop of 1.3 V than the state-of-the-art vertical Si-PiN diode. The N- thickness or width between the anode and cathode of the vertical diode and that of the proposed diode was 80 μm and 50 μm respectively, because of the best trade-off comparison without the waveform oscillation.

The trade-off curve between the reverse recovery time and the forward voltage drop clearly indicates the fast reverse recovery of the proposed diode (Fig. 14). The trade-off curve was calculated with an active chip area varying from 0.1 cm^2 to 1 cm^2 . The reverse recovery speed of the vertical diode was close to that of the proposed diode in the high forward voltage range by more than 1.5 V, because the long-term tail current of the vertical diode is not considered in the reverse recovery time under the latter's definition (Fig. 2).

The trade-off curve between the reverse recovery loss and forward voltage drop clearly indicates the low reverse recovery loss of the proposed diode (Fig. 15). The loss of the proposed diode reduced to one-half compared with the vertical diode.

Because the current flows in the thin Si layer, the proposed diode has a slight drawback. The forward voltage drop is slightly larger than that of the vertical diode for the same active chip area (Fig. 16). On the other hand, the reverse recovery time and reverse recovery loss are strongly reduced. The conduction loss of the proposed diode increased to 1.3 times that of the vertical diode for same active chip area.

When a 1- μm -thick Al electrode is assumed, the increase in the forward voltage drop becomes a severe problem because of the large sheet resistance value of approximately 30 $\text{m}\Omega/\text{sq}$. The voltage drop increase is estimated to be a few volts at the large forward current of 100 A. Therefore, special electrodes or wiring should be utilized for low resistance, for example, a thick copper electrode, or a number of bonding wires with every small chip area (Fig. 17).

4. Conclusion

Fast switching, low forward voltage drop, and low cost power semiconductor devices are required. In particular, fast reverse recovery (fast switching) has a large impact not only on the diode, but also on the switching device.

We have analytically calculated the reverse recovery speed by a bipolar device model and found that there is much room for faster reverse recovery between the state-of-the-art commercialized diode and the theoretical limit. On the other hand, it was also found by TCAD simulation that a fast Si-PiN diode induced a strong waveform oscillation during reverse recovery.

We proposed a lateral SOI diode with traps and achieved ultrafast reverse recovery and low reverse recovery loss without the oscillation. The trap concept would contribute to ultrafast switching (ultrafast reverse recovery) of all power devices including IGBTs and power MOSFETs.

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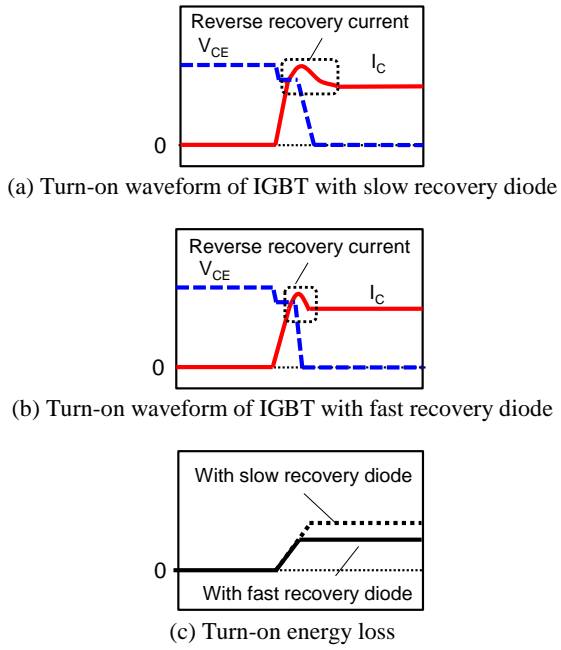


Fig. 1. Image of reduced turn-on energy with fast recovery diode.

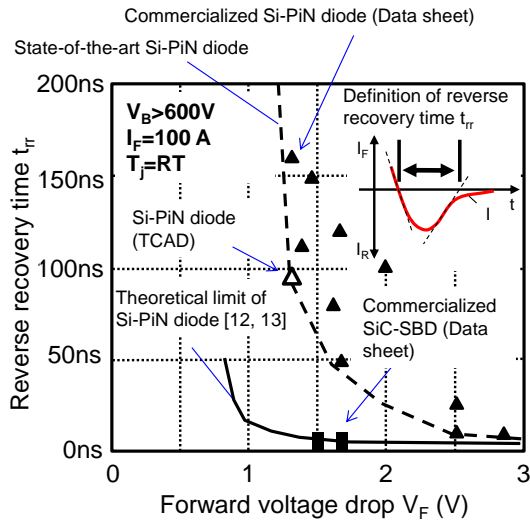


Fig. 2. Performance of state-of-the-art 600V Si-PiN diode and benchmarks.

Table 1. Simulated reverse recovery waveforms of conventional vertical diodes with different N- layer width.

Si-PiN Structure	100 μm	90 μm	40 μm
t_{rr} (ns)	150	130	110
$V_F @ 300A/cm^2(V)$	1.85	1.71	1.13
Reverse recovery waveform ($L_S=100nH$, $V_B>600V$, $T_J=RT$)			

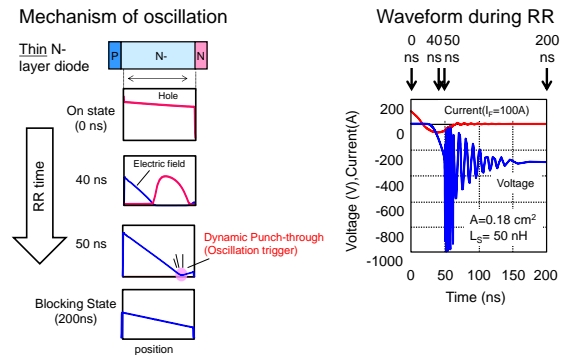


Fig. 3. Waveform oscillation trigger called “dynamic punch-through” in fast reverse recovery diode.

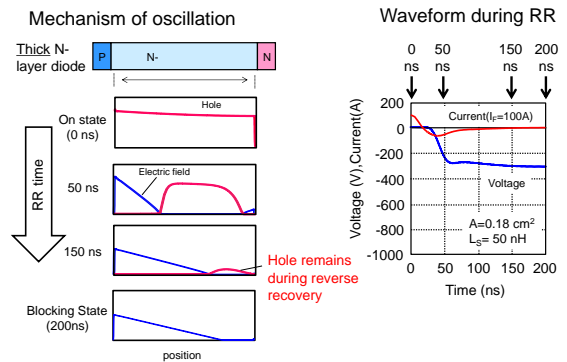


Fig. 4. “Dynamic punch-through” prevention in slow reverse recovery diode.

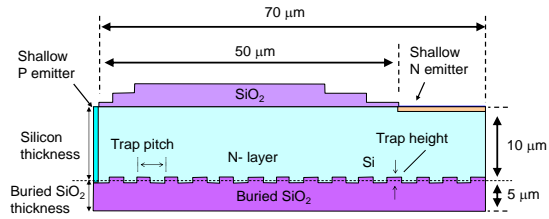


Fig. 5. Proposed lateral SOI diode with traps for fast reverse recovery.

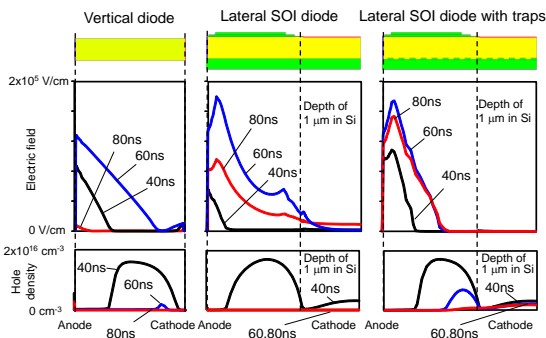


Fig. 7. Dynamic phenomena in N-layer corresponding reverse recovery of Fig. 6.

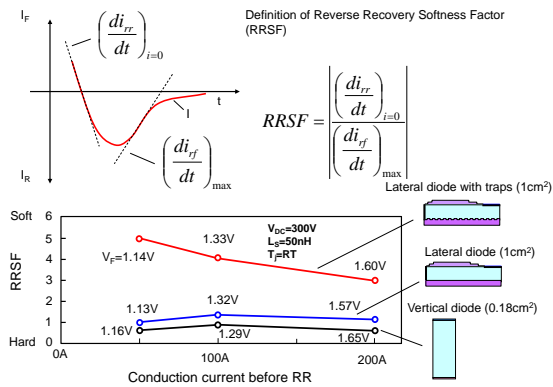
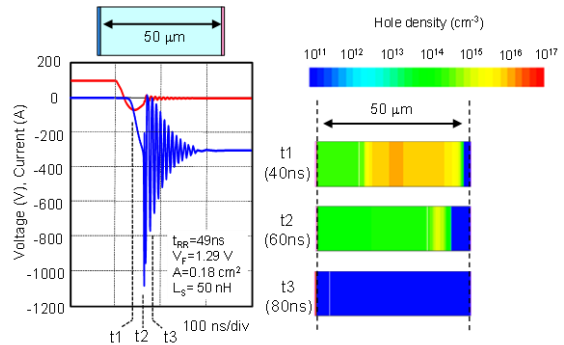
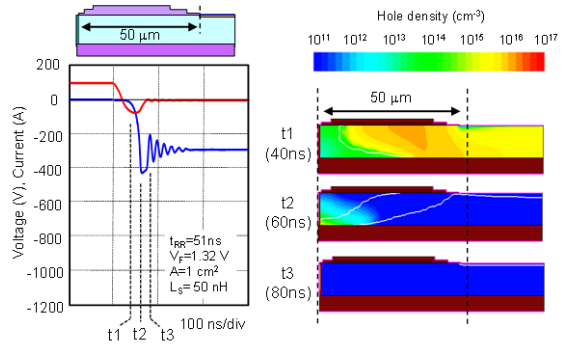


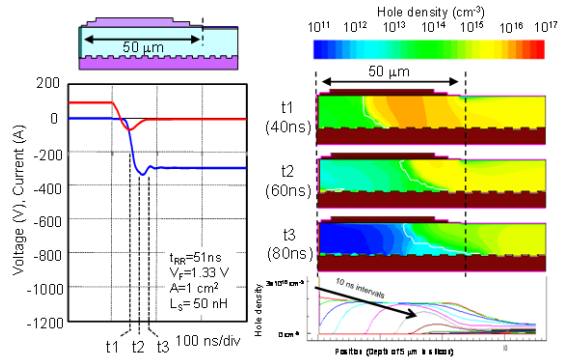
Fig. 8. Reverse Recovery Softness Factor (RRSF) of proposed diode and benchmarks.



(a) Vertical diode(Conventional diode)



(b) Lateral SOI diode



(c) Lateral SOI diode with traps (Proposed diode)

Fig. 6. Waveform and corresponding hole distribution during reverse recovery.

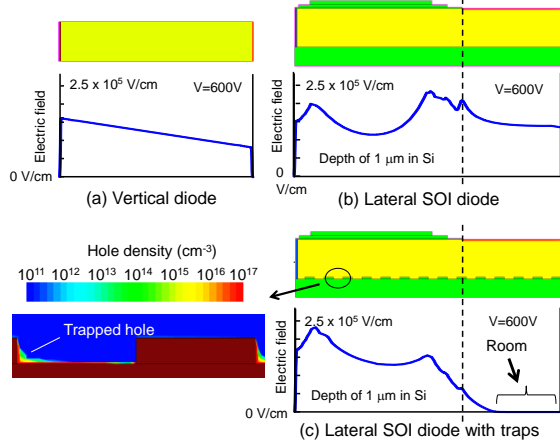


Fig. 9. Design and arrangement concept to prevent dynamic punch-through.

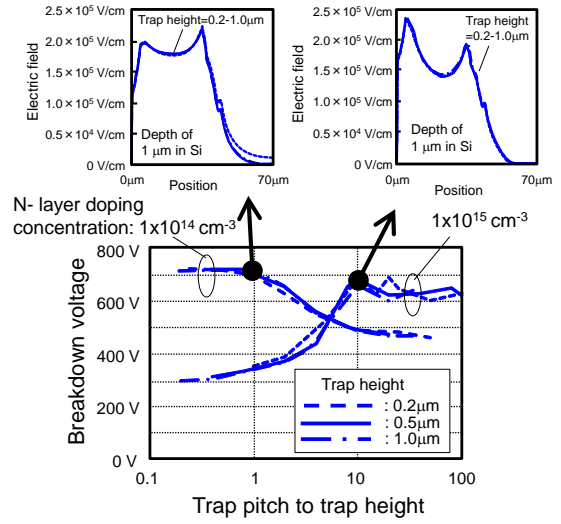


Fig. 10. Breakdown voltage and electric field determined by the ratio of trap pitch to trap height.

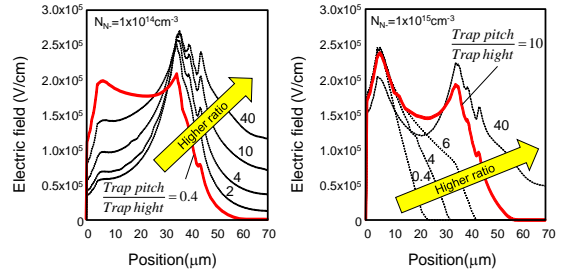


Fig. 11. Trap optimization for high breakdown voltage and oscillation suppression with electric field.

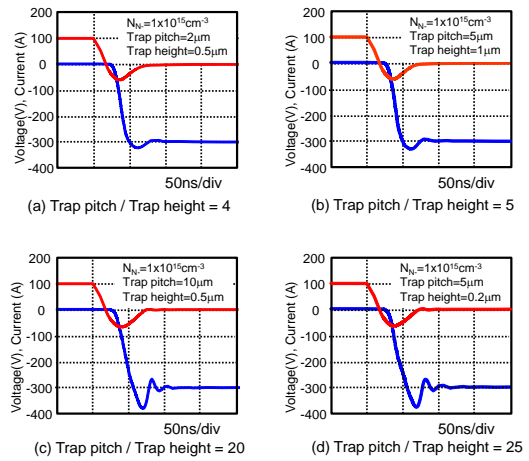


Fig. 12. Waveform oscillation effect of each trap design and arrangement.

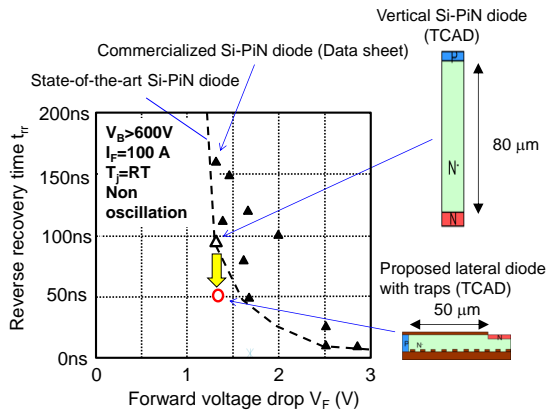


Fig. 13. Fast reverse recovery of proposed diode without oscillation.

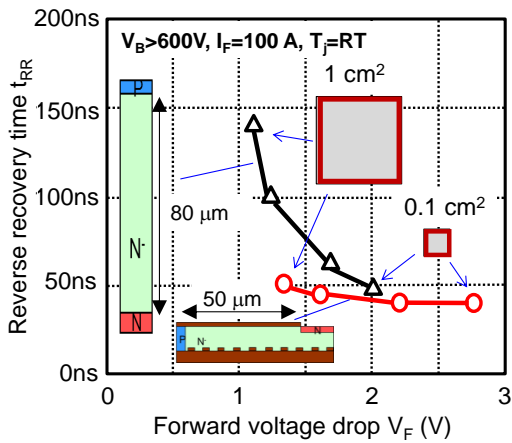


Fig. 14. Trade-off curve between reverse recovery time and forward voltage drop.

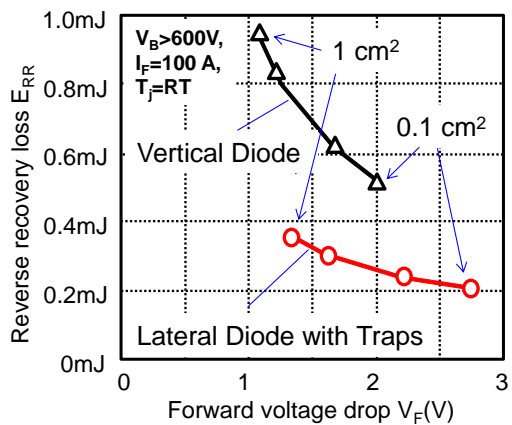


Fig. 15. Trade-off curve between reverse recovery loss and forward voltage drop.

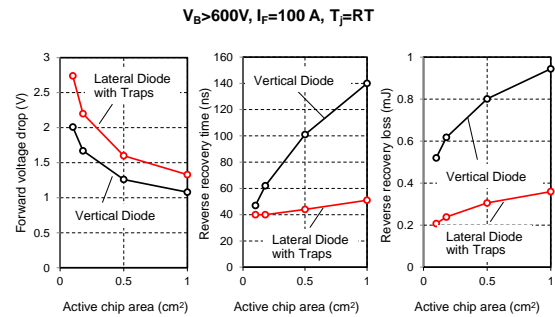


Fig. 16. Main diode characteristics dependence on active chip area.

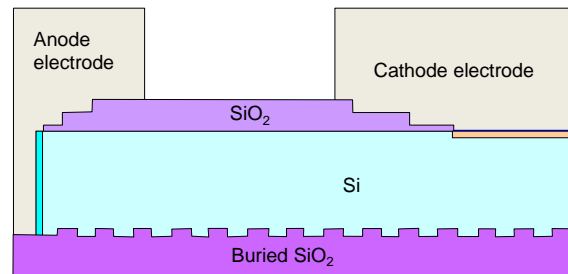


Fig. 17. Example of metal electrode.

According to Referee's comments, we revised our paper as following;

----- Referee 1 -----

- >Table 1: Condition Current density at VF or current and area to be given.
- >Is voltage drop in metallization and bond wires neglected?
- >Then this is to be mentioned.

We gave the current density in the Table 1 and mentioned the condition of voltage drop simulation in chapter 2 as "Please note that the forward voltage drop (VF) of electrode metal and bonding wires is not considered in this paper."

- >Fig. 2: For use of this RRSF definition, the parameters have to be given:
- > Applied voltage, current density, di/dt, circuit, inductance.
- >The RRSF can vary very strongly for the same diode if one of the parameters is modified.

We gave the applied voltage, current density, and stray inductance in chapter 2 as "The applied voltage is 300 V, current density is 250 A/cm², and stray inductance is 50 nH for TCAD simulation".
And we gave the applied voltage, stray inductance, junction temperature, and chip area in Fig. 8.

Fig. 3, 4: Now Current is displayed, area is to be given.

I gave the information of current and area in the Fig. 3, 4.

Fig. 6: To compare, device area for (a) and total silicon area for (b) and (c) is to be given.

It was mentioned as "A" in the Fig. 6.

- >Page 4: "The electric field of the vertical diode has a linear slope, corresponding to the doping concentration of the N-layer. At high blocking voltage, the electric field spreads all over the N-layer (Fig. 9).
- >" However, Fig. 9 shows a lateral diode.
- >Please improve this sentence.

We improved the sentence in chapter 3.3 as "The electric field of the vertical diode has a linear slope, corresponding to the doping concentration of the N-layer. At high blocking voltage, the electric field spreads all over the N-layer (Fig. 9(a))".

Fig. 9: resolution not good enough, text too small.

We enlarged the Fig. 9.

----- Referee 2 -----

- >In Fig. 1, two times "slow-recovery diode" is used as caption (a,b).
- >On which base the theoretical limit of the Si-PIN diode was calculated? Please describe more in detail.

We corrected the Fig. 1.

We described the detail in chapter 2 as "The theoretical reverse recovery time limit is calculated with flat carrier distribution, so it's assumed that only drift current flows in the N- layer [16]".

>How the junction termination will be applied?

We described the detail in chapter 3.1 as “And about junction termination, dielectric separation technology like power IC can be applied for this proposed structure”.

>You write that you have a disadvantage regarding higher forward voltage drops.

>Can you please make a drawing of a contacting concept for this type of lateral diode.

>You have to bring the anode contact to the top of the device to carry higher current densities.

We made a drawing in the Fig. 17.

>Fig. 6b t2 --> Why there are still holes beneath the anode electrode, despite the charge-carrier hill already disappeared?

>Is it due to Impact Ionization?

We mentioned it in the chapter 3.2 as “the hole of the lateral SOI diode was also completely swept out of the N-layer by the electric field during the reverse recovery with impact ionization”.

>RRSF -> Info: also called "soft factor" in [21, Lutz et al]

We mentioned it in the chapter 3.2 as “the advantage of the proposed diode is clearly indicated from the aspect of the Reverse Recovery Softness Factor (RRSF) [27] (also called “soft factor [21])”.

Maybe the headline "with traps for preventing..." is not the best wording? Traps are often known as special recombination centres. You use more a "geometric" trap.

We will request the change of headline as “Ultrafast lateral 600 V silicon SOI PiN diode with geometric traps for preventing waveform oscillation”.

And we request the change of affiliation name and e-mail address aside from referee's comments because our affiliation name was changed from “International Centre for the Study of East Asian Development (ICSEAD)” to “Asian Growth Research Institute (AGI)”.