Smart Power Devices and ICs Using GaAs and Wide and Extreme Bandgap Semiconductors

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Abstract—We evaluate and compare the performance and potential of GaAs and of wide and extreme bandgap semiconductors (SiC, GaN, Ga_2O_3, diamond), relative to silicon, for power electronics applications. We examine their device structures and associated materials/process technologies and selectively review the recent experimental demonstrations of high voltage power devices and IC structures of these semiconductors. We discuss the technical obstacles that still need to be addressed and overcome before large-scale commercialization commences.

I. Introduction

a. Material properties

Silicon has long been the dominant, often exclusive semiconductor of choice for high voltage power devices [1,2]. Over the last three decades, a succession of alternatives have been proposed to augment silicon power devices. First GaAs, then wide bandgap semiconductors (WBG), SiC and GaN, and ultrawide or extreme bandgap semiconductors, like diamond, AlN, and more recently, Ga_2O_3, devices, due to their appealing physical properties, such as electric breakdown field, intrinsic carrier concentration and thermal conductivity.

In Table 1, the relevant material and electrical properties of GaAs, SiC, GaN, Ga_2O_3, diamond and AlN are shown and compared to those of silicon. Superior power device performance, when compared to that of silicon devices, has been projected using these material parameters. Consequently, first GaAs, then SiC and GaN power devices, as well as diamond and AlN, have been under active research and development. Though GaAs vertical Schottky diodes have long been available commercially, SiC power diodes, first available in 2001, have now become established as critical components in advanced power electronics systems.

Material	E_g (eV)	*Direct/ Indirect*	n_i (cm^{-3})	ε_r	μ_n ($cm^2/V\text{-}s$)	E_c (MV/cm)	v_{sat} (10^7 cm/s)	λ (W/cm-*K*)
Si	1.12	I	1.5×10^{10}	11.8	1350	0.25	1.0	1.5
GaAs	1.42	D	1.8×10^{6}	13.1	8500	0.4	1.2	0.55
2H-GaN	3.39	D	1.9×10^{-10}	9.9	1000^a 2000**	3.3* 3.75^a	2.5	2.5 4.1*
4H-SiC	3.26	I	8.2×10^{-9}	10	720^a 650^c	2.0^a	2.0	4.5
Ga_2O_3	4.5-4.9	D	2.6×10^{-19}-1.2×10^{-22}	10	300	8	-	0.13-0.21
Diamond	5.45	I	1.6×10^{-27}	5.5	2800	10	2.7	22
2H-AlN	6.2	D	$\sim10^{-34}$	8.5	300	12*	1.7	2.85

Table 1. Material and electrical properties of various semiconductors. Note: a – mobility along a-axis, c-mobility along c-axis, *Estimated value, **2DEG

Here, we first perform a comparative evaluation of these semiconductors, using salient figures of merit and specific on-resistance vs. breakdown voltage to highlight the potential improvement possible and to offer a comparative assessment of their applicable blocking voltage ranges. We also contrast differences in device structures and associated material/process technologies for Si, SiC, GaAs, and GaN. We selectively review the recent experimental demonstrations of GaAs, SiC, GaN, Ga_2O_3, and diamond high voltage power devices and IC structures. Finally, we detail the technical obstacles that still need to be overcome before widespread commercialization can take place.

b. Power Electronics Applications

1 Categories of WBG device applications and comparison to silicon

Due to their extreme intrinsic material characteristics, WBG power semiconductor devices have several advantages over

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silicon in power electronics applications. Table 2 categorizes the advantages of WBG ([3]). Some applications of silicon unipolar devices such as the power MOSFET and superjunction (SJ) MOSFET for voltage ranges below 1000V are well served by WBG unipolar devices (Category 1) with higher switching speed and lower conduction losses. Specfically, high switching speed is expected for lateral unipolar devices such as AlGaN/GaN HFETs and low conduction loss is expected for vertical devices such as SiC FETs.

Applications currently served by silicon double injection bipolar devices such as IGBTs and PiN diodes in the voltage range from 400V to 3000V will transition to unipolar WBG devices (Category 2) with higher switching speed and lower conduction losses. In the 2.5kV to 8kV voltage range, double injection bipolar WBG devices such as SiC-IGBTs and SiC-PiN diodes will replace silicon thyristors in some applications (Category 3). Replacement of silicon by WBG devices in this category will be limited to higher switching speed applications due to the relatively high on-state voltages of WGB bipolar devices. For voltages over 8kV, new applications for WBG devices are expected. It should be noted that use of devices rated to 8kV or higher reduces series connections in high voltage power system applications.

	Voltage range	Silicon device		WBG device	Advantage
CATEGORY 1	~1000V	MOSFET	→	Unipolar*	Low loss High speed
CATEGORY 2	400-3000V	IGBT(bipolar)	→	Unipolar*	Low loss High speed
CATEGORY 3	2.5k- 8kV	IGBT/Thyristor	→	Bipolar**	High speed
CATEGORY 4	over 8kV	none	→	Bipolar**	New applications

* MISFET, MESFET, HFET, SIT, low injection BJT etc.
** Double injection bipolar device such as IGBTs, Thyristors

Table 2 Four categories of WBG device possibility

2 Existing applications and WGB device possibilities

Typical silicon device applications and possible WBG power semiconductor replacements are shown in Table 3. WBG double injection bipolar devices such as SiC-thyristors and SiC-IGBTs are candidates to replace silicon thyristors and IGBTs in high voltage DC transmission applications. In the 25kV range, WBG conduction losses are significantly lower than those of silicon devices. The same voltage range devices can be used for medium voltage AC drives and traction applications for high frequency 2-level inverter/converter

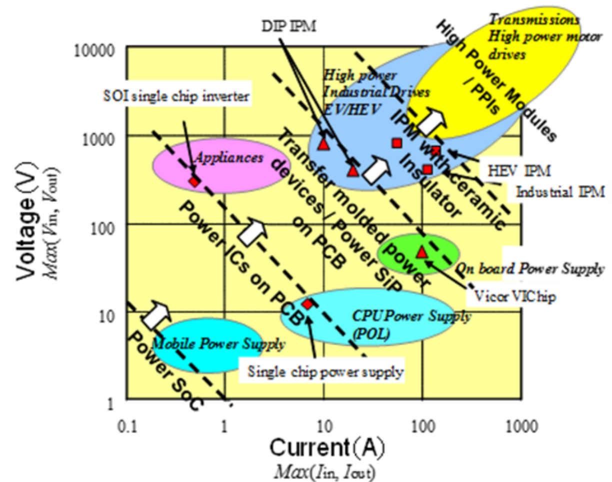


Fig. 1 Voltage-current range of power electronics applications and integration and packaging technology. Arrows show the advantage of WBG device on package, assembling and power ICs.

Application	System Power, voltage	Typical Device type	Typical Circuit topology	Device Voltage and current	Switching Frequency	Package	WBG device possibility
UHVDC	1GW-8GW -800kV	Thyristor	MMC / series connected	4.5kV-8kV 3kA-5kA	50-60Hz	Pressure contact	>25kV SiC/GaN double injection bipolar, >50kV diamond device
HVDC	50MW-1GW 40kV – 250kV	IGBT	MMC / series connected	2.5kV-6.5kV 2kA-3kA	>50Hz	Pressure contact	>25kV SiC/GaN double injection bipolar, >50kV diamond device
Medium voltage AC drives / Traction	1MW-50MW	IGBT IGCT (GTO)	2-level / 3-level voltage source inverter	2.5kV-6.5kV 0.5kA-8kA	>300Hz	Module, Pressure contact	WBG vertical unipolar device with new topology at higher frequency, 13-25kV Double injection bipolar with high frequency 2-level
EV/HEV power train	10-200kW	IGBT	2-level voltage source inverter / chopper	500V-1000V 100A-500A	1kHz-5kHz	6 in 1, 12 in 1 module, water cooled	Vertical unipolar device, higher frequency
Wind-firm	1MW-5MW	IGBT	2-level / 3-level voltage source inverter	1000V-6.5kV 500A-2.5kA	500Hz-5kHz	DBC Module, Pressure contact	Vertical unipolar device
Large scale PV-inverter	100kW-3MW	IGBT	2-level / 3-level voltage source inverter	1000V-6.5kV 500A-2.5kA	500Hz-5kHz	DBC Module	Vertical unipolar device
Data center HVDC	100kW-1MW	IGBT, SJ-MOSFET	Isolated DC-DC	800-1.2kV 25A-250A	>10kHz	Transfer molded discrete, DBC Module	Vertical unipolar device, higher frequency
Appliance (Air-conditioner)	1kW-2kW	IGBT / SJ-MOSFET	2-level voltage source inverter	600V 5A-10A	1-10kHz	Transfer molded module	WBG Power IC
IH-cooker	1-3kW	IGBT	Soft switching	600V 5A-10A	30kHz-	Transfer molded discrete	WBG Power IC
EV Quick charger	20-50kW	IGBT SJ-MOSFET	2 level converter, Isolated DC-DC	600V-1200V 20A-100A	5kHz-50kHz	Transfer molded discrete, DBC module	Vertical unipolar device, higher frequency
EV charger	1.5-5kV	IGBT SJ-MOSFET	2 level converter Isolated DC-DC	600V 5-10A	5-50kHz	Transfer Molded discrete, DBC module	Vertical unipolar device, power IC with higher frequency

Table 3: Power electronics applications and possible WBG device replacement.

systems with smaller filter sizes. For EV/HEV applications at lower output power ranges, WBG unipolar vertical devices such as SBDs will have higher efficiency at high switching frequency than silicon IGBTs and PiN diodes leading to smaller magnetic core sizes in the bi-directional chopper circuit connecting the battery and motor. The impact of WBG devices on power ICs is shown in Fig. 1. Specially, WBG lateral devices will expand the application area for power ICs([4]).

II. Power Device Structures

The structures of SiC vertical power transistors, shown in Fig. 2, strongly resemble those of silicon power devices. This is due to process similarities and the indirect bandgap of both semiconductors (making bipolar transistors feasible). While diamond is also an indirect semiconductor, it is difficult to dope it n-type and its MOS capability is not fully developed. It is difficult to achieve p-type doping in Ga_2O_3, but its MOS properties appear to be acceptable. However, it is a direct semiconductor so BJTs and IGBTs are not feasible.

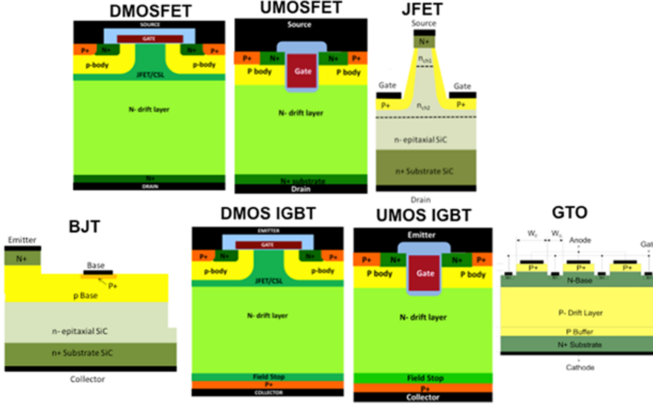


Fig. 2: SiC Vertical Power Transistor Structures

The structures of SiC and GaN lateral power transistors are shown in Fig. 3. The lateral RESURF-type SiC MOSFET is identical to its Si counterpart, and the lateral AlGaN/GaN power HEMTs are very similar to AlGaAs/GaAs HEMTs. Interestingly, lateral GaN RESURF MOSFETs, lateral Ga_2O_3 depletion-mode MOSFETs, lateral diamond MOSFETs, and diamond HEMTs with two dimensional hole gas (2DHG) layers, have all been experimentally demonstrated. Some of these devices will be described more fully.

III. FOM and Projected Performance

To predict the performance of power devices using wide to extreme bandgap semiconductors and to quantitatively evaluate them in comparison with their silicon counterparts, several figures of merit (FoM) have been proposed to [5-8]. The most general and relevant are the following: (a) Unipolar figures of merit UFM_1 ($\equiv \varepsilon\mu E_C^3$, identical to Baliga's Figure of Merit, BM) [5], UFM_2 ($\equiv \lambda\varepsilon\mu E_C^3$) and UFM_3 ($\equiv \mu E_C^2$,

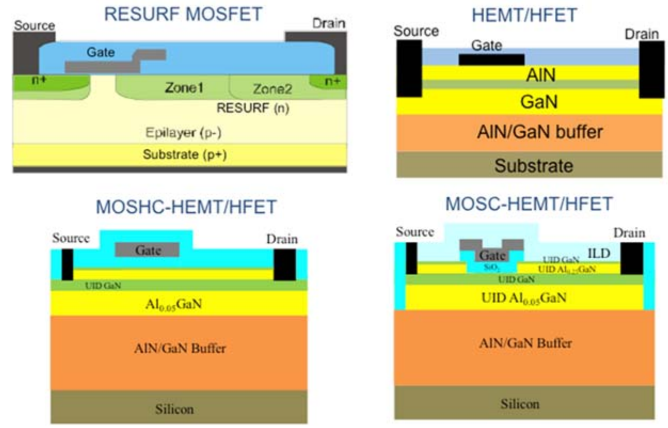


Fig. 3: Lateral Power Transistor Structures

identical to Baliga's High-Frequency Figure of Merit, BHFM) [7] and UFM_4 ($\equiv \lambda\mu E_C^2$). Of these, UFM_2 is best when conduction power loss dominates and UFM_4 is best when switching power loss is comparable to the conduction loss, because thermal conductivity is explicitly included. Table 4 summarizes these FoM for the semiconductors in Table 1. For comparisons between bipolar power devices, different figures of merit need to be used, dependent on whether the device has an odd or even number of junctions [9]. It may be noted that, besides SiC and GaN, diamond and AlN are the next generation of power devices. Ga_2O_3 is not as desirable due to its poor thermal conductivity.

Material	UFM_1 (BFM) $\varepsilon\mu E_c^3$	UFM_2 $\lambda\varepsilon\mu E_c^3$	UFM_3 (BHFM) μE_c^2	UFM_4 $\lambda\mu E_c^2$
Si	1	1	1	1
GaAs	29	11	16	6
GaN	2097	3496	167	278
4H-SiC	231	694	34	102
Ga_2O_3	6170	535	278	20
p-Diamond	$8.4x10^4$	$1.2x10^6$	4504	$6.6x10^4$
AlN	$1.8x10^4$	$3.4x10^4$	512	973

Table 4 FoMs for vertical power devices of various semiconductors.

When the conduction loss is the dominant power loss, we can define a cross-over voltage, VCO. This voltage is the blocking voltage at which the unipolar power device has the same conduction loss at the same forward current density as the analogous bipolar power device of the same semiconductor. For silicon (comparing the power MOSFET with the IGBT), this cross-over voltage is about 500V. For SiC, VCO is over 5kV [10], due principally to its approximately 2.7V turn-on knee, which is proportional to the bandgap. The turn-on knee is only 0.6V for Si. For diamond, VCO is estimated to be well over 25kV. Note that the VCO criterion does not apply to bipolar power devices with an even number of pn junctions such as the BJT [10], since they do not include a diode-drop overhead. From this discussion, for the replacement of Si IGBTs, we can see that between the

blocking voltage of 500 and 5kV, SiC power MOSFETs have lower conduction loss than Si IGBTs. Above 5kV, SiC IGBTs need to be used. Another perspective from this examination is that, if we are willing to use wider bandgap semiconductors, we can always use unipolar diodes and FETs regardless of blocking voltage rating. As higher blocking voltages are required, we can deploy unipolar power devices made of larger bandgap semiconductors, first SiC and GaN, and then diamond and AlN.

Material	Q_S	μ_n	$LUFM_1$ (BFM) $\mu Q E_c^2$	$LUFM_2$ $\lambda \mu Q E_c^2$
Si	1	1	1	1
GaAs	1.6	10	41	15
GaN	15	2.5	8438	3496
4H-SiC	8	0.8	410	1229
Ga_2O_3	32	0.38	12452	1079
n-Diamond	40	2.5	$1.6x10^5$	$2.3x10^6$

Table 5 FoMs for lateral power devices of various semiconductors.

For lateral RESURF-type [11] power devices, alternate FoMs need to be used since in these devices 2 and 3 dimensional electric field effects preclude the use of simple triangular field models. For heterojunction devices, alternate FoMs are required to account for dopant-independent carrier concentration and the lack of significant impurity scattering. Recently, a FoM for the lateral HEMT ($LHUFM_1$) has been proposed [12]. This figure is not ideal, since it fails to account both for device thermal conductivity effects, and also for doping dependent mobility in device drift layers (eg. lateral power MOSFETs with doped drift layers, such as lateral RESURF-type Si, SiC or Ga_2O_3 power MOSFETs). Nevertheless, this FOM can be used for GaAs, GaN and Diamond HEMTs. In Table 5, a refined HEMT FoM (defined as $LHUFM_2 \equiv LHUFM1 \times \lambda$) clearly illustrates the superiority of diamond as compared to GaN, SiC and Ga_2O_3, and the inferiority of Si and GaAs

Items	Values and assumptions	Remarks
Device voltage	600V, 1200V, 4.5kV, 25kV classes	20% margin added for breakdown voltage
FET model	Classical model with triangle electric field distribution along N-drift	
Superjunction model	P-column and N-column has same aspect ration of 10.	
IGBT model (Double injection device model)	Flat stored carrier distribution in N-base is assumed (i.e. sufficiently long carrier lifetime is assumed) with giving stored carrier density of 1.0-2.0e16/cm^3. Forward offset voltage is calculated from the ratio of stored carrier density to intrinsic carrier density.	Soft Punch-through design for IGBT.
Conduction loss density limit	≤300W/cm^2 for 600V and 1200V, ≤200W/cm^2 for 4.5kV, ≤100W/cm^2 for 25kV	Used for chip area calculation
Series resistances	Total series resistance (sum of channel resistance, JFET resistance, substrate resistance, contact resistance etc.) is assumed to be 0.1mΩcm^2	Series resistance is added to device resistance
Chip area for 100A device	Chip active area is determined to fit the conduction loss density (W/cm^2) limit for 100A conduction. Edge termination area is not included.	Corresponding to chip area for rated current of 100A
Forward voltage drop (at30A)	Voltage drop at conduction current of 30A	30% of rated current as average operation condition
Switching time (at 30A)	Discharge time of Q_{OSS} at 30A switching. Q_{OSS} is set to N-drift depletion charge at half of device voltage for FET, PN column depletion charge for SJ-MOSFET and open base turn-off charge for sweeping out total stored charge in N-base for IGBT.	30% of rated current

Table 6 Performance calculation methods for vertical power devices

Vertical devices

Based on material properties, vertical power device performances are calculated using the methods and assumptions shown in Table 6. Voltage classes considered here are 600V, 1200V, 4.5kV and 25kV. Chip area is one of the most important considerations for WBG device commercialization and this is reflected in the models for device operation and power dissipation density. Chip active area for 100A devices is calculated with an assumed conduction loss density limit (300W/cm^2 for 600V and 1200V, 200W/cm^2 for 4.5kV, 100W/cm^2 for 25kV device chips), corresponding to conduction power loss divided by chip area. The minimum chip area for a 100A device with the assumed maximum power loss density is defined as the chip area for 100A rated current. Forward voltage drops and switching times at 30A are calculated to simulate characteristics under real operating conditions. Switching time is the discharge time of Qoss for FETs and the open base turn-off time for IGBTs, (i.e. time to collect injection-efficiency determined stored base minority carriers). A fixed series resistance of 0.1mΩcm^2 is added for all devices to model channel resistance, JFET resistance, contact resistance, and substrate resistance.

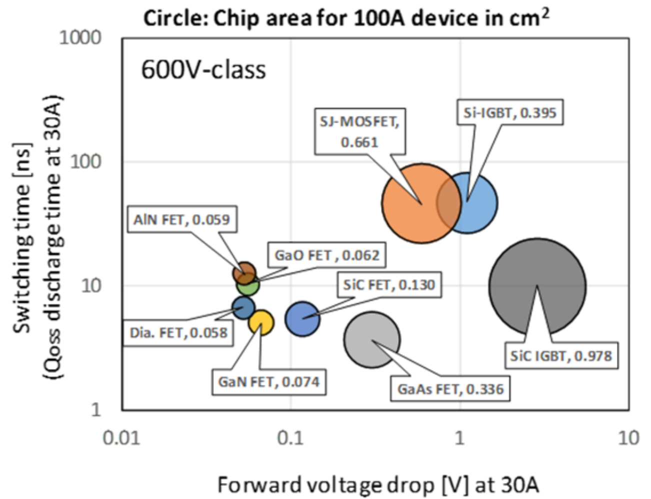
It should be noted that the calculated performances are sensitive to measured material properties and assumptions, so the advantage/disadvantage relations may change as more accurate material properties become available. For the 600V and 1200V classes, WBG devices have significant advantages over silicon superjunction devices and IGBTs both in conduction and switching performances as shown in Fig. 4. When high speed switching is the overriding requirement, GaAs transistors are best in this voltage range and lower. Despite intrinsic material performance differences between Ga_2O_3, diamond, GaN and AlN, in this voltage range device series resistance (the sum of channel resistance, JFET resistance, contact resistance and substrate resistance) is the limiting factor so that overall device performance for the three materials is substantially similar. Although SiC-IGBTs show some advantage over silicon in calculated performance, larger chip areas and higher forward voltage drops are the theoretical limitation with the carrier injection (conduction modulation) mechanism in WBG devices.

As shown in Fig. 5, for the 4.5kV range, SiC-MOSFETs are both larger and better performing than silicon IGBTs. Only WGB devices are feasible in the 25kV range, the new frontier of power device applications.

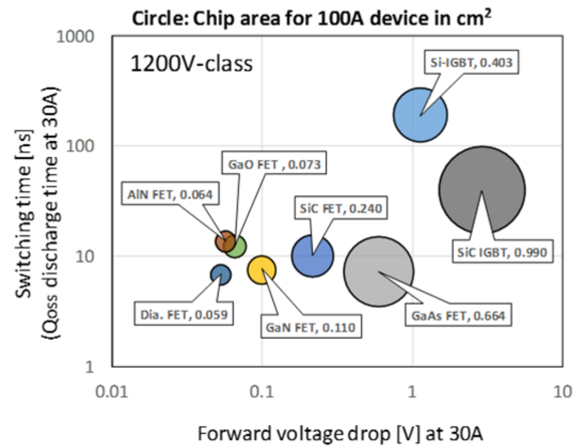
Lateral devices

Based on material properties, lateral power device performances are calculated based on the method explained in Table 7. Voltage classes are 100 and 500V. Since lateral devices have the advantage in high frequency performance rather than specific on-state resistance $R_{on}A$[Ωcm2], $R_{on}Q_{oss}$ [V-sec] is selected as the performance index. A fixed series resistance of 0.5Ωmm is added to the on-state resistance for all devices to model the channel contact resistances. It should be noted that the calculated performances are sensitive to the assumed material properties, so that the advantage / disadvantage relation can change as more accurately measured material properties become available.

Both 100V and 500V class WBG devices have a significant advantage over silicon lateral devices, including GaAs transistors. The series resistance (sum of channel resistance and contact resistance) acts as a “performance limiter”, indicating that the parasitic series resistance reduction is important for GaN, Ga_2O_3, AlN and diamond.

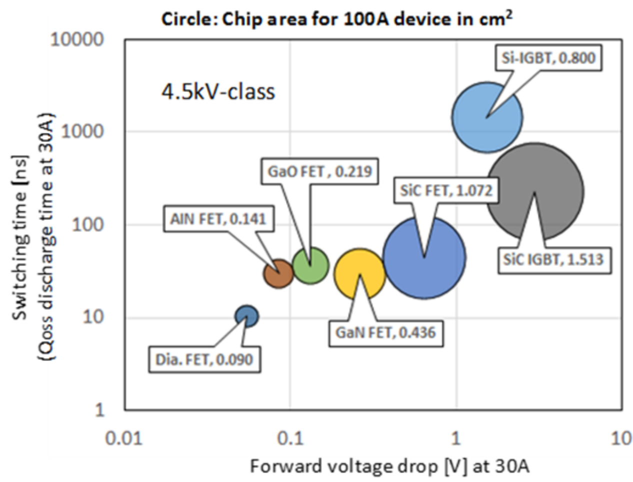


(a) 600V class vertical device performance and chip area

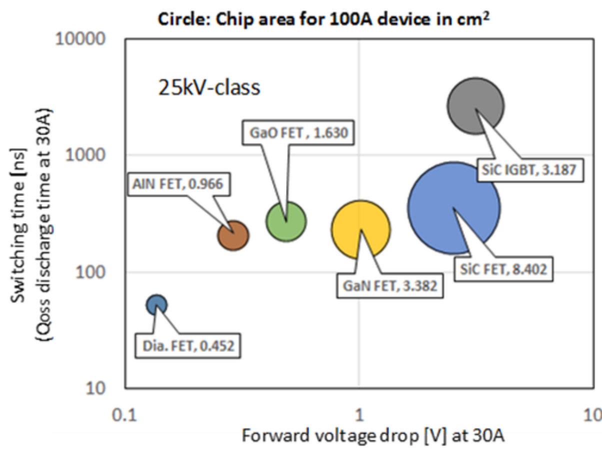


(b) 1200V class vertical device performance and chip area

Fig. 4 Calculated forward voltage drop and switching time with chip area for 600V devices (a) and 1200V devices(b). Area of circle and the number in the label show chip area for 100A rated current. Horizontal and vertical axes show forward voltage drop and switching time under 30A operation, respectively. Fixed series resistance of 0.1mΩcm^2 is added for all material devices in the calculation to consider channel resistance, JFET resistance, contact resistance and substrate resistance

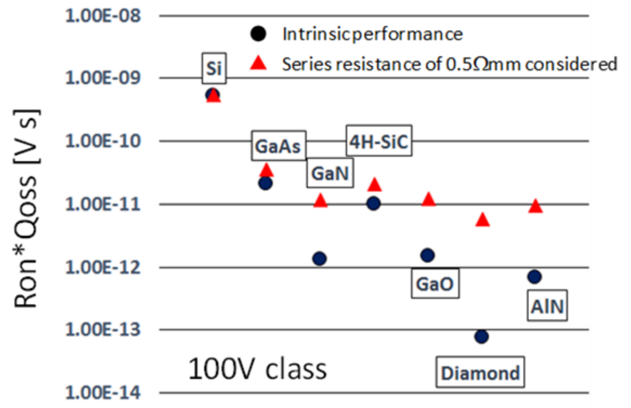


(a) 4.5kV vertical device performance and chip area.

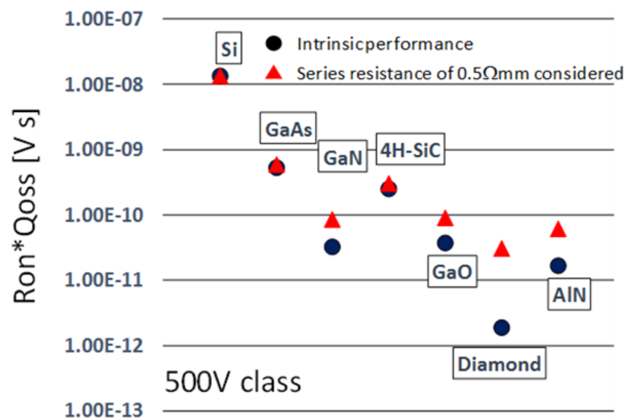


(b) 25kV vertical device performance and chip area.

Fig. 5 Calculated forward voltage drop and switching time with chip area for 4.5kV devices (a) and 25kV devices(b). Area of circle and the number in the label show chip area for 100A rated current. Horizontal and vertical axes show forward voltage drop and switching time under 30A operation respectively. Fixed series resistance of 0.1mΩcm^2 is added for all material devices in the calculation to consider channel resistance, JFET resistance, contact resistance and substrate resistance.



a) 100V class lateral device performance comparison



b) 500V class lateral device performance comparison

Fig. 6 Calculated Ron*Qoss for 100V devices (a) and 500V devices(b). Circle marks show the intrinsic performances and triangle marks show performances with series resistance of 0.5Ωmm as representative of contact resistances and channel resistance.

Items	Values and assumptions	Remarks
Device voltage	100V, 500V classes	20% margin added for breakdown voltage
Drift layer model	Critical electric field is decomposed to horizontal part and vertical part so that horizontal part is used for drift layer length calculation and vertical part field for drift layer conduction charge density calculation.	
Ooss/W	Assumed to be total conduction electron charge in drift layer for device width W	
Ron*W	-Intrinsic drift layer resistance for device width W or -Sum of intrinsic drift layer resistance and additional series resistance of 0.5Ωmm. The series resistance represents channel resistance, contact resistance etc.	2DEG mobility is used for GaN
Ron*Qoss	FOM for high voltage lateral high speed device.	Gate driving effect is not included in the model

Table 7 Performance calculation method for lateral power devices

Materials/Process Technologies

SiC, like Si, is an indirect semiconductor and large-diameter, heavily doped n-type substrates up to 200mm in diameter are available. Also, like silicon, a thermally grown SiO_2 layer and n and p-type dopant implantations are possible, so MOS devices with implanted source/drain regions are possible. Hence, most of the power device structures are vertical for efficient current conduction and quite similar to those of silicon power devices. These include Schottky and junction rectifiers, power MOSFETs, IGBTs and thyristors [10].

By contrast, GaN technology strongly resembles that of GaAs in its use of heterojunctions and composition grading with In or Al to achieve custom bandgaps and band offsets. In addition, since native GaN substrates have only become available recently, most commercial GaN devices have been fabricated on sapphire or silicon substrates. Like for GaAs, heteroepitaxy instead of homoepitaxy has been the perfered method of GaN active layer growth. Due to its direct bandgap, the basic GaN electronic device building blocks are unipolar - Schottky diodes and FETs. Therefore, it is not surprising that the power transistors commercially available are lateral AlGaN/GaN heterojunction pseudomorphic HEMTs on silicon substrates. Further for GaN (and GaAs), p-n junctions can only be fabricated epitaxially, since ion implantation of acceptors also produces compensating donor-like defects. On the other hand, GaN MOS structures are much easier to fabricate than GaAs MOS structures and, in fact, the inversion electron mobility of (0001) GaN on sapphire has been shown to be much higher than that of (0001) 4H-SiC, despite much less effort expended [13,14].

Due to their respective resemblance to Si and GaAs materials and process technologies, it is natural that the SiC device processing shares many features with silicon discrete power device processing while GaN device fabrication sequences have borrowed many unit process steps from those of GaAs HEMTs. Nevertheless, vertical GaN power devices are presently under active research, and, if proven successful, vertical GaN power devices may also adopt many aspects of vertical discrete silicon power devices.

The extreme bandgap semiconductors of diamond and Ga_2O_3 have many materials properties that resemble Si while AlN resembles the narrower bandgap nitride semiconductors.

IV. Representative Examples and Performances

GaAs

Gallium Arsenide Based Lateral Power Devices

Gallium Arsenide semiconductor technology was pioneered in the 1970's, and is now commercially used for RF power, optoelectronics and solid state lighting applications. The advantages of GaAs over silicon are its high electron mobility, higher bandgap and consequently higher field critical electric field strength and operating temperature, and the availability of a semi-insulating substrate to provide natural isolation and minimize parasitics. The most widely used FET in the GaAs material system is the Pseudomorphic High Electron Mobility Transistor (p-HEMT), shown in Figure 7, in which a high mobility 2D electron gas is introduced in a pseudomorphic InGaAs layer sandwiched between two higher bandgap layers, which are typically AlGaAs [17-18].

In a GaAs pHEMT, a 2D electron gas is responsible for conduction in both the channel and drift region, and hence the achievable electron mobility is much higher than conventional drift devices and is very close to the phonon scattering limit. A carrier mobility of over 6000 $cm^2V^{-1}s^{-1}$ can be obtained at room temperature for a sheet carrier concentration of $3x10^{12}$ cm^{-2} in the pHEMT. The electron mobility is therefore about 4x higher than for AlGaN/GaN (with ~1500 $cm^2V^{-1}s^{-1}$) and 5x higher than silicon drift (1200 $cm^2V^{-1}s^{-1}$). The electron mobility advantage translates to superior power device performance for lateral power devices. This is especially evident for low voltage devices (BV<50 V), where the extrinsic components like the channel, contact and access resistances are critical to device performance. In addition GaAs pHEMTs have the advantage of the semi-insulating GaAs substrate, which provides natural electrical isolation and minimizes parasitics for power ICs.

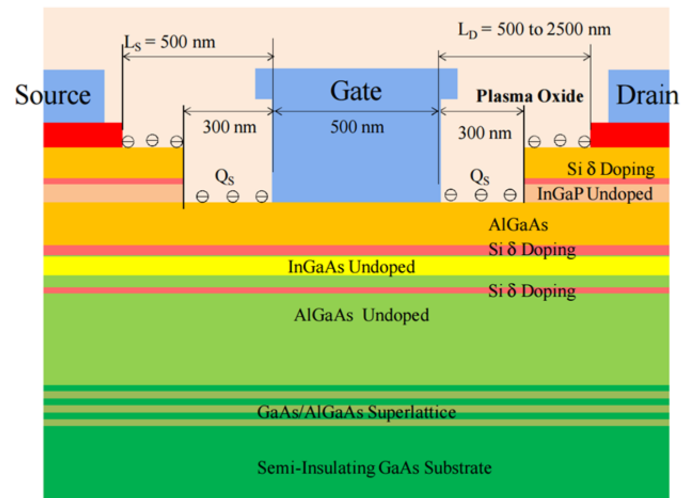


Figure 7: Cross section of a pseudomorphic HEMT

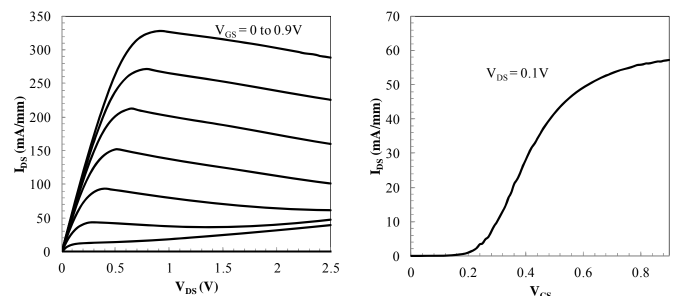


Figure 8: Output and transfer characteristics of the GaAs pHEMT with LD=500nm and BV of 11 V

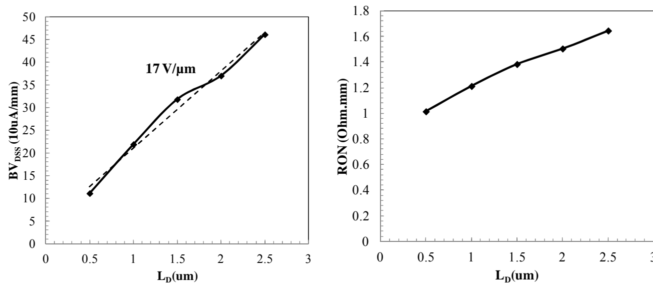


Figure 9: Breakdown voltage and ON Resistance of the GaAs pHEMT as a function of drift length.

In extended drain pHEMT devices, charge compensation by charges at the surface passivation can be used to increase the breakdown voltage. Using a double recess structure, breakdown voltages of up to 47V have been obtained in this structure in [19] for an enhancement mode device. The output and transfer characteristics of the device are shown in Fig. 8. The breakdown voltage and specific on-state resistance (in Ohm mm) is shown in Fig. 9.

When comparing the on-state resistance and gate charge, 22V and 32V pHEMTs show an order of magnitude improvement over commercially available 20V silicon NMOSFETs as shown in Fig. 10. Also shown is the calculated limit for a 0.5 µm minimum feature size pHEMT process. Due to their low gate charge and low on-state resistance, GaAs pHEMTs can enable power converters with higher efficiencies at higher frequencies and with smaller die areas than silicon devices.

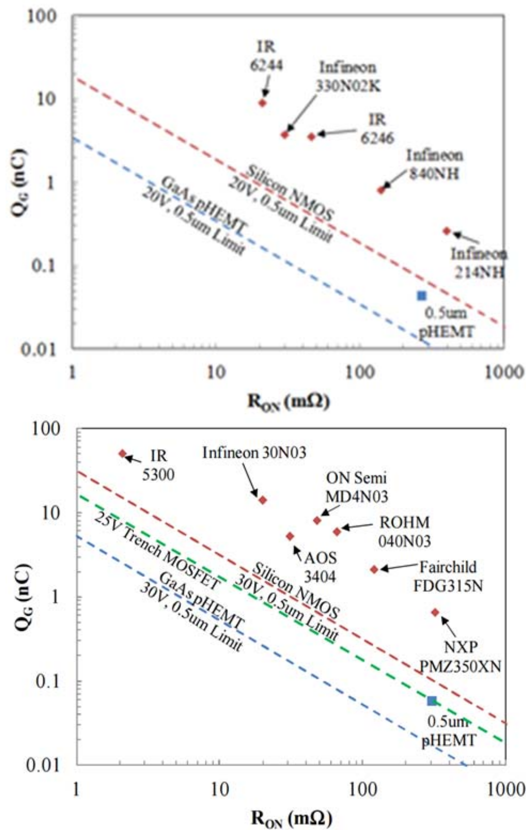


Figure 10: Performance of the 22V and 32 V pHEMT compared to Silicon NMOSFETs. Also shown are the intrinsic limits for a 0.5 um feature size.

Because of their natural isolation from their substrate and superior figure of merit, GaAs pHEMTs are well suited for integrated power ICs switching from 10s of MHz to 100s of MHz, an order of magnitude higher than where most power ICs operate today. A pHEMT buck converter IC [20] is shown in Fig.11. In this chip, 11V rated enhancement mode pHEMTs are used as power switches, and the gate driver is integrated along with the low and high side power devices on the same chip. The gate driver is made of E/D pHEMT inverter buffer stages. The power IC is then flip chip assembled on a 5x5mm2 laminate on which the passives are also integrated. The IC is capable of switching at 200MHz. At

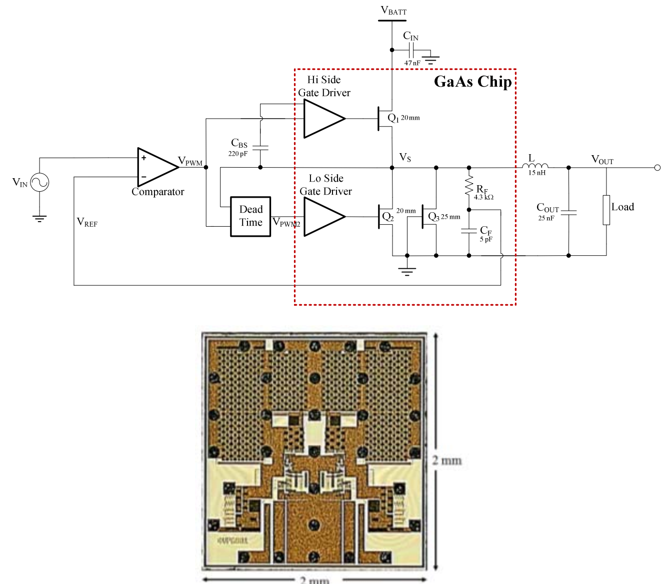


Figure 11: Top level schematic and die photo of the GaAs buck converter IC

these frequencies, air core inductors can be used to reduce the overall module footprint without a major efficiency penalty. A 0402 size 15 nH wire-wound surface mount inductor is used for the design. The open loop power efficiency of the circuit for various voltage conversion ratios for an input voltage of 4.5V and a switching frequency of 100MHz is shown in Fig.12. When switched at 100 MHz, the peak measured efficiency of the converter at a steady state output voltage of 3.375 V is 88% for 34dBm power output. The converter can

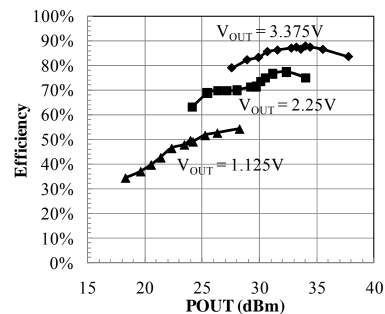


Figure 12: Measured power efficiency of the converter as a function of output power at 75 %, 50 % and 25 % voltage conversion ratios.

operate at up to 37 dBm output power for at the peak voltage. The example demonstrates that integrated power ICs in GaAs are a promising technology for <50V power ICs, especially where high switching frequencies are mandated.

Since there are separate papers that focus specifically on SiC and GaN power devices in this special issue, we will only present selectively the highlights of recent advances.

SiC

The progressive increase in the diameter of 4H-SiC ingots over the last decade has resulted in the recent announcement of 200mm diameter wafers [21]. While heavily doped n+ and semi-insulating substrates are available commercially, lightly doped n-type, long lifetime substrates, which are desirable for ultrahigh power devices, are not. A novel way to create an n- substrate by growing a thick, lightly-doped epitaxial layer on an n+ substrate and then complete and selectively removing the substrate, has been demonstrated on 100mm diameter 4H-SiC wafers [22]. These n- substrates are very useful for the realization of uni- and bi-directional ultrahigh voltage, vertical power devices.

Despite more than two decades of research in SiC MOS optimization, the electrical properties of the SiO_2/4H-SiC interface are still inferior to those of the SiO_2/Si interface in state-of-art Si MOSFETs [23]. The biggest challenge for SiC MOS is improvement of the inversion channel electron mobility. Post oxidation/deposition anneal in NO and/or N_2O at 1100-1300°C is the standard procedure to increase the field-effect mobility. Although this procedure greatly reduces the conventional slower interface traps, it has also been shown to generate other faster interface traps [24,25]. Fig. 13 shows the interface state density of SiO_2/4H-SiC capacitors after high-temperature NO annealing [25]. It should be noted that in addition to the effect on interface states, NO annealing also renders the inversion electron mobility, as measured by MOS-gated Hall structures, mediocre (~50cm^2/V-s), due to interface scattering [26]. To estimate the maximum channel mobility possible in SiC, an extension of the silicon inversion model has been made and a value of only about 200cm^2/V-s is projected [27]. The reason for this low mobility as compared to Si is the larger transverse electric field across the gate oxide necessitated by the large band-bending from the 3X larger bandgap of SiC as compared to Si.

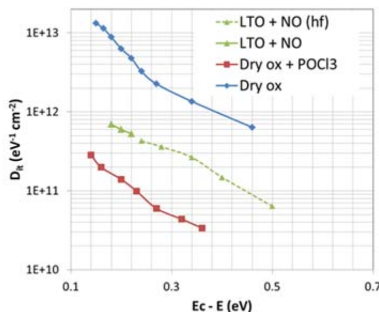


Fig.13 Interface state density of SiO_2/4H-SiC capacitor after high-temperature NO anneal [25].

Another very important parameter in the performance of SiC power MOS devices is the gate oxide reliability [28,29]. One recent, promising reliability report is shown in Fig. 14, a Weibull plot of the percentage of gate oxide failures vs. stress time [29]. Due to the asymmetric conduction vs. valence band offsets, the reliability data under PBTI vs. NBTI stressing are different, with the former being more difficult to achieve reliability (Fig. 15). Over the past few years, state-of-the-art SiC gate oxide quality has been steadily improving as evidenced by Fig. 14. Nevertheless, several irregularities observed in the latest data set suggest that SiC gate oxide reliability has not yet matched that of Si MOS.

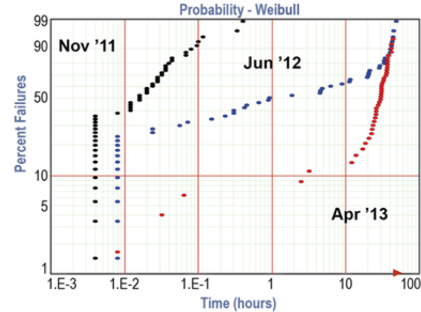
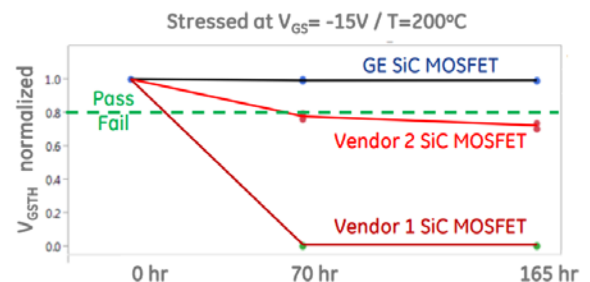


Fig. 14 Weibull plot of the percentage of failures vs. stress time [29].

At present, the focus of SiC power MOSFET commercialization has been the 900-1200V range. Due to the inferior SiC inversion channel mobility, a large percentage (50% or more) of the total device specific on-resistance is the channel specific on-resistance. Fig.16 clearly demonstrates the importance of the channel mobility to the performance of 1kV SiC power MOSFETs [30]. The channel density can be increased by reducing the MOSFET cell pitch but the lower limit of the cell pitch is determined by the JFET width and



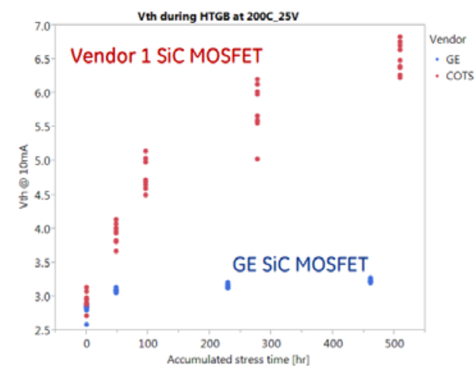


Fig. 15 Threshold voltage shift under PBTI vs. NBTI stressing conditions [29].

on-resistance for planar vertical DMOSFETs.

As previously mentioned, for blocking voltages above 5kV, the IGBT is preferred over the power MOSFET for SiC. Over the last five years, numerous SiC IGBTs have been reported with increasing blocking voltages and improved on-state performance, with the highest reported breakdown voltage reaching 27kV [31-35]. Nevertheless, the recombination lifetimes in the drift layer are still too short for adequate conductivity modulation, so the forward drop is still higher than optimum. Recently, using the lightly doped n-type free-standing wafer technology described previously, high voltage bi-directional n-channel 4H-SiC IGBTs have been experimentally demonstrated for the first time [36]. These transistors utilize dual-sided wafer processing during device fabrication and necessitate identical MOS processing for both surfaces. With a collector current density of 50A/cm^2, the Si-face forward voltage (V_F) was 9.7V at room temperature and 11.5V at 150°C; V_F was even higher for the C-face. However, the 11.5V V_F compares favorably to the 27V V_F for 15kV 4H-SiC power MOSFETs previously reported [37]. In Fig.17, the forward I-V characteristics of a high voltage SiC BD-IGBT at 25 and 150°C are shown, together with the specific on-resistance of the drift layer [37]. In addition, the small positive temperature coefficient for V_F is attractive for stable current sharing among devices connected in parallel. While the threshold voltages of Si- and C-face channels need to be better matched and breakdown voltage further enhanced, the differential specific on-resistance in the on-state has been found to be more than 3 times lower than the unipolar limit of the drift layer, indicating sufficiently long minority carrier diffusion length and some degree of conductivity modulation. The advantages of a bi-directional transistor switch include reduced device component count and module cost as well as higher reliability. Hence bi-directional transistors are a promising trend in SiC power transistor development.

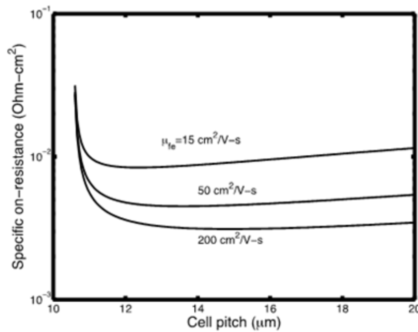


Fig. 16 The effect of MOS channel mobility on the performance of 1kV SiC power MOSFETs [30].

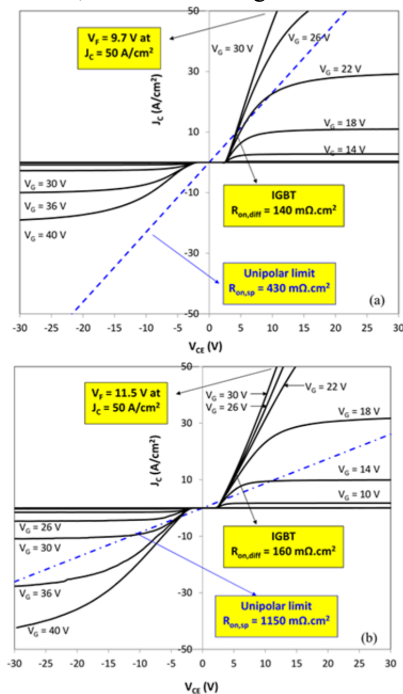


Fig. 17   Forward I-V characteristics of a high voltage SiC BD-IGBT, together with the specific on-resistance of the drift layer at room temperature and 150C [36].

GaN

Several lateral AlGaN/GaN power HEMTs that have been explored for power electronics applications [38]. Among these, the MOS Channel-HEMT (MOSC-HEMT), in which the AlGaN layer is completely etched from a MOS channel, appears to be easiest way to achieve the normally-off operation that is required for power switching. However, the MOS inversion channel electron mobility is about an order of magnitude lower than that of the 2DEG in a heterojunction channel [39]. Nevertheless, the on-state performance of a MOS channel device can be made to approach that of a conventional HEMT if the channel length is reduced to deep micron dimensions [40]. In addition, with the availability of high-quality GaN substrates, vertical power transistors, such as the CAVET [43], are also possible [41-45]. Vertical DMOS-type MOSFETs have been impeded due to the difficulties in activating implanted acceptors in GaN.

Interestingly, the specific on-state resistance dependence on the breakdown voltage is different for lateral RESURF power devices when compared to that of vertical power devices. For lateral RESURF devices, it can be shown that in the ideal case, when the device drift layer resistance dominates, $R_{on,sp} \propto (BV)^n$, where n ranges from 1 to 1.3, dependent on the doping profile, carrier mobility, critical field dependence on doping, and substrate character (junction vs. SOI) [46-47]. This dependence is substantially different from the n value of 2.4 to 2.6 for 1D vertical devices and the commonly derived value of 2 for lateral devices deduced from the linear dependence of both BV and on-resistance on drift length. However, for lateral GaN HEMTs on silicon, which can be viewed as functionally equivalent to SOI RESURF structures, the 2DEG mobility and the breakdown field do not depend on the drift layer doping, and the ultimate n value can approach unity when the lateral space charge (polarization or dopant charge) concentration profile is non-uniform [47]. We have shown the polarization charge concentration at the AlGaN/GaN

heterojunction can be modified by varying the GaN cap thickess [48]. Experimentally, the specific on-resistance of lateral GaN HEMT vs. breakdown voltage is shown in Fig. 18. An empirical n value of ~1.3 has been extracted from the reported data for BV ranges from 30 to 1kV.

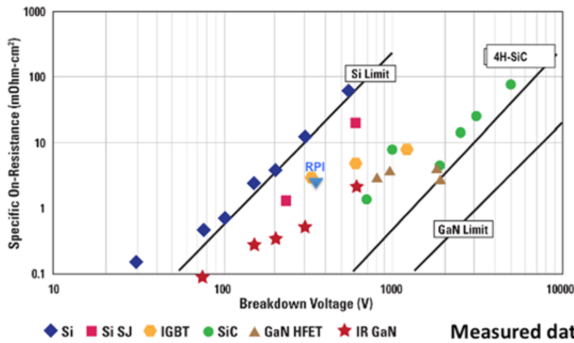


Fig. 18 Specific on-resistance vs. breakdown voltage for lateral GaN power HEMTs vs. Si and SiC vertical power MSOFETs [49]

One of us has compared the on-state performance of Si IGBTs and superjunction UMOSFETs with SiC and GaN vertical and lateral power transistors for breakdown voltages ranging from 600V to 15kV [50,51]. Fig. 19 shows the comparison of the forward J-V characteristics for the 600V case [49]. While SiC and GaN devices have clearly lower on-state power losses, cost-effectiveness is an issue. When blocking voltage increases, the Si superjunction MOSFET and the lateral GaN power HEMT are no longer competitive or practical. Above 6kV, the SiC IGBT becomes superior over the SiC power MOSFET. Over 10kV, unless extreme bandgap power devices are considered, the SiC IGBT is the only viable choice, as shown in Fig. 20 [50].

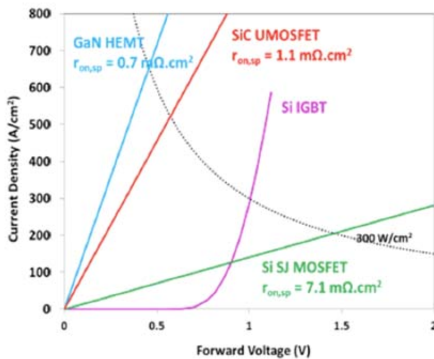


Fig. 19 Comparison of on-state performance of 600V Si vs. SiC and GaN power transistors [50].

The main advantage of the lateral GaN power HEMTs is its ability to integrate them with optoelectronic devices, yielding high-performance and cost-effective power electronic or photonic systems/subsystems. Demonstrated examples of these include a GaN power converter IC on Si [52], an ultracompact GaN 3x3 power converter IC with drive-by-microwave technology (DBM) [53], and an integrated GaN LED/lateral MOSC-HEMT pair [54,55]. A

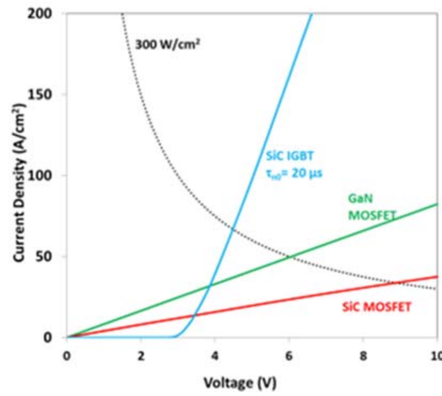
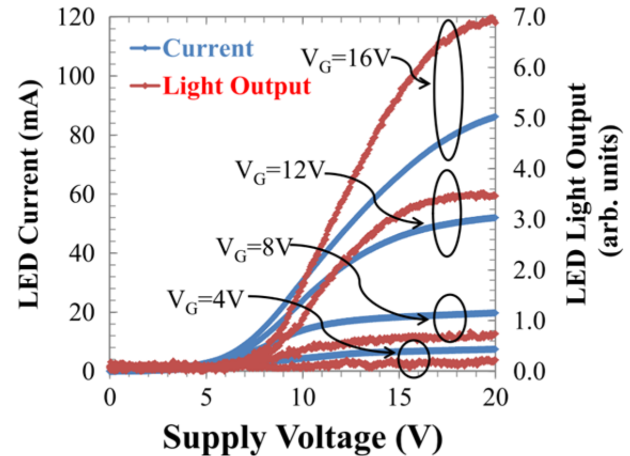


Fig. 20 Comparison of on-state performance of 15V Si vs. SiC and GaN power transistors [51].

100W, 3 phase GaN power converter IC has been implemented with six normally-off power transistors, isolated with Fe implantation, operating in the bi-directional conduction mode without external fast recovery diodes, and achieving an efficiency as high as 93% [52]. An innovative 3 phase AC-AC matrix converter IC has been demonstrated with nine RF-triggered GaN gate injection transistors (GITs) operating as bidirectional power switches and co-integrated with RF couplers and novel isolated dividing couplers. DBM technology realizes a low power, simple gate drive



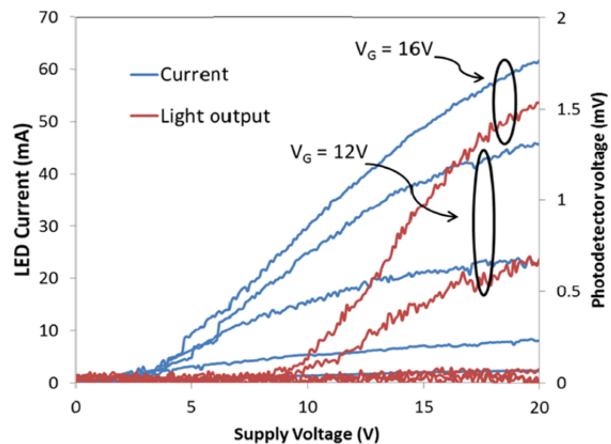


Fig. 21 LED current and light output intensity vs supply voltage, plotted as a function of the HEMT gate voltage [55,56].

capability to provide isolated gate signals and eliminates photo-couplers and isolated power supplies [52]. There are at least 3 ways of implementing a GaN optoelectronic IC [56]. These are: selective epi removal, selective epi growth and 3D integration with wafer bonding. The first GaN monolithic optoelectronic integration was demonstrated recently by integrated fabrication of a vertical InGaN/GaN MQW LED in series with a lateral AlGaN/GaN power HEMT using the selective epi removal approach [54,55]. Operation up to 225°C was also demonstrated, as shown in Fig. 21 [55], showing the superior potential at high switching frequencies and elevated temperature of integrated GaN FETs over conventional silicon LED driver circuits.

GaN Power IC

Power electronics systems with GaN power ICs show potential to replace the discrete silicon IGBT / MOSFET base systems in 2-3 kW class motor drive inverters and ICT power supplies. Based on a simple calculation, a 36mm^2 600V GaN motor drive power IC chip can switch 11A, or 2-3kW, sufficient for most appliance and home power supply applications ([57]). GaN output power density per chip area is 5 times high than silicon based single chip motor drives for the same cooling conditions.

Table 8 shows GaN power IC technology requirements for a variety of integration levels ([57]). One potential difficulty is realization of analog circuits such as voltage reference functions for output voltage control, since p-type transistors are required.

Integration of Si gate drive circuitry with GaN power transistors shows promise to reduce drive loss and switching loss by producing sharp PWM drive signals to the GaN transistor from standard digital PWM inputs while simultaneously adding more noise immunity in gate drive circuits [58].

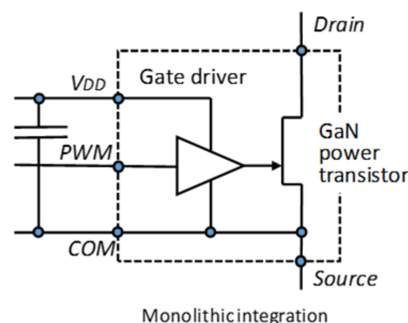


Fig. 22 Monolithic integration of gate driver and power transistor on GaN[57].

Ga_2O_3

For unipolar power device applications, Ga_2O_3 has some attractive attributes: a breakdown electric field of 7-8MV/cm (due to a bandgap larger than 4.5 eV) [59-63], good controllability of n-type doping in the wide range of n=10^{15}~10^{19} cm^{-3} through Si or Sn doping [64-66], and tunable resistivity spanning 10^{-3}~10^{12} Ω·cm.

The performance of power devices is commonly correlated with basic material properties of semiconductors through Baliga's Figure of Merit (BM). The estimated BM of 2,000~3,400 for Ga_2O_3 is several times larger than those for SiC and GaN. This value provides strong motivation for the development of Ga_2O_3 power devices.

Industrialization and commercialization efforts for SiC and GaN devices have been adversely affected by a lack of affordable native substrates. In contrast, Ga_2O_3 wafers can be fabricated in large volumes from bulk single crystals synthesized by melt-growth techniques such as float-zone [64,67], Czochralski [68,69], vertical Bridgman [70], and edge-defined film-fed growth (EFG) [71,72]. The availability

	Power Device	Gate drive / signal isolation	Analog	CMOS like logic
Feature size	<1 micron	<0.5 micron +high gm	0.35-1 micron	<0.25 micron
Number of metal layers	1-2 layers	2 layers	>2 layers	>> 2 layers
Frequency	10 kHz for motor drive ~10 MHz for power supply >10 MHz for class E, F	100 kHz 100 MHz >100 MHz	100 kHz 100 MHz >100 MHz	(>1GHz)
Voltage	400V-1200V for motor drive and AC/DC, DC/AC 30-200V for DC/DC	5 V for gate drive + high voltage signal isolation	3.3 V – 5 V	<2.5V
Power loss	-	1-5% of power device	1% of power device	1-5% of power device
Uniformity across wafer/ Wafer bending	Depends on wafer handling yield	Wafer bending < 10 micron	Severe uniformity required	Severe uniformity required
Complementary transistor	Not required	Better to have	Required	Indispensable
Compact model	Required	Required	Indispensable	Indispensable
Technology barrier	-	-	high	Very high

Table 8 GaN power IC technology requirements [57]

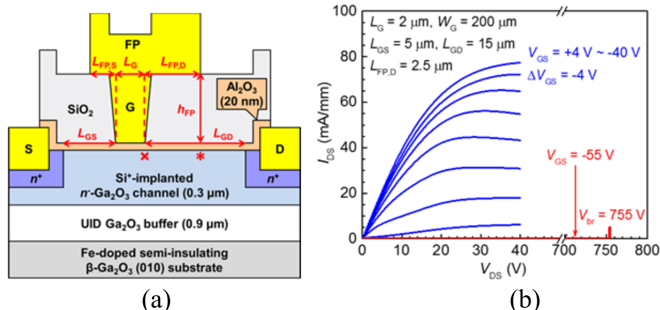
of melt-grown Ga_2O_3 bulk single crystals leads directly to a significant reduction in the production cost of Ga_2O_3 wafers and thus market prices of commercial products. Figure 23 shows a photograph of a 4-inch-diameter single-crystal Ga_2O_3 wafer produced from an EFG-grown bulk crystal. EFG Ga_2O_3 wafers have already demonstrated very high crystal quality with a dislocation density on the order of 10^3~10^4 cm^{-2}. The good material workability of Ga_2O_3 is another important feature for economical mass wafer production.

Fig. 23 Photograph of 4”-diameter Ga2O3 wafer.

Two main drawbacks of Ga_2O_3 are often noted in power device contexts, a lack of p-type material and poor thermal conductivity. There has been no report of successful p-type doping or effective hole conduction in Ga_2O_3. Furthermore, self-trapping of holes in the bulk, which prohibits effective p-type conductivity due to the resultant low mobility, has been predicted by first-principles calculations of the Ga_2O_3 band structure [73]. The issue of low thermal conductivity is the most serious potential weakness for Ga_2O_3 power devices. Experimental thermal conductivity values for Ga_2O_3, which fall in the range of 0.1~0.3 W/cm·K at room temperature, are one or two orders of magnitude smaller than those of other wide bandgap semiconductors [74].

Field-Effect Transistors (FETs)

In 2012, Ga_2O_3 metal-semiconductor field-effect transistors (MESFETs) became the first reported Ga_2O_3 transistors [63]. A Sn-doped n-type Ga_2O_3 channel layer was grown by ozone molecular-beam epitaxy (MBE). In this first demonstration, the MESFETs showed good device characteristics including a sharp drain current (I_d) pinch-off, a three-terminal off-state breakdown voltage (BV) of 250 V, and an Id on/off ratio of about four orders of magnitude at a drain voltage (V_d) of 40 V. However, the MESFETs suffered from high contact resistance at the source and drain electrodes and a significant leakage current through the unpassivated Ga_2O_3 surface.



(a) (b)

Fig. 24 (a) Schematic cross section and (b) DC output characteristics of Ga_2O_3 FP-MOSFET.

A schematic cross section of the state-of-the-art Ga_2O_3 field-plated metal-oxide-semiconductor FET (FP-MOSFET) structure is illustrated in Fig. 24(a) [75]. New process technologies developed to solve the MESFET’s deficiencies were employed to fabricate the FP-MOSFETs. Good ohmic contacts on n-Ga_2O_3 were fabricated using Si-ion implantation doping and Ti-based metal stacks [76]. A high activation ratio of implanted Si was attained by post-implantation annealing at relatively low temperatures of 900~1000°C, which also avoided all but negligible diffusion of the implanted atoms. A specific contact resistance of less than 1×10^{-5} $\Omega\cdot cm^2$ was reproducibly obtained for the high Si implantation doped (5×10^{19} cm^{-3}) source/drain regions. MBE-grown unintentionally-doped Ga_2O_3 provided effective inter device isolation with a high resistivity of 10^8~10^9 $\Omega\cdot$cm, and MOSFET channels were defined by selective-area Si-ion implants with a 0.3-μm-deep box profile and a plateau concentration of 3×10^{17} cm^{-3}. A reduction in leakage current by more than six orders of magnitude was achieved using gate and passivation dielectric films.

Figure 24(b) illustrates the room-temperature DC output characteristics of the Ga_2O_3 FP-MOSFET. The Ga_2O_3 FP-MOSFET showed a room-temperature maximum Id of 78 mA/mm at a gate voltage (Vg) of +4 V. Successful FP engineering resulted in an off-state BV exceeding 750 V, corresponding to an improvement of more than 80% over the value for the Ga_2O_3 MOSFETs without a field plate [77,78]. Furthermore, effective surface passivation and high Ga_2O_3 material quality contributed to the absence of DC-RF dispersion of drain current. Stable operation under thermal stress up to at least 300°C has also been confirmed.

Recently, Green et al. reported Ga_2O_3 MOSFETs with a 0.6 μm gate-to-drain distance and a 230 V breakdown voltage, indicating average and maximum electric fields of 3.8 MV/cm and 5.3 MV/cm, respectively [79]. These experimental values are larger than the theoretical limits of SiC and GaN and thus illustrate exploitation of the inherent material advantage of Ga_2O_3.

Schottky Barrier Diodes (SBDs)

In early years, SBDs lagged behind FETs in technological progress due mainly to a lack of suitable epitaxial growth techniques for thick n--Ga_2O_3 layers. Recently, homoepitaxial high-speed growth of high-quality Ga_2O_3 thin films has been achieved by halide vapor phase epitaxy (HVPE) [80,81]. In an HVPE reactor, Ga and O source gases are separately introduced into a growth zone, and $SiCl_4$ is simultaneously supplied during the growth for n-type doping. The growth rate can be increased up to about 25 μm/h without compromising material quality. UID Ga_2O_3 thin films grown by HVPE possess excellent electrical properties including a residual net carrier concentration of less than 1×10^{13} cm^{-3}. Typical values of room-temperature electron mobility in HVPE-grown Si-doped Ga_2O_3 thin films are 100~150 $cm^2/V\cdot s$ for $n=10^{15}$~10^{17} cm^{-3}. The intrinsic donor activation energy in HVPE-grown Si-doped Ga_2O_3 films is estimated to be approximately 50 meV from temperature-dependent Hall

measurements; therefore, Si is a shallow donor and fully activated at room temperature.

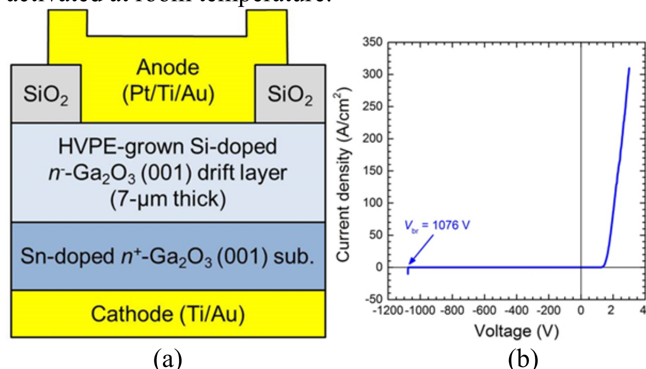


Fig. 25 (a) Cross-sectional schematic illustration and (b) current density–voltage (J–V) characteristics of Ga_2O_3 FP-SBD.

A record BV for Ga_2O_3 power devices of over 1 kV was reported for Pt/Ga_2O_3 FP-SBDs fabricated on n--Ga_2O_3 drift layers grown on n+-Ga_2O_3 (001) substrates by HVPE [82]. Figures 25(a) and (b) show a cross-sectional schematic illustration and room-temperature current density–voltage (J–V) characteristics of the FP-SBD, respectively. The specific on-state resistance and ideality factor of the FP-SBD were estimated to be 5.1 mΩ·cm^2 and 1.05, respectively. Successful FP engineering resulted in a 1076V breakdown voltage, approximately two times larger than SBDs without field plates [83].

Forward current conduction in typical Ga_2O_3 SBDs with HVPE-grown drift layers was governed by thermionic emission with a near-unity ideality factor, and, as expected for wide bandgap semiconductor SBDs, reverse leakage current agreed well with the thermionic field emission model. These results indicate that the Pt/Ga_2O_3 interface formed an excellent Schottky contact [84].

Diamond

The previous decade has seen significant advances in diamond rectifier and FET technology. In 2004, 2.5kV diamond Schottly diodes, without termination, were demonstrated on 18μm thick intrinsic drift epi layers on p+ substrates, but at a forward voltage of 10V the on-state current density reached only 1A/cm^2 at room temperature [85]. Next, using a smart-cut thin film transfer process, thin diamond epi layers were mounted on molybdenum substrates and high voltage vertical and lateral rectifier structures were fabricated and characterized [86,87]. Vertical Schottky diodes, with proton implanted junction termination extensions achieved breakdown voltages as high as 3.7kV on 20μm thick, extrinsic boron-doped (10^{14}-5×10^{15} cm^{-3}) epi layers but the forward current densities were low (0.6 A/cm^2 at a forward voltage of 20V at 290°C) [87]. More recently [88,89], vertical and quasi-vertical high voltage diamond Schottky diodes were reported to have breakdown voltages from 200 to 1800V and forward current densities of 100-1800A/cm^2 at forward drops 7V or lower.

Notably, a forward current density of J_F of 4000A/cm^2 at V_F of 6V at 25°C (and 400A/cm^2 at V_F of 2V at 300°C) was achieved by employing a novel diamond Schottky pin diode structure (Fig. 26), and a high rectification ratio (~10^{10}) was reported [89]. However, this device relied on a lightly doped n-type blocking layer which was designed to remain fully depleted even during forward conduction. Although the estimated breakdown field was a respectable 10MV/cm, the blocking layer was only ~70nm thick resulting

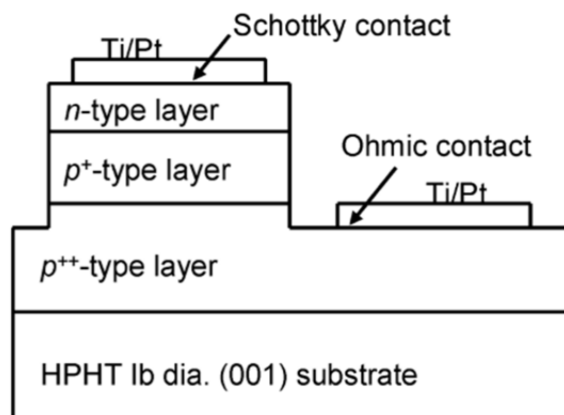


Fig 26: Novel depleted diamond rectifier [89]

in a blocking voltage of only ~70V. Achieving a high breakdown voltage by scaling up the thickness of the lightly doped blocking layer without altering the novel, forward bias depletion effect is non-trivial. Recent reports [90,91] to improve the breakdown voltage by increasing the p-type drift layer thickness result in blocking voltage of 500 to over 750V. However, the forward drop is substantially higher, due to the serial voltage drops of the Schottky and np junctions.

Diamond high voltage p-channel FETs

1. P-channel high voltage FET

The extreme or ultrawide bandgap of diamond allows superior high-temperature and high-voltage switching performance potentials. Diamond field effect transistors (FETs) are limited to p-channel FETs, since n-type regions are highly resistive not suitable for MOS channel fabrication with present technology. However, bulk hole mobility of diamond is more than 1000 cm^{2}V^{-1}sec^{-1}, the highest of any wide band gap semiconductor. The lowest p- type resistivity achieved is 10^{-3} Ω–cm, as low as that of Si. There are two ways to form p-type channel. Boron doping produces bulk acceptors, and hydrogen-terminated (C-H) surfaces result in a surface 2 dimensional hole gas (2DHG) . In high voltage applications, metal semiconductor FETs [93] and junction FETs [94] have been demonstrated using boron-doped channels. Metal oxide semiconductor FETs (MOSFETs) using 2 dimensional hole gas (2DHG) have also been demonstrated and exhibit high blocking voltages [95-97]. For the 2DHG devices, the gate insulator and passivation layers of the MOSFETs fabricated by ALD of Al_2O_3, which is also required for formation of the 2DHG on the C-H diamond surface (Fig.27) [95].

2. Off-state: Breakdown voltage

In the off-state, breakdown voltage (*BV*) as a function of gate-drain length (L_{GD}) shows high-voltage durability for

planar FETs. Blocking properties are often evaluated using the BV/L_{GD} ratio, with a 1MV/cm ratio used as a respectable benchmark. The BV/L_{GD} relationship of diamond MOSFETs with 2DHG and MESFET and JFET with boron doped channel are shown in Fig.27, along with the benchmark line. In a JFET with a small L_{GD} of 1-2 μm, *BV* was 608 V suggesting maximum electric field (E_C) of 6 MV/cm [94]. In the MESFET above with L_{GD} = 20 μm, *BV* over 1000 V was obtained for the first time [94] in diamond (Fig. 27 closed stars). The maximum *BV* reported for a MESFET is 1500 V where E_C was estimated to be ~2 MV/cm [94]. At an L_{GD} of 2-10 μm for MOSFETs with 200nm thick Al_2O_3 on C-H diamond, the BV/L_{GD} is on the 1 MV/cm line up to a *BV*~1000 V [97]. At L_{GD} >10 μm, *BV* exceeds 1000 V and reaches 1646 V at L_{GD} of 22μm (Fig. 27 open squares) [98], though the BV/L_{GD} is less than 1. With a 400nm Al_2O_3 on drift layer, BV/L_{GD} stays at 1MV/cm above 1000 V and *BV* reaches 1700 V at L_{GD} of 16 μm (Fig. 27 closed circles) [99]. Normally-off MOSFETs have been fabricated by partially oxidizing the channel under the Al_2O_3 gate oxide to achieve threshold voltages V_{th} of -3~-5V. Here, *BV* reaches 2000V at L_{GD} of

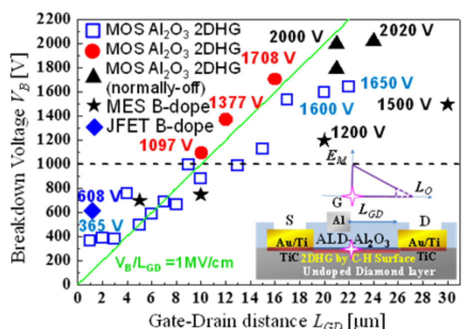


Fig. 27 Maximum breakdown voltages VB of C-H diamond MOSFETs as a function of gate-drain length L_{GD}. Epitaxial C-H diamond FETs covered by ALD Al_2O_3 films in 200nm thick on channel as gate oxide and in 200 nm (open squares) and 400 nm (closed circles) on drift layer. Partially oxidized channel under 200 nm Al_2O_3 gate oxide with 400 nm Al_2O_3 passivation on drift layer (closed triangles) showing normally-off mode. Diamond MESFET (closed stars) and JFET (closed rhomboid).on boron doped channel and drift layer

21 μm (Fig.27 closed triangles).

Electric field distribution at the MOS diamond surface is schematically shown in Fig. 27, where the E_C of the diamond surface is located near the gate edge (cross in Fig.27). The electric field distributes in an oblique line indicating that E_C is much higher than BV/L_{GD}. Its slope is governed by negative or positive surface charge density of diamond in the range of 10^{10}-10^{13} cm^{-2}. L_{GD} dependence of *BV* in Fig.27 might originate from a relatively small surface charge density (<10^{12} cm^{-2}) where L_O (length to the extrapolated "zero field point") is larger than L_{GD}.

The *BV* of C-H diamond lateral MOSFETs without field plate structures becomes comparable to those of other wide bandgap semiconductor planar FETs with field plate such as SiC (BV/L_{GD}=0.8 MV/cm), AlGaN/GaN (1.0 MV/cm) and AlGaN/ AlGaN (1.7 MV/cm) (Table 1). Diamond can achieve BV/L_{GD} >3 MV/cm, because *BV* of 365 V and 608 V were achieved at L_{GD} of 1-2 μm in MOSFET [96] and JFET [94], respectively.

3. On-state: drain current density

At on-state, the drain current density is an important parameter. Drain current density, normalized by gate width reaches 100mA/mm in the C-H MOSFET with a *BV* of ~1700V [97], is higher than those of the diamond JFET and the MESFET with a boron-doped channel and drift layer (1mA/mm)[93,94] with *BV* of 608 V and 1500 V, respectively [93] . The low drain current is caused by high activation energy of boron as an acceptor (0.37 eV). The drain current density becomes comparable to those of SiC planar MOSFETs (90mA/mm), AlGaN/GaN (~300mA/mm) and AlGaN/ AlGaN (~200mA/mm). Between 100-600K, C-H diamond MOSFETs can have almost constant FET performance, indicating a wide temperature range for power device applications.

V. Technical Obstacles and Commercialization Challenges

Key Technical Challenges

There are two kinds of technical challenge facing these new semiconductors. The first kind are the challenges associated with reaching the technical maturity necessary to exploit the full potential of the novel WBG/EBG material systems. The second kind are the challenges associated with directly competing against existing silicon power devices.

While the technological advancement of wide and extreme bandgap semiconductors have progressed rapidly over the last decade, there are still major technical challenges in their further development and commercialization. These are summarized below for each semiconductor considered.

GaAs

GaAs has more manufacturing infrastructures than any of the other semiconductors considered here. However, compared to silicon nanometer CMOS, it is lacking in a consistent scaling technology driven by a well-planned roadmap generated by industrial consortium. In addition, monolithic integration with silicon digital circuitries is not possible. Consequently, despite its potential performance shown here for high-frequency dc-dc converters, it is difficult to commercialize GaAs devices and compete directly with silicon at present.

SiC

The announcement of the demonstration of 200mm diameter 4H-SiC wafers is definitely good news but it remains to be seen how quickly large volume production and cost reduction advance. Minority carrier lifetimes must be further improved (> 20μs) with increasing blocking voltage to allow good conductivity modulation in bipolar device drift regions.

MOS process technologies in 4H-SiC have significantly improved but are not yet on par with state-of-art Si MOS, particularly in terms of reproducibility, reliability and robustness for high-yield manufacturing.

GaN

Lateral AlGaN/GaN HEMTs on silicon substrates have been commercialized but their large-scale cost-effective manufacturability and robustness has not yet been proven. Vertical power GaN transistors are preferred for medium to high power applications, but native GaN substrates are generally needed. While GaN substrate development has progressed rapidly, the maximum wafer diameter is still only 100mm and its surface and bulk material properties, as well as defect densities, have not been ascertained to have sufficiently high quality. Consequently, the development and commercialization of vertical GaN power transistors are limited by cost-effective substrate availability. In addition, because of its direct bandgap, only unipolar GaN transistors and diodes are feasible. Reliability of GaN MOS devices, assumed similar to 4H-SiC MOS, still needs to be systematically evaluated. Further, at present, unlike SiC, there is no consensus on which power FET structures are best for commercialization.

Ga_2O_3

Research and development (R&D) on Ga_2O_3 power devices are still at the and early stage. Many fundamental technologies for this material system must still be developed before realization of advanced vertical transistors and diodes. Further improvements in bulk growth, epitaxial thin film growth, and device process technologies are required. Unsolved technical challenges related to the material properties of Ga_2O_3 include the realization of *p*-type conductivity and the management of heat dissipation to overcome poor thermal conductivity. Development of normally-off FETs and high-voltage SBDs requires high-quality dielectric deposition techniques. To attack the many R&D challenges and solve the many material systems issues, a large number of researchers and engineers working on Ga_2O_3-related materials and devices will be required.

VI. CONCLUSION

We have comparatively reviewed GaAs, SiC, GaN, Ga_2O_3 and diamond transistors for power switching applications, in terms of Figure of Merit, power electronic applications, process technologies, selective experimental device demosntrations, and key technical challenges for ultimate performance realization and widespread commercialization. We expect GaAs and these wide and extreme bandgap semiconductors to significantly impact the energy efficiency power electronics systems over the next few decades.

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