

Mutual Inductance Measurement for Power Device Package Using Time Domain Reflectometry

Kazunori Hasegawa

Department of Biological Functions Engineering
Kyushu Institute of Technology
Kitakyushu, Fukuoka, Japan

Keiji Wada

Department of Electrical and Electronic Engineering
Tokyo Metropolitan University
Hachioji, Tokyo, Japan

Ichiro Omura

Department of Electrical and Electronic Engineering
Kyushu Institute of Technology
Kitakyushu, Fukuoka, Japan

Abstract— Stray inductance inside power device package will be a constraint on improvement of power density as well as switching frequency in power converters because the converters will suffer from electromagnetic interference (EMI)-related problems. This paper proposes a measurement method of mutual inductance for power device packages using time domain reflectometry. The method is characterized by introducing four-terminal measurement that distinguishes self and mutual inductances among collector, emitter, and gate terminals. A measurement fixture for a discrete IGBT is designed, constructed, and tested to ensure repeatability of the proposed method. Experimental results verifies the viability of the proposed method.

Keywords—Time domain reflectometry, stray inductance, power device package, IGBT.

I. INTRODUCTION

Attention has been paid to measurement of parasitic parameters in power electronic converters as well as in power semiconductor devices [1-7]. The parasitic parameters will be a constraint on improvement of power density as well as switching characteristics in the converters because the converters will suffer from electromagnetic interference (EMI)-related problems. Recent power converters are employing leading-edge semiconductor devices such as silicon carbide (SiC) and gallium nitride (GaN) devices to achieve lower power loss and higher switching frequency [8]. In addition, existing silicon devices including insulated-gate bipolar transistor (IGBT) have been being developed to have higher current capability [9].

Many researchers have been addressed measurement methods for stray inductance inside package of power devices because the inductance may have an influence to switching characteristics such as switching loss and overvoltage [1-7]. However, the methods can measure total inductance between each terminal, so that they could not separate self and mutual inductances inside the package. Reference [1] has pointed out that not only self inductances but also mutual inductances among drain, source, and gate (collector, emitter, and gate) terminals affect switching characteristics in a metal-oxide-

semiconductor field-effect transistor (MOSFET). Therefore, both self and mutual inductance measurement procedure and those separation methods should be discussed for the package of power semiconductor devices.

In recent years, time domain reflectometry (TDR) has emerged as an effective technique for measuring parasitic parameters in power electronic converters as well as in power devices [2-6]. For example, reference [2] has addressed stray inductance measurement for an IGBT module. Reference [6] has proposed a TDR measurement method for voltage-dependent

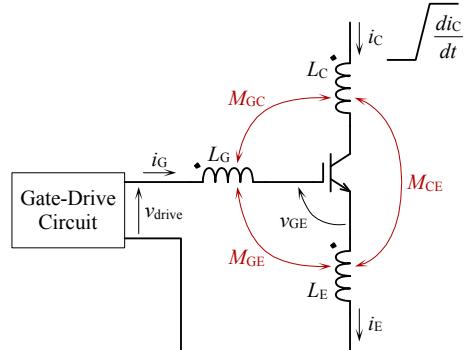


Fig. 1 Effect of mutual inductances to the gate-emitter voltage v_{GE} .

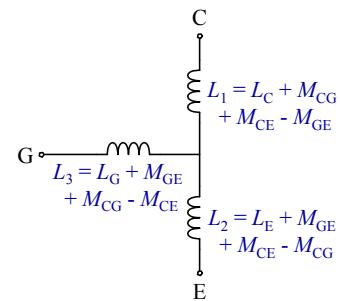


Fig. 2 Equivalent circuit of self and mutual inductances among collector, emitter, and gate terminals, with star configuration

capacitances of power devices and passive component like ceramic capacitors.

This paper proposes a measurement method of mutual inductance for power device packages using TDR. The method is characterized by introducing the neutral point of power device chip inside TO-247 package, which allows to distinguish all the self and mutual inductances among collector, emitter, and gate terminals of an IGBT or MOSFET. This paper makes theoretical discussion for the measurement, which reveals that it is impossible to extract mutual inductances only from three terminals, collector, emitter, and gate.

II. HOW TO SEPARATE MUTUAL INDUCTANCE

A. Why is mutual inductance measurement necessary?

Fig. 1 shows relation between package inductances and the gate-emitter voltage v_{GE} , which is given by

$$\begin{aligned} v_{GE} &= v_{drive} - v_{LG} - v_{LE} \\ &= v_{drive} - L_G \frac{di_G}{dt} - (L_E + M_{GC} + M_{GE}) \frac{di_C}{dt} \end{aligned} \quad (1)$$

where i_E is assumed to equal i_C , and v_{LG} and v_{LE} stand for voltages across L_G and L_E , respectively. v_{GE} is a function of the collector current via M_{GC} and M_{GE} , so that the mutual inductances affect switching speed of the IGBT [1]. On the other hand, a negative M_{CE} contributes to reducing surge voltage between the collector and emitter terminals.

B. Four-terminal measurement

Fig. 2 shows an equivalent circuit of stray inductances in the IGBT, where the three mutual inductances and the three self inductances are combined as three inductances L_1 , L_2 , and L_3 with star configuration. The input, output, and reverse transfer capacitances of the IGBT are disregarded because they behave as a short circuit in a high-frequency range of TDR measurement. This equivalent circuit implies that one can identify only L_1 , L_2 , and L_3 using collector, emitter, and gate terminals, but cannot distinguish the mutual inductances from L_1 , L_2 , and L_3 . Hence, the three-terminal measurement cannot uniquely specify the three self inductances and three mutual inductances in the IGBT.

Four-terminal measurement including the neutral point N among the collector, emitter, and gate terminals identifies all the self and mutual inductances. Self inductances L_C , L_G , and L_E can be obtained from measurement between the neutral point N and

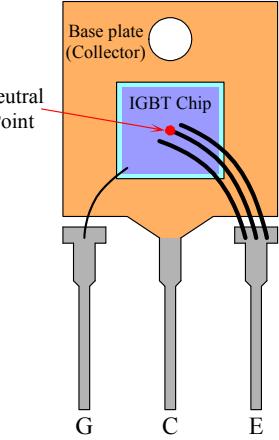


Fig. 3 Structure of TO-247 package

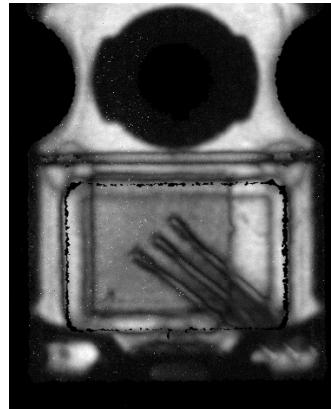


Fig. 4 Internal image of the DUT by scanning acoustic tomography

the collector, gate, and emitter terminals, respectively. Mutual inductances can be calculated by self inductance of each terminal and inductance between two of three terminals (collector, gate, emitter) as follows:

$$M_{GE} = \frac{1}{2}(L_{GE} - L_G - L_E) \quad (2)$$

$$M_{CG} = \frac{1}{2}(L_{CG} - L_C - L_G) \quad (3)$$

$$M_{CE} = \frac{1}{2}(L_{CE} - L_C - L_E) \quad (4)$$

where L_{GE} , L_{CG} , and L_{CE} stand for the inductance between the gate and emitter, that between the collector and gate, and that between the collector and emitter terminals, respectively. As a

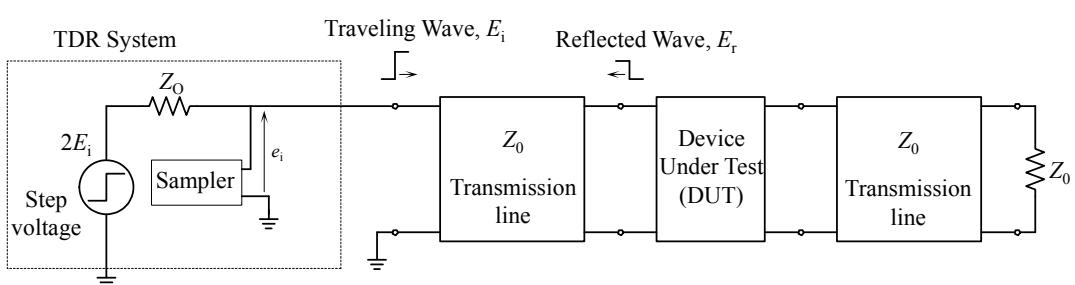


Fig. 5 Basic principle of the TDR measurement.

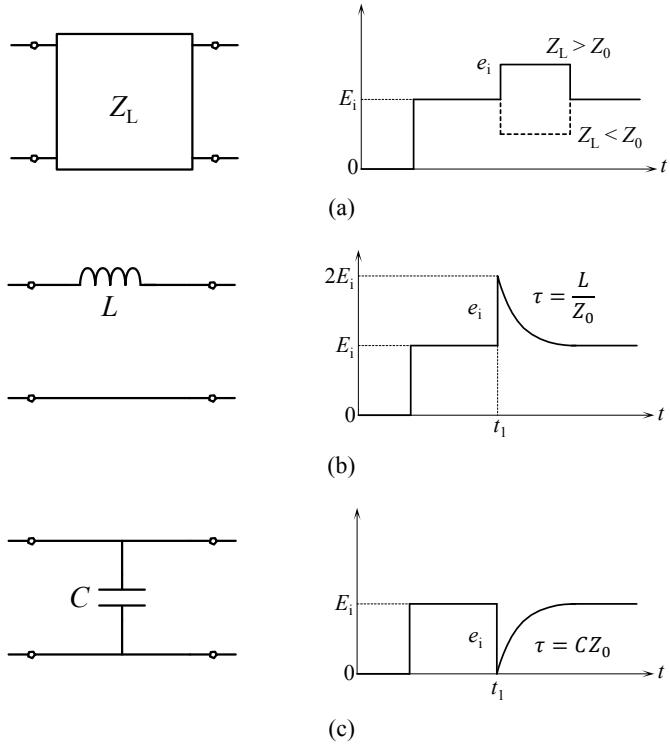


Fig. 6 Reflected waveform of DUT. (a) mismatched impedance element. (b) series inductance. (c) shunt capacitance.

result, introduction of the neutral point N makes it possible to separate all the self and mutual inductances.

between two of the four terminals

C. Decision of the Neutral Point N by Scanning Acoustic Tomography

Fig. 4 illustrates an internal structure of a discrete IGBT package that consists of an IGBT chip, a base plate, and three terminals. The collector terminal is directly connected to the base plate, whereas the gate and emitter terminals are connected to the IGBT chip by bonding wires. Hence, \$L_G\$ and \$L_E\$ tend to be larger than \$L_C\$. The neutral point should be as close to the center of IGBT chip as possible, so that it is necessary to know its location in the package. This paper introduces scanning acoustic tomography to obtain an internal image of the package [10]. Fig. 5 shows a scanned internal image of the DUT, where a discrete IGBT with TO-247 package (IRG7PH46U, rated at 1200 V 130 A, International Rectifier) is used. The probing point of the neutral point is decided according to the scanned image as described in section IV.

III. TDR MEASUREMENT

A. TDR principle

Fig. 5 illustrates a basic principle of the TDR measurement that consists of a step generator with an amplitude of \$2E_i\$ and a

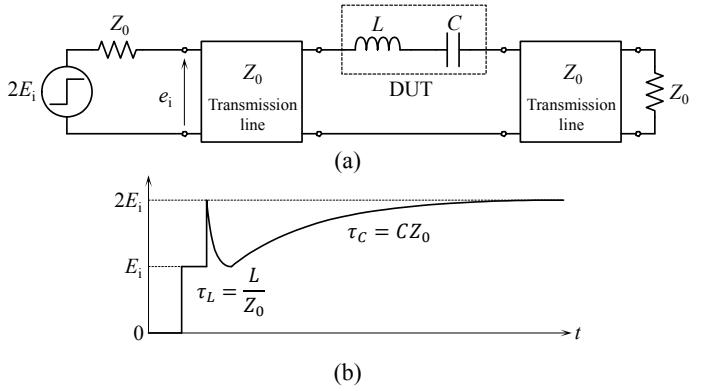


Fig. 7 Effect of the capacitance between terminals of the DUT. (a) Equivalent circuit in measurement. (b) Impedance profile.

transmission line having a characteristic impedance of \$Z_0\$. The step voltage progresses into the transmission line as a travelling wave without reflection if the characteristic impedance is constant, whereas it is reflected at a mismatched impedance point. If a device under test (DUT) is inserted in the transmission line, a reflected wave \$E_r\$ occurs at the DUT, and be observed at the sampler. Fig. 6 shows reflected waveforms of three examples: a discontinuous impedance element shown in (a), a series inductance shown in (b), and a shunt capacitance shown in (c). The mismatched load termination result in a discontinuous profile according to \$Z_L\$. The series inductance acts as an open circuit at an instant that the travelling wave arrives at the inductance, and then the impedance profile decreases with a time constant of \$L/Z_0\$. Hence, the inductance can be calculated by the following equation:

$$L = \frac{Z_0}{E_i} \int_{t_1}^{\infty} e_i(t) dt \quad (5)$$

The shunt capacitance shown in Fig. 3(c) behaves as a short circuit at an instant that the travelling wave arrives at the inductance, and then the impedance profile increases with a time constant of \$CZ_0\$. The capacitance can be calculated by the following equation:

$$C = \frac{1}{Z_0 E_i} \int_{t_1}^{\infty} e_i(t) dt \quad (6)$$

As a result, the TDR measurement presents an impedance profile in time domain.

B. Effect of input, output, and reverse transfer capacitances

Since the TDR measurement provides an inductance between two of the four terminals, the travelling wave progresses through capacitance between the two terminals, i.e., input, output, and/or reverse transfer capacitance in the DUT, except between the neutral point N and the collector terminal. Fig. 7 shows an equivalent circuit of the DUT measurement, in which the DUT consists of a series circuit of stray inductance and the capacitance between terminals. In practice, however, the capacitance act behaves as almost a short circuit because the time constant of \$\tau_c = CZ_0\$ is much larger than that of \$\tau_L = L/Z_0\$. \$\tau_c\$ takes of the order of 100 ns in case \$C\$ is of the order of 1000 pF, whereas \$\tau_L\$ takes of the order of 0.1 ns in case \$L\$ is of the

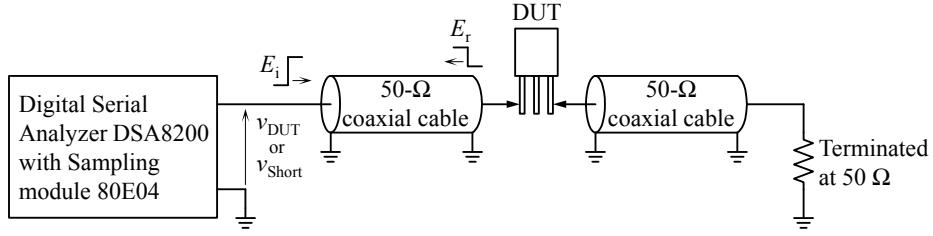


Fig. 8 Experimental system configuration.

order of 1 nH. Thus, it is possible to distinguish the reflection

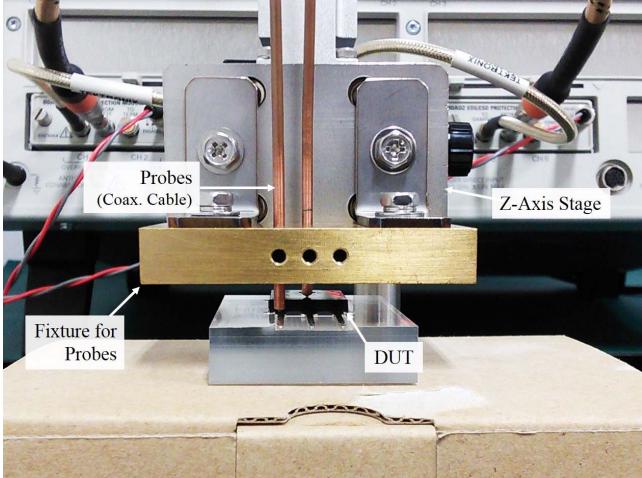


Fig. 9 Exterior of the experimental setup.

resulting from the inductance and that from the capacitance.

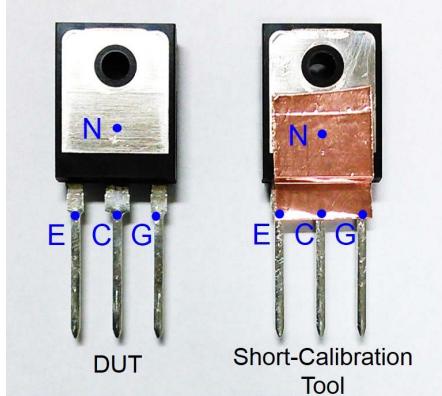


Fig. 10 DUT and short-calibration tool, indicating probing points.

IV. EXPERIMENT

A. Experimental Setup

Fig. 8 shows system configuration of the TDR measurement for the DUT, where a digital serial analyzer (sampling oscilloscope) DSA8200 equipped with a TDR sampling module 80E04 is used. The sampling module generates a step voltage

E_i of 250 mV with a rise time less than 17.5 ps. Fig. 9 shows exterior of the experimental setup that is designed and constructed for TO-247 packages. The setup consists of a fixture for probes and a Z-axis stage to contact the probes with the DUT. The probes consist of semi-rigid coaxial cables RG405/U. Two set of the probe contact two of four terminals including the neutral point, so that the setup measures each self inductance and inductance between each terminal.

Fig. 10 shows the DUT and the short-calibration tool using the same DUT covered with copper foil tape, and indicates probing points of the gate, emitter, collector, and neutral point. Experimental results were obtained by subtracting the result by DUT and that by the short-calibration tool.

B. Results

Figs. 11-16 show experimental waveforms tested between the emitter and neutral point, between the collector and neutral point, between the gate and neutral point, between the emitter and collector, between the gate and collector, and between the gate and emitter, respectively. As the experimental waveforms are shown over a range of 1500 ps, they contains reflection resulting almost only from the inductance.

Figure 17 shows summary of all the self and mutual inductances in the IGBT package obtained from the experimental waveforms. Note that L_C is much smaller than L_G or L_E because the neutral point is put on the base plate at the collector. This also brings quite small values into M_{CG} and M_{CE} .

V. CONCLUSION

This paper has proposed a measurement method of mutual inductance for power device packages using time domain reflectometry. The method identifies not only self inductances but also mutual inductances among collector, emitter, and gate (or drain, source, and gate) terminals using four-terminal measurement. A measurement fixture for a discrete IGBT is designed, constructed, and tested to ensure repeatability of the proposed method. Experimental results verified that the proposed method identifies self and mutual inductances separately.

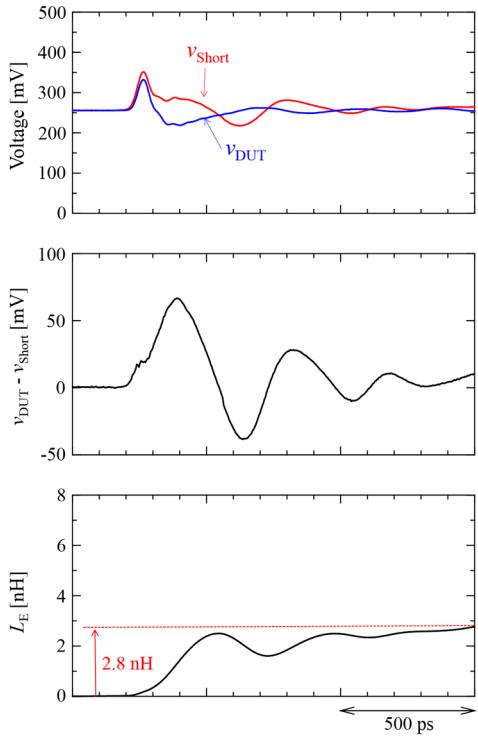


Fig. 11 Experimental result of inductance between the gate and neutral point, L_E

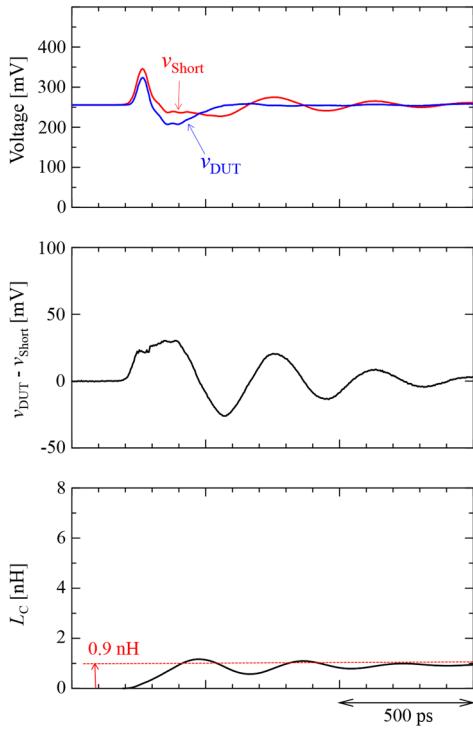


Fig. 12 Experimental result of inductance between the collector and neutral point, L_C

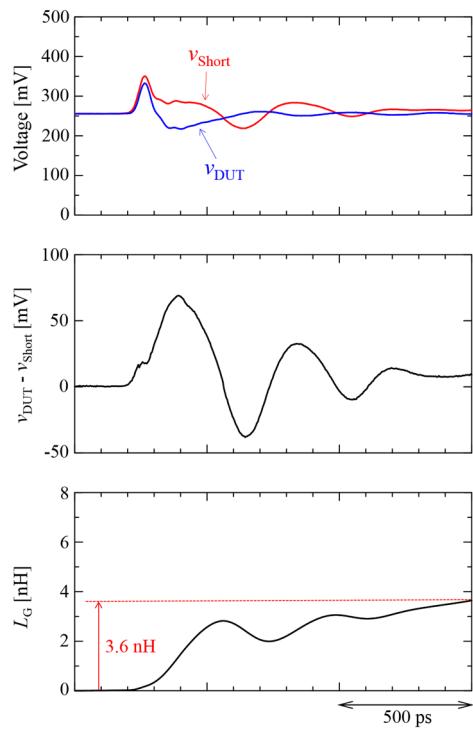


Fig. 13 Experimental result of inductance between the collector and neutral point, L_G

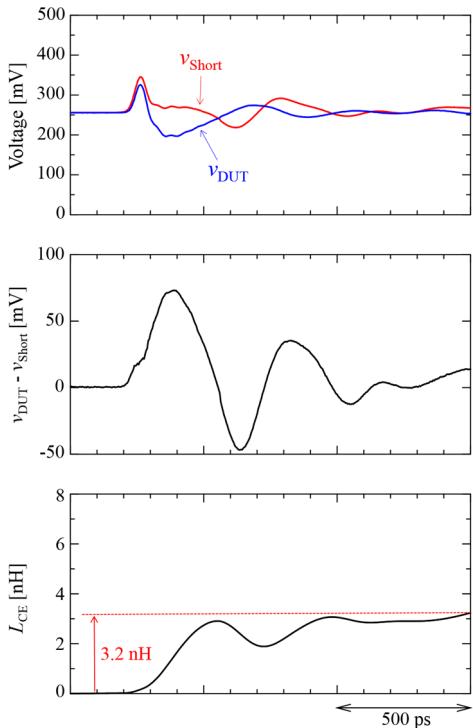


Fig. 14 Experimental result of inductance between the collector and neutral point, L_{CE}

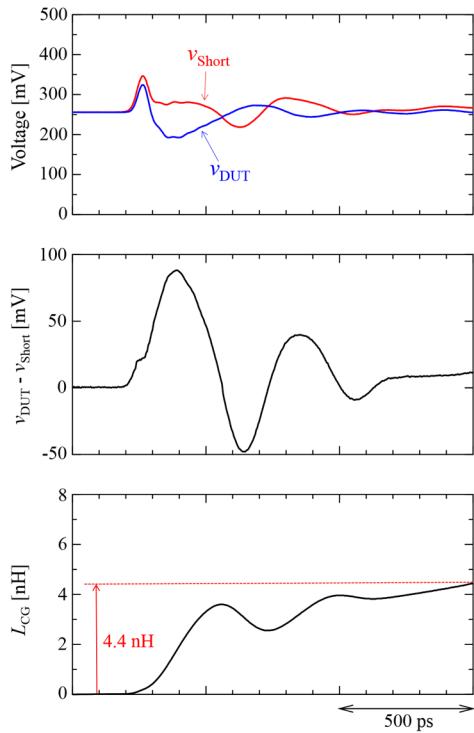


Fig. 15 Experimental result of inductance between the collector and neutral point, L_{CG}

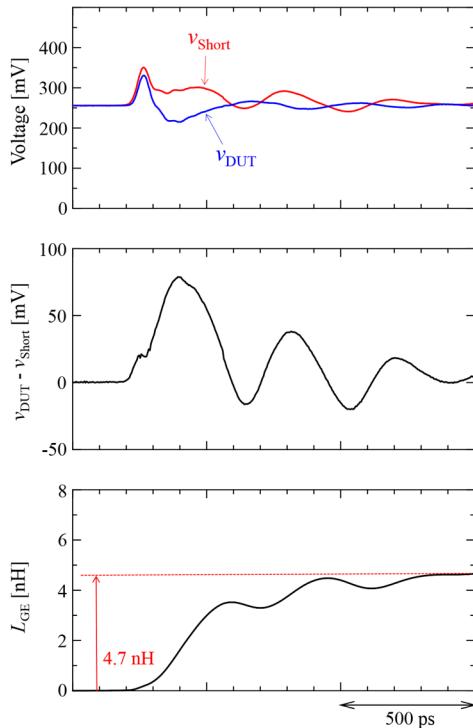


Fig. 16 Experimental result of inductance between the collector and neutral point, L_{GE}

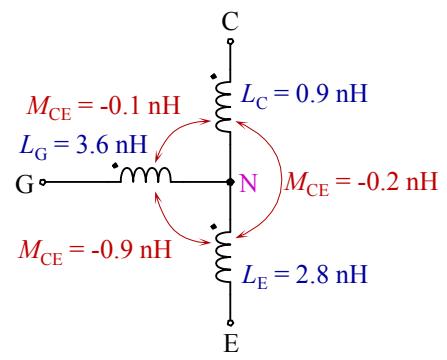


Fig. 17 Summary of all the self and mutual inductances obtained by experiment.

ACKNOWLEDGMENT

This paper is based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

REFERENCES

- [1] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental Parametric Study of the Parasitic Inductance Influence on MOSFET Switching Characteristics," *IEEE Intl. Power Electron. Conf.*, pp.164-169, 2010.
- [2] H. Zhu, A. R. Hefner Jr., and J. -S. Lai, "Characterization of Power Electronics System Interconnect Parasitics Using Time Domain Reflectometry," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 622-628, 1999.
- [3] Y. Wang, K. P. Cheung, R. Choi, and B. -H. Lee, "An accurate capacitance voltage measurement method for highly leaky devices—Part I," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2429–2436, Sep. 2008.
- [4] Y. Wang, K. P. Cheung, R. Choi, and B. -H. Lee, "An accurate capacitance voltage measurement method for highly leaky devices—Part II," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2437–2442, Sep. 2008.
- [5] S. Hashino and T. Shimizu, "Separation measurement of parasitic impedance on a power electronics circuit board using TDR," *IEEE ECCE*, pp. 2700-2705, 2010.
- [6] Z. Ariga, K. Wada, and T. Shimizu, "TDR Measurement Method for Voltage-Dependent Capacitance of Power Devices and Components," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3444-3451, Jul. 2012.
- [7] J. Wang, H. S. Chung, and R. T. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," vol. 28, no. 1, pp. 573-590.
- [8] S. Sandler, Faster-switching GaN: Presenting a number of interesting measurement challenges," *IEEE Power Electron. Mag.*, vol. 2, no.2, pp. 24-31, June 2015.
- [9] I. Omura, "Future Role of Power Electronics," *Intl. Conf. on Integrated Power Electronics Systems (CIPS)*, pp. 1-9, 2010.
- [10] A. Watanabe, M. Tsukuda, and I. Omura, "Failure analysis of power devices based on real-time monitoring," *Microelectron. Rel.*, vol. 55, no. 9-10, pp. 2032-2035, Aug./Sept. 2015