Temperature and Voltage Measurement for Field Test Using an Aging-Tolerant Monitor

Yousuke Miyake, Yasuo Sato, Seiji Kajihara, and Yukiya Miura, *Member*, IEEE

***Abstract*—Measuring temperature and voltage in a current VLSI is very important in guaranteeing its reliability, because a large variation of temperature or voltage in field will reduce a delay margin and makes the chip behavior unreliable. This paper proposes a novel method of temperature and voltage measurement, which can be used for variety of applications such as field test, on-line test, or hot-spot monitoring. The method counts frequencies of more than one ring-oscillator, which composes an aging-tolerant monitor. Then, the temperature and the voltage are derived from the frequencies using a multiple regression analysis. To improve accuracy of measurement, three techniques of an optimal selection of ring-oscillator types, their calibration, and hierarchical calculation, are newly introduced. In order to make sure the proposed method, circuit simulation in 180 nm, 90 nm and 45 nm CMOS technologies is performed. In the 180 nm CMOS technology, the temperature accuracy is within 0.99 ℃, and the voltage accuracy is within 4.17 mV. Furthermore, some experimental results using fabricated test chips with 180 nm CMOS technology confirms its feasibility.**

***Index Terms*—Temperature monitor, voltage monitor, ring oscillator, field test, delay test**

I. INTRODUCTION

INCREASING system complexity and structural shrinking in semiconductor fabrication process make it harder and harder to achieve high reliability of VLSI systems. Especially for safety related systems such as automobiles, aircrafts or social infrastructure systems it is a crucial issue to guarantee their reliability against circuit aging [1-5].

One promising approach to achieve the high reliability is field test, which regularly measures the delay margin [6-10]. Field test is performed on a periodic basis during a short period at power-on, power-off, or idle time by embedded test structures [6, 7]. As the environment where the test is performed is diverse, the temperature varies in a wide range, and the supply voltage is not easy to control. Then, hot-spots on the chip or low voltage area caused by static IR-drop affect circuit delay. High temperatures or low voltages generally increase circuit delays, and low temperatures or high voltages decrease delays [8, 24]. In this way, the measured delay values are affected very much by the environment during testing. To monitor the variation of intrinsic delay caused by aging or other reasons, both the temperature and the voltage during testing should be well-controlled ideally. When it is difficult to control them, temperature and voltage on the chip should be monitored. An accurate delay measurement is proposed by removing the influence of environment from the measured delay [9, 10].

When an environment monitor is used in field test, the following features are desired:

1. Both the temperature and the voltage are measured simultaneously.
2. The measurement accuracy is guaranteed under process variation.
3. The measurement time is short compared to the test period of the field test.
4. The costs of design and manufacture are minimized.
5. Aging of the monitor itself is avoided.
6. The monitor can be placed close to the circuit under test.

There has been a lot of research activity regarding on-chip monitors to measure the temperature and/or the voltage [11-15]. Temperature sensor using a bipolar transistor as a thermal diode is the most popular sensor whose advantage is high accuracy. However, it imposes various restrictions on design and measurement. A CMOS temperature sensor using the substrate bipolar transistor has an inaccuracy of ±1.0℃ in the range of -40℃ to 120 ℃ [11]. This sensor needs a constant reference voltage and an ADC (analog-to-digital converter). A TDC (time-to-digital-converter)-based temperature sensor [12], which uses temperature-to-pulse generator, has an inaccuracy of -0.7 to +0.9℃ in the range of 0℃ to 100℃. A CMOS smart temperature sensor with a PTAT(proportional-to-absolute temperature) bias circuit and a sigma-delta ADC, has an inaccuracy of ±0.1℃ (3σ) in the range of -55℃ to 125 ℃ [13]. The measurement accuracies of these sensors are high, however, they need an analog comparator, an ADC, a reference current source or complex calibration. Then, they are usually placed only at a few locations on the chip which makes it difficult to observe temperature data of various locations on the chip or identify hot-spots. Furthermore, their power consumption may high.

An alternative to the sensors with thermal diode are a

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ring-oscillator-based sensor [14]. Its merits are low area overhead and low power consumption. Therefore, they have less restriction on placement and larger number of sensors can be embedded on a chip. On the other hand, some of them require a reference current or a clean supply voltage for calibration. Quenot et al. [15] proposed a measurement circuit using delay programmable ring oscillators that was developed for analysis of thermal dissipation and power distribution. That circuit can measure the temperature and the voltage simultaneously. The inaccuracy is less than 50 mV and 3℃ in the ranges of 4V to 6V and 20℃ to 80℃. The advantages are low area overhead and a simple design. The major disadvantage is that it requires complex processing for mapping the measured frequencies of ring oscillators into a (T, V) plane, where T is the temperature and V is the voltage. Also a standard cell library cannot be used, since the transistor and diffusion resistances in the circuit need to be designed at specific values.

The previous works [11-15] never take into account the degradation caused by circuit aging in field. There are circuit aging phenomena as electro-migration, BTI (Bias Temperature Instability), and HCI (Hot Carrier Injection). It is difficult to compensate for preventing BTI because it degrades while the transistor does not work. Although some methods [16, 17] to cut off the power supply to the circuit during non-operation are proposed, they require a dedicated power switch.

This paper proposes a novel temperature and voltage ($T\&V$) measurement method, which is suitable for the field test, on-line test, hot-spot monitoring and many other applications. The proposed method calculates $T\&V$ values simultaneously with an aging-tolerant monitor. The calculation is based on multiple regression analysis from frequencies of three different types of ring-oscillators (ROs) in the monitor. As the measurement procedures are fully digital, it is easy to implement the monitor on chip, i.e., the monitor circuit consists of logic gates in the cell library without any special cells. Therefore, it can be placed at various locations including hot-spots of the chip.

In order to achieve high measurement accuracy, the proposed measurement employs three techniques, which are an optimal ring-oscillator selection, calibration of the ROs, and hierarchical $T\&V$ calculation. Although there are many RO types with different logic gate types and fan-out numbers, this paper proposes a procedure for optimal RO selection with respect to the measurement accuracy. A selected RO has an aging-tolerant structure for BTI. Calibration based on the initial measurement result of each RO is necessary to handle process variation. The hierarchical calculation is employed, in which $T\&V$ is roughly calculated to choose a subrange and then the calculation equation of the chosen subrange is applied to calculate more accurate $T\&V$. Using this method, the linear approximation is localized in a small subrange and the approximation errors of temperature range or voltage can be reduced greatly.

Field test is one of target applications of ($T\&V$) measurement. In the field test, $T\&V$ at each test session may not be the same. It is important that the fluctuations of $T\&V$ caused by environment should be measured. The fluctuation of $T\&V$ caused by a circuit behavior itself like self-heating and supply voltage noise is not important, because the same test patterns are applied repeatedly at every test session. The fluctuations caused by the circuit behavior itself can be negligible by using the relative differences of the fluctuation of $T\&V$. The proposed method can derive the fluctuations caused by environment as the relative differences of temperature and voltage from the normal values.

In this work, a measurement time of the proposed method is set below 100µs. For example, when an allowable test time is 10ms in a typical power-on test for automotive devices, at most 100µs (1%) will be available for a temperature and voltage measurement.

Thus, unlike the previous works, the monitor satisfies all of the necessary features 1)-6) for the field test. A preliminary version of this work was presented in [18, 19], where the basic idea of temperature and voltage measurement [18], Calibration and hierarchical calculation and some methods for accurate calculation [19] were proposed.

In 180 nm CMOS technology using the proposed method, the temperature measurement accuracy is 0.86 ℃ to 0.94℃, and the voltage accuracy is 2.98 mV to 4.17 mV. The measurement accuracy of the proposed method is not better than that of the related works. However, this accuracy is enough to measure hot-spots on the chip because the path delay variation due to temperature variation, which is investigated from a measured RO frequency and a calculated temperature of test chip, is $1.23[ps/℃]$. For instance, in order to suppress the error of delay measurement within 5 ps, the temperature measurement accuracy is required to be below 4.06℃.

This paper is organized as follows. Section 2 describes the concept of the proposed $T\&V$ measurement method using ROs. Section 3 describes a design of the proposed monitor. Section 4 shows simulation results for the monitors with 180 nm, 90 nm and 45 nm CMOS technologies, respectively. Section 5 shows results of test chip evaluation. Section 6 concludes the paper.

II. T&V Calculation from RO Frequencies

A. Basic Idea of T&V Calculation Using Multiple Regression Analysis

Fig. 1 shows examples of relations between the RO frequency and temperature, and between the RO frequency and voltage. For example, in case of the 45 nm or mature CMOS technology, the RO frequency decreases when temperature increases, and the RO frequency increases when voltage increases. Thus, $T\&V$ characteristics of the RO frequency F are described as a function in equation (1). When the voltage is fixed, the temperature can be expressed as a function $f_T(F)$ for frequency F in equation (2). Similarly, when the temperature is fixed, the voltage can be expressed as a function $f_V(F)$ for F in equation (3). Both $f_T(F)$ and $f_V(F)$, which are non-linear functions, can be approximated as linear function. These equations suggest that T or V can be calculated from the frequency of an RO. Thus, a basic idea is to use linear approximation to calculate T or V from F. In general, the functions of $T\&V$ characteristics are non-linear with respect to

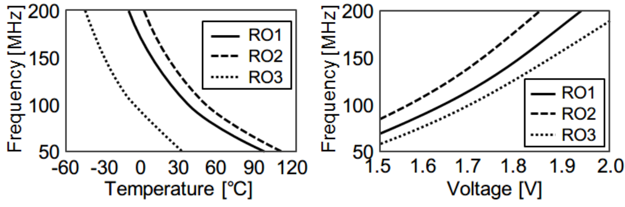


Fig. 1. T&V characteristics of the ROs

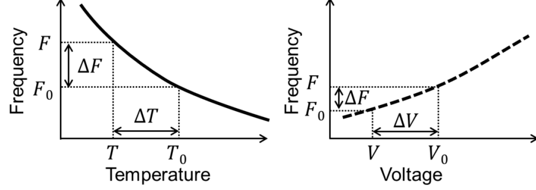


Fig. 2. Relation between (F, T, V) and (ΔF, ΔT, ΔV)

frequency. Therefore, the *T&V* calculated using linear functions include some amount of error. However, the linear functions are easy to implement either by software or by hardware because of their simplicity. Using linear approximation, the functions to calculate *T* or *V* from *F* can be expressed by equations (2)' and (3)', respectively.

$$F = g(T, V) \quad (1)$$

$$T = f_T(F) \quad \text{for a fixed } V. \quad (2)$$

$$V = f_V(F) \quad \text{for a fixed } T. \quad (3)$$

$$T \cong aF + b \quad \text{for a fixed } V. \quad (2)'$$

$$V \cong cF + d \quad \text{for a fixed } T. \quad (3)'$$

In general, neither *T* nor *V* may be known in field. Then, it is difficult to calculate both *T* and *V* accurately from one variable *F*. This problem can be solved by using more than one RO that has different *T&V* characteristics. Assume that there are three ROs with different *T&V* characteristics on a chip. The RO frequencies F_1, F_2, and F_3 can be expressed as function g_1, g_2, and g_3 of *T&V* as shown in equations (4), (5) and (6). Linear equations (7) and (8) will be obtained from three equations (4), (5) and (6) by the multiple regression analysis that calculates dependent variables (T, V) from independent variables (F_1, F_2, F_3). Because the relations of F_i and *T&V* can be investigated using *SPICE* simulation, equations (7) and (8) are created from the simulation data at design phase.

$$F_1 = g_1(T, V) \quad (4)$$

$$F_2 = g_2(T, V) \quad (5)$$

$$F_3 = g_3(T, V) \quad (6)$$

$$T = h(F_1, F_2, F_3) = a_T * F_1 + b_T * F_2 + c_T * F_3 + d_T \quad (7)$$

$$V = k(F_1, F_2, F_3) = a_V * F_1 + b_V * F_2 + c_V * F_3 + d_V \quad (8)$$

Constants $a_T, a_V, b_T, b_V, c_T, c_V, d_T$ and d_V are coefficients of calculation, which are generated by the multiple regression analysis. *T&V* are calculated by applying the calculation equations to the measured RO frequencies of the real chip. Thus the calculation method proposed in this paper employs the linear approximation and the multiple regression analysis from the frequencies of three ROs with different *T&V* characteristics. Note that the higher the number of ROs, the better the measurement accuracy, but calculation becomes more complex.

B. Calculation Using Differential Frequencies

A differential approach, which uses difference between two RO frequencies at different *T&V*, is used to implement *T&V* calculation. Fig. 2 illustrates the relation between *F*, *T* and *V* of an RO. The RO frequency F_0 as a reference is measured under well-controlled $T_0\&V_0$ in manufacturing test. The differential frequency ΔF is the difference between the RO frequency at $T_0\&V_0$ and the RO frequency at actual *T&V*. We define $F = F_0 + \Delta F$, $T = T_0 + \Delta T$, and $V = V_0 + \Delta V$. The equations (7) and (8) are extended using the differential approach leading to the following equations:

$$\Delta T = a_{\Delta T} * \Delta F_1 + b_{\Delta T} * \Delta F_2 + c_{\Delta T} * \Delta F_3 + d_{\Delta T} \quad (9)$$

$$\Delta V = a_{\Delta V} * \Delta F_1 + b_{\Delta V} * \Delta F_2 + c_{\Delta V} * \Delta F_3 + d_{\Delta V} \quad (10)$$

where, $\Delta F_1, \Delta F_2$ and ΔF_3 are differential frequencies. $d_{\Delta T}$ and $d_{\Delta V}$ are usually non-zero values, because the linear approximation is adjusted to all range instead of T_0 or V_0.

C. Calibration for Process Variation

The differential approach is useful to tackle with the process variations. Process variation is classified into two categories: global variation and local variation [20]. By global variation characteristics of transistors may change smoothly across the entire wafer. Then, the RO frequencies differ depending on their location of the wafer. On the other hand, by local variation characteristics of transistors vary independently. Therefore, frequency variation caused by local variation will be reduced to $1/\sqrt{N}$ times according to the law of large numbers, where *N* is the number of RO stages. As a result, the *TVM* can reduce the influence of local variation by increasing the number of RO stages at the expense of increased area overhead.

As for the global variation, when process variation is not negligible, the errors of calculation would be larger than the ones calculated from the typical process.

In a simple transistor model of an inverter in CMOS technology, equations (11) and (12) are given using the following parameters that influence the RO frequency [24].

- T_D : Gate delay (rise/fall time)
- L_G : Gate length
- W_G : Gate width
- C_L : Load capability
- C_{OX} : Gate oxide capacitance
- μ : Electron mobility
- V_{DD} : Supply voltage
- V_{th} : Threshold voltage
- I_{DS} : Source-drain current
- RO_Stage : Number of RO stages
- α : temperature dependent of threshold voltage
- ΔT : temperature variation

Note that parameters μ_n and V_{thn} for an NMOS transistor are assumed to be the same as μ_p and V_{thp} for a PMOS transistor, which are denoted as μ and V_{th}, respectively. F_i and T_D are calculated by the following equation

$$F_i = \frac{1}{2 \cdot T_D \cdot RO_Stage} \quad (11)$$

$$T_D = \frac{C_L \cdot V_{DD}}{I_{DS}} = \frac{2L_G}{C_{OX} \cdot \mu} \cdot \frac{C_L}{W_G} \cdot \frac{V_{DD}}{V_{DD} - V_{th}(1 - \alpha\Delta T)} \quad (12)$$

T&V characteristics are determined by a circuit structure of the RO. Relation between the *T&V* characteristics and the

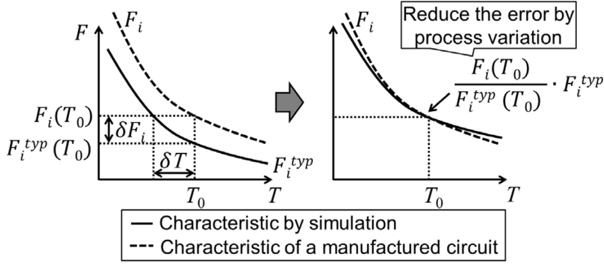


Fig. 3. Influence reduction for process variation

circuit structure will be discussed in Section 3.3.

The proposed technique tackles a variation of the threshold voltage that is influenced by the process variation. Fig. 3 illustrates the influence of the process variation on the RO frequency. There is the RO frequency F_i^{Typ} (solid line) in the typical process, and the RO frequency F_i (dashed line) is a measured frequency, which includes the influence of the process variation. Even though the temperatures are the same, the frequencies F_i^{Typ} and F_i are not the same because of the process variation. The error of calculation δT occurs, when temperature is calculated from δF_i, which is the difference between F_i^{Typ} and F_i. The error not only affects temperature but also the calculated voltage.

To tackle the problem of the process variation, calibration based on the initial measurement of each RO is performed. The proposed technique calibrates parameters in the calculation in order to reduce the influence of the process variation.

Ratios of the RO frequency of F_i^{Typ} and F_i are expressed as the equation (13) from the equation (11) and (12).

$$\frac{F_i}{F_i^{typ}} = \left(\frac{V_{DD}-V_{th}}{V_{DD}-V_{th}^{typ}}\right)\left(1-\left(\frac{V_{th}}{V_{DD}-V_{th}}-\frac{V_{th}^{typ}}{V_{DD}-V_{th}^{typ}}\right)\cdot\alpha\Delta T\right) \quad (13)$$

V_{th}^{typ} is the threshold voltage in the typical process, and V_{th} is the actual threshold voltage that includes the influence of the process variation. The variation of the RO frequency caused by the actual process variation for threshold voltage can be known using the ratios of the F_i^{Typ} for the F_i.

Fig. 3 explains the calibration technique to reduce the error caused by global variation. Ratios of the process variation are obtained by comparing the measured frequencies with the typical frequencies $\{F_i(T_0,V_0)/F_i^{typ}(T_0,V_0)\}$ for $i = 1,2,3$ at the initial measurement for each RO, where *T* and *V* are known or well-controlled as (T_0, V_0). That is, the temperature variation ΔT in the equation (13) is zero. Therefore, δF_i can be zero by the calibration using the ratios at the initial measurement. Then, the measurement error is able to be reduced. That is, the calculation equations are corrected by multiplying the ratios in equations (9) and (10). Equations (14) and (15) are used instead of equations (9) and (10). ΔT includes the influence of the reduced δT.

$$\Delta T \cong a_{\Delta T}\frac{F_1^{typ}(T_0,V_0)}{F_1(T_0,V_0)}\Delta F_1 + b_{\Delta T}\frac{F_2^{typ}(T_0,V_0)}{F_2(T_0,V_0)}\Delta F_2 + c_{\Delta T}\frac{F_3^{typ}(T_0,V_0)}{F_3(T_0,V_0)}\Delta F_3 + d_{\Delta T} \quad (14)$$

$$\Delta V \cong a_{\Delta V}\frac{F_1^{typ}(T_0,V_0)}{F_1(T_0,V_0)}\Delta F_1 + b_{\Delta V}\frac{F_2^{typ}(T_0,V_0)}{F_2(T_0,V_0)}\Delta F_2 + c_{\Delta V}\frac{F_3^{typ}(T_0,V_0)}{F_3(T_0,V_0)}\Delta F_3 + d_{\Delta V} \quad (15)$$

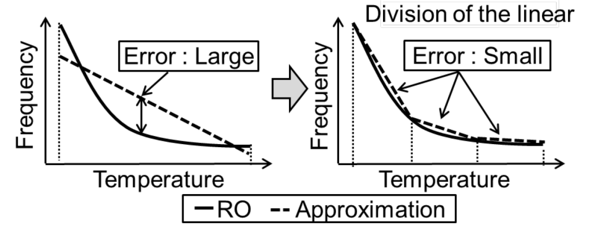


Fig. 4. Linear approximation

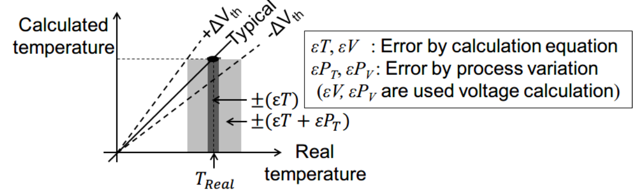


Fig. 5. Relation between calculated and real temperature

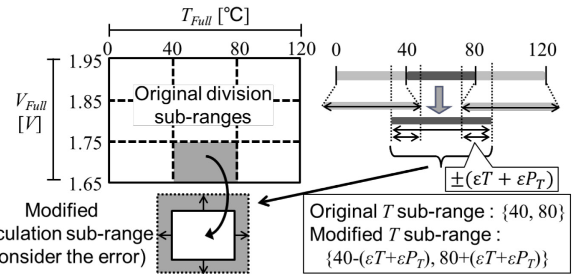


Fig. 6. Considerations of Error Ranges

The correction of equations corresponds to the change of parameters $a_{\Delta T}, a_{\Delta V}, b_{\Delta T}, b_{\Delta V}, c_{\Delta T}, c_{\Delta V}, d_{\Delta T}$ and $d_{\Delta V}$ which are generated by the multiple regression analysis as shown in Section 2.2.

As the amount of global variation differs according to the chip or the location on a chip, this calibration should be applied to every RO. The proposed calibration technique will reduce the influence of global variations such as die-to-die or within-die variations. Its effectiveness will be evaluated in the Section 4.

D. Division of T&V Ranges

The proposed *T&V* calculation uses a linearity of *T&V* characteristics of each RO. The measurement error due to the linearity is defined as the standard deviation of the error distribution of the linear approximation of the original characteristic function as shown in Fig. 4. Low standard deviation corresponds to high linearity. The *T&V* calculated by linear equations generally include some amount of approximation errors. The division of the *T&V* range into plural sub-ranges in calculation is useful for the reduction of errors caused by linear approximation. However, the problem of how to select the sub-range remains. The selected sub-range should include the real *T&V* denoted as T_{Real}&V_{Real}, because the *T&V* are calculated using the linear equation of the each sub-range. The process variation may affect the selection of the corresponding sub-range. Thus, regardless of the amount of the

process variation, the proposed method determines the sub-ranges.

Fig. 5 shows the relation between calculated temperature and real temperature. In temperature measurement, an error by process variation εP_T and a calculation error εT exist in the result. As well as temperature measurement, voltage measurement includes an error by process variation εP_V and a calculation error εV. The maximum and minimum error by process variation can be calculated by simulation corresponding to the highest and lowest V_{th}, respectively. The relations between the real values T_{Real} & V_{Real} and the calculated values T_{Cal}&V_{Cal} are given in relations (16) and (17). Note that εT and εV are the maximum errors due to the non-linearity, and εP_V and εP_T are the maximum errors by process variation. For example, relation (16) means that T_{Cal} exists in the interval whose center is the real temperature T_{Real}, and whose width is the twofold sum of εT and εP_T. Relation (17) means that the calculated V exists in the interval, whose center is the real voltage V_{Real}, and whose width is the twofold sum of εV and εP_V.

$$T_{Real} - |\varepsilon T + \varepsilon P_T| \leq T_{Cal} \leq T_{Real} + |\varepsilon T + \varepsilon P_T| \quad (16)$$

$$V_{Real} - |\varepsilon V + \varepsilon P_V| \leq V_{Cal} \leq V_{Real} + |\varepsilon V + \varepsilon P_V| \quad (17)$$

Fig. 6 shows the relation between the original sub-range and the modified sub-range taking the errors into account. Each original range is divided into three sub-ranges without any overlap. The modified sub-ranges are wide enough to allow the errors $\varepsilon T + \varepsilon P_T$ and $\varepsilon V + \varepsilon P_V$. Then, the equations are created for each modified sub-range. Neighboring sub-ranges are overlapped. The amount of the error $|\varepsilon T + \varepsilon P_T|$ for temperature is expressed as E_T for simplicity. Let the original sub-ranges of temperature be (T_1, T_2) and (T_2, T_3), the modified sub-ranges will be $(T_1 - E_T,\ T_2 + E_T)$ and $(T_2 - E_T,\ T_3 + E_T)$, respectively. Then, there is overlapped area $(T_2 - E_T, T_2 + E_T)$. The calculation error caused by linear approximation on the overlapped area is expressed as $\varepsilon T(T_1 - E_T,\ T_2 + E_T)$. As well as temperature, voltage has the original sub-ranges, the modified sub-ranges, and the overlapped area. In the overlapped area, either calculation equation for one sub-range including T_{Cal}&V_{Cal} can be applied, and the amount of errors is less than the largest error of the modified sub-ranges. Note that the number of division is three in this paper for simplicity, but it can be adjusted to match any errors εT,εV,εP_T and εP_V.

E. Hierarchical Calculation Procedure

In order to apply an equation of the sub-range including T_{Real} & V_{Real}, a procedure of hierarchical calculation is proposed (hereafter, "sub-range" is used in the meaning of "modified sub-range" as far as there is no risk of misunderstanding).

Fig. 7 illustrates the proposed procedure of hierarchical calculation. (The equations are defined for each sub-range). The calculation equations for the full-range and the divided sub-ranges are prepared. A rough calculation using the calculation equation for full-range (A) is performed, in order to find the sub-range including V_{Real} in terms of V. Then, a V sub-range is selected. Since the selected V sub-range is

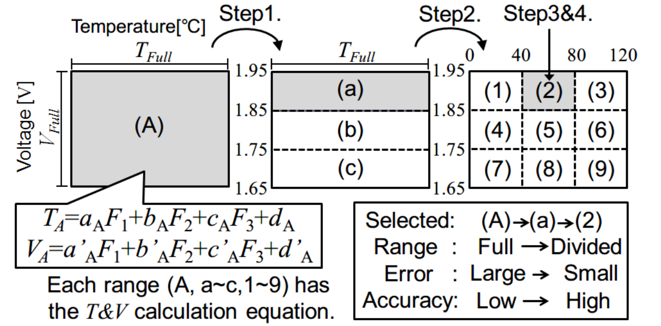


Fig. 7. Hierarchical calculation method

Algorithm Hierarchical Calculation

Input: F_1, F_2, F_3
Output: T_{cal}, V_{cal}
1: $V_{cal} \leftarrow V_A$;
2: **if** $1.65\text{V} \leq V_{cal} \leq 1.75\text{V}$ **then**
3: $T_{cal} \leftarrow T_a$;
4: **if** $0°\text{C} \leq T_{cal} \leq 40°\text{C}$ **then** $V_{cal} \leftarrow V_1$; $T_{cal} \leftarrow T_1$;
5: **else if** $40°\text{C} < T_{cal} \leq 80°\text{C}$ **then** $V_{cal} \leftarrow V_2$; $T_{cal} \leftarrow T_2$;
6: **else if** $80°\text{C} < T_{cal} \leq 120°\text{C}$ **then** $V_{cal} \leftarrow V_3$; $T_{cal} \leftarrow T_3$;
7: **else if** $1.75\text{V} < V_{cal} \leq 1.85\text{V}$ **then**
8: $T_{cal} \leftarrow T_b$;
9: **if** $0°\text{C} \leq T_{cal} \leq 40°\text{C}$ **then** $V_{cal} \leftarrow V_4$; $T_{cal} \leftarrow T_4$;
10: **else if** $40°\text{C} < T_{cal} \leq 80°\text{C}$ **then** $V_{cal} \leftarrow V_5$; $T_{cal} \leftarrow T_5$;
11: **else if** $80°\text{C} < T_{cal} \leq 120°\text{C}$ **then** $V_{cal} \leftarrow V_6$; $T_{cal} \leftarrow T_6$;
12: **else if** $1.85\text{V} < V_{cal} \leq 1.95V$ **then**
13: $T_{cal} \leftarrow T_c$;
14: **if** $0°\text{C} \leq T_{cal} \leq 40°\text{C}$ **then** $V_{cal} \leftarrow V_7$; $T_{cal} \leftarrow T_7$;
15: **else if** $40°\text{C} < T_{cal} \leq 80°\text{C}$ **then** $V_{cal} \leftarrow V_8$; $T_{cal} \leftarrow T_8$;
16: **else if** $80°\text{C} < T_{cal} \leq 120°\text{C}$ **then** $V_{cal} \leftarrow V_9$; $T_{cal} \leftarrow T_9$;

Fig. 8. Algorithm of hierarchical calculation

broadened to the modified range by taking errors into account, V_{Real} would exist in the selected V sub-range. Furthermore, by using the calculation equation of a small range, errors caused by linear approximation can be reduced, and a measurement accuracy of V can be improved. Final values of T&V are calculated using a calculation equation of the T&V sub-range such as range (2) in Fig. 7.

Such a hierarchical calculation narrows down the range of T&V alternately, in order to use a sub-range including T_{Real}&V_{Real}. The details are shown in the following:

Step1: Select a sub-range of V using calculation equation for V under the T&V full-ranges. The T range is still full-range, but the V range becomes a sub-range described as range (a) in Fig. 7.

Step2: Select a T sub-range using the equation for T under the full-range of T and the V sub-range. The selected range is a T&V sub-range described as range (2) in Fig. 7.

Step3: Calculate V_{Cal} using calculation equation of the selected T&V sub-range.

Step4: Calculate T_{Cal} using calculation equation of the selected T&V sub-range.

Fig. 8 shows an algorithm of the hierarchical calculation. V_A, V_a, V_b, V_c, V_1, … , V_9, T_A, V_a, T_b, T_c, T_1, … , and T_9 are calculation values using T&V calculation equation of each T&V

range such as $V_A = a_A F_1 + b_A F_2 + c_A F_3 + d_A$.

It should be noted that three T sub-ranges are prepared for each V sub-range; the calculation equations, which are shown in equations (7) and (8), are defined for each $T\&V$ sub-range.

In general, as voltage influence the RO frequency more than temperature, selection of V sub-range should be performed before selection of T sub-range. However, the influence of temperature and voltage on the frequency is dependent on the number of sub-ranges and the width of each range. For example, when the number sub-ranges for V is greater than that for T, selection of T sub-range should be performed before selection of V sub-range.

III. TVM DESIGN

A. Influence of NBTI on ROs

If the ROs used in the $T\&V$ monitor (hereafter denoted as *TVM*) degrade as time passes, the measurement accuracy of the *TVM* will be getting worse and worse. Aging such as electro-migration or HCI can be avoided by stopping oscillation, it is known that Negative BTI (NBTI) degrades the RO even if it does not oscillate. This section discusses an aging-tolerant RO structure focusing on NBTI. Note that PBTI may be likely to its influence in future CMOS technology as well as NBTI and the proposed idea of the aging-tolerant structure can be extended to PBTI.

NBTI of a PMOS transistor occurs while the PMOS transistor is "ON". If the PMOS transistor is "OFF", the transistor is not degraded. Although, a recovery effect of NBTI is also known, it is too slow to cancel the aging [21-23].

Fig. 9 shows a typical structure of a basic RO consisting of one 2-input NAND gate and four inverters. The RO has two operation modes, which are an oscillation mode and a non-oscillation mode. When *En* input is set to 1, the RO operates in the oscillation mode. When *En* input is set to 0, the RO moves to the non-oscillation mode and stops the oscillation. While the RO is in the non-oscillation mode, aging by NBTI occurs at the PMOS transistors of inverters A and B. This is because the PMOS transistors in the inverters stay "ON" during the non-oscillation mode.

B. Aging-Tolerant Structure of ROs

In this section, a special structure of ROs is introduced such that NBTI-aging occurring in the non-oscillation mode is prevented [18].

Fig. 10 shows an example of the aging-tolerant RO structure, which consists of an odd number of 2-inputs NAND gates. Its oscillation is controlled by control inputs *En* and *Start* and it has the following three operation modes as shown Fig. 11.

1. Non-oscillation mode:

In case *En* and *Start* are set to 0, the RO is in the non-oscillation mode. Gate output S3 and subsequent input S2 of all 2-input NAND gates are kept 1. The RO does not oscillate and all transistors P1, P2, N1 and N2 are kept in the states shown in Table I. In the RO structure of the 2-input NAND gate as shown in Fig.10, the transistors used for oscillation are PMOS transistor P1 and NMOS transistor N1. Since P1 is kept "OFF", NBTI does not degrade P1 during the non-oscillation mode. On the other hand, PMOS transistor P2 is kept "ON" and NMOS transistor N2 is kept "OFF". Since P2 is kept "ON", NBTI degrades P2 during the non-oscillation mode. However, the degradation of P2 does not affect the oscillation of the RO because P2 does not be used for oscillation.

2. Initialization mode:

In case *En* is set to 1 and *Start* is set to 0, the RO is in the initialization mode. The gate outputs are initialized just before starting oscillation. The outputs of 2-input NAND gates on the oscillation loop are kept "0" and "1" alternately. The initialization mode is necessary to prevent a race of oscillation signals which is caused by changing values of more than one gate outputs simultaneously. Because the time of the initialization mode is far shorter than that of the other modes, the effect of NBTI in the initialization mode is negligible.

3. Oscillation mode:

In case *En* is set to 1 and *Start* is set to 1, the RO is in the oscillation mode. After the initialization mode, *Start* signal is changed from 0 to 1, and the RO oscillates. In the oscillation mode, PMOS transistor P1 switches its state between "ON and OFF" repeatedly. NBTI of P1 occurs when P1 is "ON" in the oscillation mode. However, the oscillation time can be far shorter than the non-oscillation time in field use. For example in Section 5.5, it is shown that 1μs of oscillation time is enough for frequency stabilization. If the $T\&V$ measurement does not have to be performed continuously, NBTI of the P1 will be negligible in the oscillation mode.

In the same manner as Fig. 10, other types of NBTI-tolerant RO can be easily implemented. One is a 4-input ORNAND type RO that consists of 4-input complex gates as shown in Fig. 12. The 4-input complex gate can be described as a gate level circuit with one 2-input NAND gate followed by two 2-input OR gates. The transistors used for oscillation are PMOS transistor P4 and NMOS transistor N4 in Fig. 12. Since P4 is kept "OFF", NBTI does not degrade P4 during the non-oscillation mode. Furthermore, the degradation of others transistor do not affect the oscillation of the RO.

Thus it is possible to compose aging-tolerant ROs not only for electro-migration and HCI but also for NBTI. As electro-migration and HCI are accelerated during the oscillation mode, their degradation in non-oscillation mode is also negligible. Although the proposed aging-tolerant ROs can not prevent all aging completely, the aging-tolerant ROs are effective as a monitor for field test.

C. Influence of Temperature and Voltage on RO frequency

Parameters that affect the RO frequency are shown in equation (12) in Section 2.3. The parameters μ and V_{th} are temperature dependent, and V_{DD} is voltage dependent. Though parameters L_G, C_{OX} and V_{th} affect $T\&V$ characteristics, they are determined by the CMOS technology. Different RO_Stage numbers of ROs generates different $T\&V$ characteristics, but the differences are trivial (i.e. the same coefficient ratios) [24]. The parameters that are related to the $T\&V$ characteristics and are controllable without designing a special cell are only W_G and C_L. Parameter W_G is related to the drive strength of a

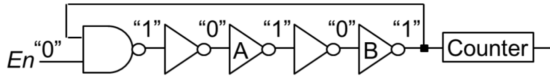


Fig. 9. Basic RO structure

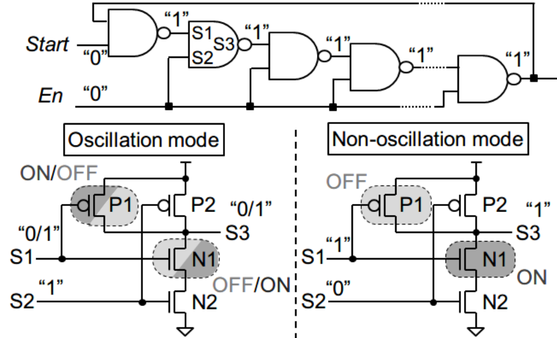


Fig. 10. Aging-tolerant RO with 2-input NAND gates

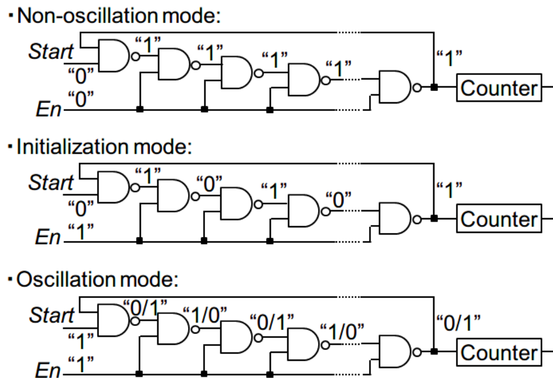


Fig. 11. Operation modes of TVM

TABLE I
STATE OF THE TRANSISTOR WITH 2-INPUT NAND GATES

	Signal value		State of value			
	S2(En)	S1(S3)	P1	N1	P2	N2
Oscillation	1	0/1	ON/OFF	ON/OFF	OFF	ON
Non-Oscillation	0	1	OFF	ON	ON	OFF

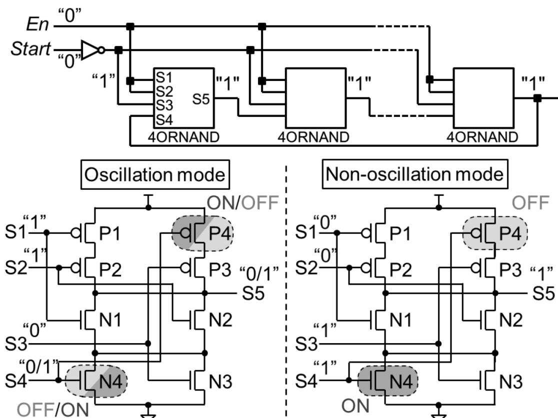


Fig. 12. Aging-tolerant RO with 4-input ORNAND gates

logic gate [25-28], and parameter C_L is related to the number of fan-outs of a logic gate. For each logic gate, several cells with different drive strength may be provided in a standard cell library. The number of fan-outs of each gate can be chosen arbitrary up to the permitted maximum at design phase. Since the $T\&V$ characteristic of an RO can be controlled by changing the number of fan-outs and drive strength of logic gates, it is possible to prepare several ROs with different $T\&V$ characteristics using the cells provided in the standard cell library.

$T\&V$ characteristics such as $T\&V$ linearity are determined by drive strength and the number of fan-outs of a logic gate. When the drive strength increases, the ratio of given parameter $\{C_L/W_G\}$ in equation (12) decreases. When the number of fan-outs increases, the ratio $\{C_L/W_G\}$ also increases. Because the parameters that have temperature dependency and voltage dependency are different, the different $T\&V$ characteristics of the ROs can be generated. Furthermore, when the type of logic-gate is different (e.g. 2-input NAND or 3-input NAND), the different $T\&V$ characteristics can be obtained. Since the number of transistors of 2-input NAND and 3-input NAND is different, the ratio $\{C_L/W_G\}$ and an equation of the transistor model such as equation (12) are different.

Even if the type of logic-gate is same, the different $T\&V$ characteristics can be obtained when the drive strength and the number of the fan-outs are different. However, when the drive strength is N times, the ratio is $1/N$ times. Thus, ROs of the same type of logic-gate may become similar $T\&V$ characteristics each other.

D. RO Selection Procedure

The proposed *TVM* is composed of three ROs with different $T\&V$ characteristics. One of the important factors for high measurement accuracy is the selection of an optimal combination of three RO types from a menu of many RO types different in composition. When there are N kinds of available ROs with different logic gate types, fan-out or drive strength, the number of combinations of three ROs is ${}_NC_3$. The proposed procedure tries to select the optimal combination from them without examining accuracy of all combinations. The proposed procedure first checks the linearity of the temperature and the voltage characteristic of each RO with *SPICE* simulation respectively, and then selects ROs composing the *TVM* according to their linearity.

The following shows the procedure to select three ROs of RO1, RO2 and RO3:

Step 1: Prepare RO candidates that are different in composition from one another.

Step 2: Calculate the linearity of each RO in terms of temperature and voltage.

Step 3: Select RO1, RO2 and RO3 to compose a *TVM*.

3-1) Select RO1 whose linearity for voltage is the highest of all candidates.

3-2) Select RO2 whose linearity for temperature is the highest of the candidates that consist of different logic gate composition from RO1.

3-3) Select RO3 where the sum of normalized linearity for temperature and voltage is the highest of the candidates that consist of different logic gate types from RO1 and RO2.

In Step 1, a variety of ROs are provided for RO selection. Here, the ROs should have an aging-tolerant logic structure as shown in Section 3.2. The NAND gate-based RO in Fig. 10 and the 4ORNAND gate-based RO in Fig. 12 can be used as

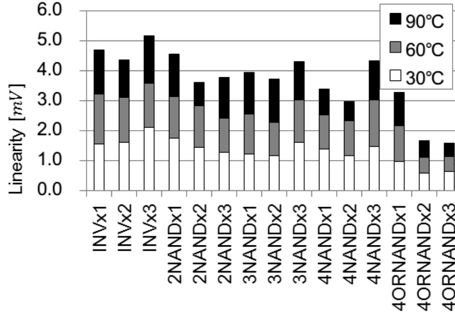


Fig. 13. Linearity of the voltage (RO1)

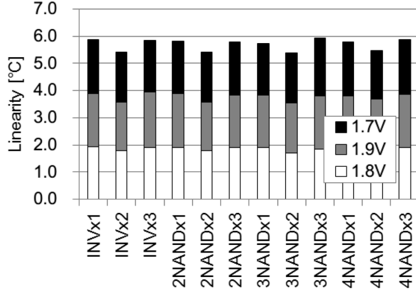


Fig. 14. Linearity of the temperature (RO2)

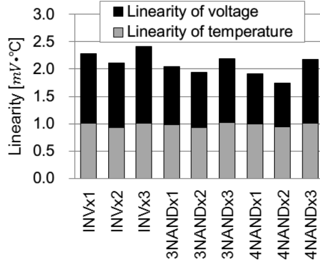


Fig. 15. Linearity of the temperature and voltage (RO3)

candidates. The number of RO types increases by changing the drive strength or the number of fan-outs.

In Step 2, *SPICE* simulation is first performed to calculate the frequency of each RO provided in Step 1 for several combinations of T and V values. For the voltage linearity, three points of temperatures 30, 60 and 90 ℃ are examined. If a typical V_{DD} voltage is 1.8 V, voltage is examined from 1.7 V to 1.9 V by 0.05 V increment (in case of 180 *nm* CMOS technology). From the simulation results, a linear approximation function for each temperature is derived by the least-squares method. The sum of mean square errors of the functions (i.e. for each temperature) is defined as the voltage linearity of the RO, where small errors mean high linearity.

Temperature linearity is defined similarly to the voltage linearity. Three points of voltage are examined at each temperature. If a typical V_{DD} voltage is 1.8 V, voltage is examined at 1.7, 1.8 and 1.9 V (in case of 180 *nm* CMOS technology). The temperature range is between 20 ℃ and 100 ℃ and the increment is 10 ℃.

In Step 3, three RO types are selected according to the linearity calculated in Step 2. RO1 and RO2 are selected with the highest linearity for voltage and temperature, respectively. To avoid selecting ROs with similar $T\&V$ characteristics,

TABLE II
COMBINATIONS OF THE SELECTED ROs

	Selected ROs by proposed method			Approximation error	
Technology	Step1	Step2	Step3	Temperature [℃]	Voltage [mV]
180nm	4ORNANDx3	2NANDx2	4NANDx2	1.19	2.66
45nm	4ORNANDx1	2NANDx2	4NANDx1	3.05	7.71

TABLE III
APPROXIMATION ERROR

	Temperature error [℃]			Voltage error [mV]		
	Selected ROs	#RANK:1	Average	Proposed ROs	#RANK:1	Average
180nm	1.19 (RANK:22)	1.00	1.82	2.66 (RANK:3)	1.99	4.79
45nm	3.05 (RANK:3)	3.03	5.43	7.71 (RANK:1)	7.71	17.27

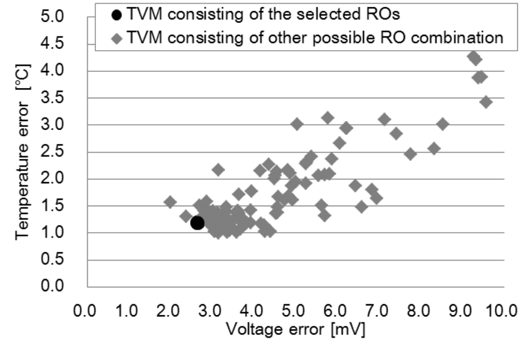


Fig. 16. Approximation error of the all combinations (180 nm)

different types of RO are selected. For example, if an RO of 2-input NAND gates is selected as RO1, RO2 is selected from ROs of 3-input NAND, 4-input NAND or 4ORNAND etc.. For RO3, the sum of normalized linearity of temperature and voltage is calculated and the most linear one is selected.

E. Evaluation results of RO Selection

RO selection procedure was performed for 180 *nm* and 45 *nm* CMOS technology, respectively. The available RO types for the selections are as follows:

Technology: 180 *nm*

Cell types are INV, ORNAND(input-4), and NAND(input-2,3,4). Drive strength are x1, x2, and x3.

Technology: 45 *nm*.

Cell types are INV, ORNAND(input-4), and NAND(input-2,3,4). Drive strength are x1, x2, and x4.

They include NAND gates with 2, 3 or 4 inputs, 4ORNAND gate shown in Fig. 10, and an inverter (note: the inverter is for reference only because its RO is not aging-tolerant). The drive strength is 1, 2 or 3 for each cell. In sum, there are 12 types of RO available, and there are 108 kinds of *TVM*s possible to be composed of these ROs.

Fig. 13 shows the result of voltage linearity of each RO for 180 *nm* CMOS technology. The RO of 4ORNAND gate with drive strength 3 has the highest linearity (the smallest value), which will be selected as RO1. Fig. 14 shows the result of temperature linearity. The ROs consisting of 4ORNAND gates have a little bit lower linearity (larger value). The RO of 2-input NAND gates with drive strength 2 has the best linearity and is selected as RO2. Fig. 15 shows the result of the sum of normalized linearity of $T\&V$, and the RO consisting of 4-input

NAND gate with drive strength 2 has the best linearity, which is selected as RO3. Table II shows the summary of RO selections for 180 *nm* and 45 *nm* CMOS technology.

Table II also shows the approximation errors of the *TVM*s using the selected ROs. The errors are calculated as the standard deviation of errors with the multiple regression analysis. For 180 *nm* CMOS technology, the temperature and voltage accuracies were 1.19 ℃ and 2.66 mV, respectively. For the 45 *nm* CMOS technology, the temperature and voltage accuracies were 3.05 ℃ and 7.71 mV, respectively. In order to ensure the validity of the proposed procedure, the approximation errors of all other ROs are checked in Table III, where the rankings of the selected ones are shown.

In case of 45 *nm* CMOS technology, almost the best *TVM* is selected by the proposed procedure. In case of 180 *nm* CMOS technology, although the rank of the *TVM* consisting of the selected ROs was the 22nd in temperature accuracy and the 3rd in voltage accuracy, the absolute values of error are close to those of the best one. This can be seen in Fig. 16 which shows the errors of all possible *TVM*s. It suggests that the method only using the linearity may be not enough to evaluate *T&V* characteristics of ROs. The use of other criteria such as gradients of frequencies for *T&V* ($\Delta F/\Delta T$ and $\Delta F/\Delta V$ etc.) in addition to linearity remains future work.

IV. Evaluation by Circuit Simulation

A. Measurement Accuracy

In order to evaluate the accuracy of the proposed measurement method and the effects of hierarchical calculation, *SPICE* simulations were performed for 180 *nm*, 90 *nm* and 45 *nm* CMOS technology, respectively. In the evaluation, the *TVM* consists of the following three ROs; RO1 has 51 stages of 2NAND with fan-out of 1, RO2 has 19 stages of 4ORNAND with fan-out of 4, and RO3 has 21 stages of 2NAND with fan-out of 7.

The simulation conditions are as follows:

Technology: 180 *nm*.

T range: 0℃ to 120℃ with 1℃ increment.

V range: 1.65V to 1.95V with 0.05V increment.

Technology: 90 *nm*.

T range: -40℃ to 110℃ with 5℃ increment.

V range: 1.00V to 1.30V with 0.05V increment.

Technology: 45 *nm*.

T range: 0℃ to 120℃ with 1℃ increment.

V range: 0.91V to 1.09V with 0.01V increment.

Tables IV, V and VI show the measurement accuracy levels for each CMOS technology. The accuracy levels are expressed with standard deviation of errors of the approximations in the full-range (2nd and 6th columns, 3rd line) or the divided three sub-ranges (3-5th, 7-9th columns, 4-6th lines) of *T&V*. For instance, the temperature accuracy 3.21℃ in the full-range (2nd column, 3rd line) is reduced to 0.86℃ in a sub-range (3rd column, 5th line) in 180 *nm* CMOS technology. The results in the tables show that the division technique improves the measurement accuracy significantly. The temperature accuracy was improved from 3.21℃ to 0.86-0.99℃, and the voltage accuracy

TABLE IV
Measurement Accuracy (180 nm)

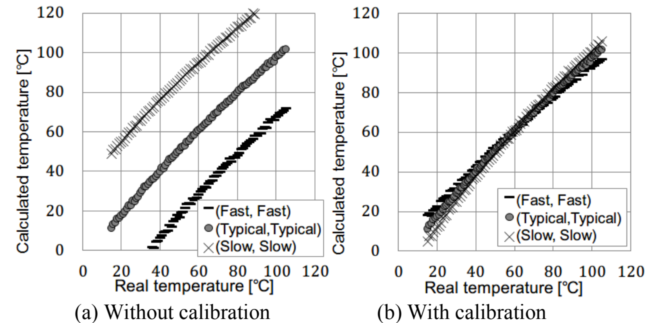
180 nm		Temperature accuracy [℃]				Voltage accuracy [mV]			
V_0 : 1.80v T_0 : 60℃		Full-range	Sub-range			Full-range	Sub-range		
		0～120℃	0～40℃	40～80℃	80～120℃	0～120℃	0～40℃	40～80℃	80～120℃
Full-range	1.65v～1.95v	3.21	-	-	-	11.77	-	-	-
Sub-range	1.85v～1.95v	-	0.86	0.93	0.99	-	3.58	3.58	3.55
	1.75v～1.85v	-	0.86	0.91	0.98	-	3.97	3.32	3.34
	1.65v～1.75v	-	0.94	0.91	0.94	-	4.17	3.52	2.98

TABLE V
Measurement Accuracy (90 nm)

90 nm		Temperature accuracy [℃]				Voltage accuracy [mV]			
V_0 : 1.15v T_0 : 50℃		Full-range	Sub-range			Full-range	Sub-range		
		-40～110℃	-40～20℃	20～80℃	80～110℃	-40～110℃	-40～20℃	20～80℃	80～110℃
Full-range	1.00v～1.30v	2.84	-	-	-	7.49	-	-	-
Sub-range	1.20v～1.30v	-	1.17	0.87	0.65	-	2.58	2.19	1.73
	1.10v～1.20v	-	1.36	1.28	1.13	-	3.32	3.39	1.96
	1.00v～1.10v	-	1.20	1.08	0.76	-	2.27	2.88	1.40

TABLE VI
Measurement Accuracy (45 nm)

45 nm		Temperature accuracy [℃]				Voltage accuracy [mV]			
V_0 : 1.00v T_0 : 60℃		Full-range	Sub-range			Full-range	Sub-range		
		0～120℃	0～40℃	40～80℃	80～120℃	0～120℃	0～40℃	40～80℃	80～120℃
Full-range	0.91v～1.09v	4.13	-	-	-	10.67	-	-	-
Sub-range	1.03v～1.09v	-	2.09	1.81	1.42	-	7.72	6.03	4.17
	0.97v～1.03v	-	2.72	2.22	1.80	-	9.04	6.57	4.67
	0.91v～0.97v	-	3.75	2.85	2.29	-	11.30	7.62	5.33



(a) Without calibration (b) With calibration

Fig. 17. Effects of Calibration for Process Variation

TABLE VII
Effects of the Proposed Technique (180 nm)

180 nm V_0 : 1.80V T_0 : 60℃		Residual error				
		Without calibration			With calibration	
Process variation		*(Typical,Typical)*	*(Fast, Fast)*	*(Slow, Slow)*	*(Fast, Fast)*	*(Slow, Slow)*
Temperature [℃]	+Max.	0.58	-47.10	31.16	5.35	5.04
	-Max.	-1.23	-57.96	25.23	-5.85	-5.62
	Average	-0.27	-51.92	28.80	-0.07	-0.28
Voltage [mV]	+Max.	1.76	328.35	-235.43	12.95	10.59
	-Max.	-3.59	300.82	-257.61	-12.65	-15.50
	Average	-0.97	313.47	-248.02	-0.85	-1.02

was improved from 11.77 mV to 2.98-4.17 mV in 180 *nm* CMOS technology. In the same way, the accuracy was improved from 2.84℃ to 0.65-1.17℃ and from 7.49mV to 1.40-3.39 mV in 90 *nm* CMOS technology, and from 4.13℃ to 1.42-3.75℃ and from 10.67mV to 4.17-11.30 mV for 45 *nm* CMOS technology, respectively.

However, the voltage accuracy of one sub-range (0-40℃, 0.91-0.97V) in 45 *nm* CMOS technology was not improved. A possible reason is that the proposed RO selection procedure selects one combination of ROs for the full-range, not for each sub-range. Therefore, the combination of ROs might not be optimum for a specific sub-range.

B. *Effectiveness of Calibration Technique*

To evaluate of the proposed calibration technique for process variation in Section 2.3, *SPICE* simulation was performed for 180 *nm* CMOS technology using the same RO as Section 4.1. The simulation conditions were with the temperature range of 15℃ -105 ℃ with 1℃ increment, and with the fixed voltage of 1.8 V. Three types of threshold voltage (*Typical*, *Fast*, and *Slow*) are introduced as the process variation corners. (*Typical*, *Typical*) means that the threshold voltages of NMOS and PMOS transistors (*NMOS*, *PMOS*) have the typical values. In the same way, (*Fast*, *Fast*) and (*Slow*, *Slow*) corners are defined.

Fig. 17 (a) shows relations between real temperatures and calculated temperatures using three types of threshold voltage (*Typical*, *Typical*), (*Fast*, *Fast*) and (*Slow*, *Slow*). As seen from the data, the difference between the real temperature and the calculated temperature is large. The calculated temperature of (*Fast*, *Fast*) corner is lower than that of (*Typical*, *Typical*) corner. In the same way, the calculated temperature of (*Slow*, *Slow*) corner is higher than that of (*Typical*, *Typical*) corner.

Fig. 17 (b) shows the relation between real temperatures and calculated temperatures using the proposed calibration technique. The initial measurement was performed at 60℃, and the parameters of calculation equations were calibrated using the ratios of $\{F_{(Typical,Typical)}(60℃)/F_{(Fast,Fast)}(60℃)\}$ for (*Fast*, *Fast*), and $\{F_{(Typical,Typical)}(60℃)/F_{(Slow,Slow)}(60℃)\}$ for (*Slow*, *Slow*). The calibrated results in Fig. 17(b) show that the calculation errors were reduced.

Table VII shows the averages of residual errors shown in Fig. 17. In case of no calibration, the errors of temperature and voltage in (*Fast*, *Fast*) are -51.92 ℃ and 313.47 mV, respectively. By the proposed technique, the errors are reduced to -0.07 ℃ and 0.85 mV, respectively. The errors in (*Slow*, *Slow*) are 28.80 ℃ and -248.02 mV, respectively. By the proposed calibration technique, the errors are reduced to -0.28 ℃ and -1.02 mV, respectively.

The results show that the proposed calibration technique can greatly reduce the influence of the process variation.

Although the new values match to the real temperatures at the initial conditions, the errors seem to increase as the temperature difference becomes larger. For example, the error of temperature at 60 ℃ is 0.03℃, but the error temperature at 100 ℃ is already at -4.89℃, as shown in Fig. 17(b). This is because calibration is applied for only one point of *T&V*, and it may cause errors as other *T&V* points. Future research is required to solve this problem.

V. Evaluation by Test Chip

In this section, the effectiveness of *T&V* measurement and calibration technique is confirmed using a fabricated test chip. First, test chip design for *TVM* and area overhead are shown in in Section 5.1. Second, a validity of voltage measurement is discussed in Section 5.2. Third, a validity of temperature measurement is discussed in Section 5.3. Then, the effectiveness of *T&V* measurement and calibration is shown in Section 5.4. Finally, the measurement time is discussed in Section 5.5.

A. *Test Chip Design*

Fig. 18 shows the test chip design with 180 *nm* CMOS technology. The structure of the test chip is as follows:

- *TVM*: The three types of RO and counter.
- *TVM_controller*: The controller of the *TVM*.
- *Heating_circuit*: A heating circuit that consists of 1,000 ROs with controllable oscillation ratios to achieve various temperatures. The RO that consists of 9 stages of inverter is used only to generate self-heating effect. Note that the RO of the heating circuit are different from the ROs of the *TVM*.
- *Heating_circuit_controller*: The controller of the heating circuits.

Fig. 19 illustrates the circuit structure of a *TVM* using ROs. The *TVM* consists of three pairs of ROs and a counter. Three counter values are sent to *TVM_controller* in serial after the measurement; then, the values are stored in a non-volatile memory, which can be either on-chip or off-chip. After storing the counted value of the ROs, the *T&V* calculation is performed using on-chip or off-chip software or hardware. How to implement the calculation can be determined adapting to a product or a target application. More than one *TVM* is placed at various locations on a chip. Thus, the *TVM*s are able to monitor various spots including hot-spots on the chip.

Fig. 20 illustrates RO structures of the *TVM* in the test chip. RO1 of the *TVM* has 51 stages of 2NAND with fan-out of 1. RO2 has 19 stages of 4ORNAND with fan-out of 4. RO3 has 21 stages of 2NAND with fan-out of 7. Six *TVMs* are embedded in the chip. Four *TVMs* are placed at the chip boundary, and the others are placed near the center of the chip. Four heating circuits are placed between the *TVMs*. The chip temperature is controlled by the number of oscillating ROs in heating circuits, (e.g. 10% means that 100 ROs of the heating circuit are running). If the rate increases, the temperature increases. Changing the rate, *TVMs* can be measured at various temperatures.

The test chip is packed in QFP, which has only two pair of power supply pins at top and bottom of the chip in Fig. 18.

Table VIII shows the area overhead of the *TVM* and the *TVM_controller*. Because the numbers of total cells of *TVM* are only 291 cells, the impact on chip design will be small for a large industrial chip.

B. *Validity of Voltage Measurement*

When the proportion of oscillating ROs in the heating circuit increases, the corresponding current at the heating circuit also increases and the internal voltage at a location of the *TVM* drops.

Fig. 21 shows the relation between the voltage measured by the *TVM* and the current measured by ammeter. During 0% to 20% of the ratio of the heating circuit, the amount of calculated voltage drop is proportional to the amount of measured current. When the ratio is larger than 20%, the voltage drop by the heating circuit is somewhat larger than calculated. This is because the high resistance to the power supply due to the small number of power pins.

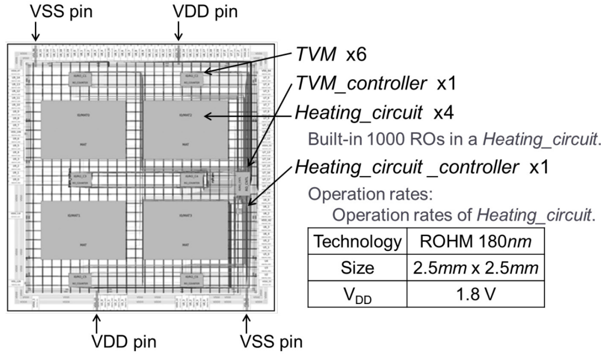


Fig. 18. Test chip design

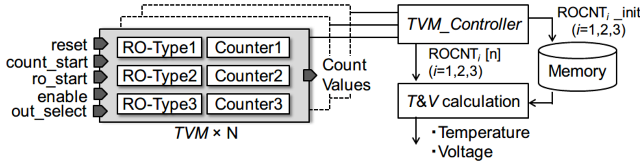
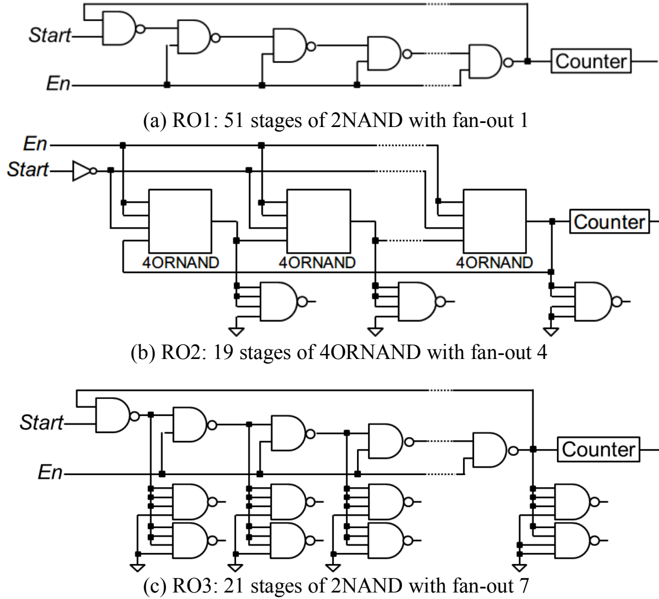


Fig. 19. TVM architecture



(a) RO1: 51 stages of 2NAND with fan-out 1

(b) RO2: 19 stages of 4ORNAND with fan-out 4

(c) RO3: 21 stages of 2NAND with fan-out 7

Fig. 20. RO structures of the TVM in the test chip

TABLE VIII
AREA OVERHEAD ONE TVM (180 NM)

	TVM					TVM_Controller
	RO1	RO2	RO3	counter	total	
Number of cells	55	66	44	126	291	407

C. *Validity of Temperature Measurement*

Fig. 22(a) shows the experimental setup of the test chip for evaluating the validity of temperature measurement. Fig. 23(a) shows a fabricated test chip. Fig. 23(b) shows the thermal map of surface temperature measured with an infrared camera (thermal image sensor) and internal temperatures by the *TVM*. The number of the data of surface temperature corresponding to the chip size (2.5×2.5 mm) is 9×9. Surface temperature of a bare chip is observed by the infrared camera to compare measured and real temperatures. The temperature of bulk silicon (T_a) is calculated from the surface temperature (T_b) using a thermal resistance and the thermal equation circuit model shown in Fig. 22(b). The relation between internal and surface temperature, which are given in equation (18), is extracted using Laplace transform. Here, R is thermal resistance and C is thermal capacity. The parameters of R and C are derived from a heating value of the chip and the thermal equation circuit model. X, Y, Z, α and β are constants derived from the model. ΔT_a and ΔT_b are the difference between the initial temperature at non-operating mode and the temperature at each activation ratio, respectively. The initial internal and surface temperatures are assumed to be the same at initial measurement of non-operating mode, because the measurement is performed after enough waiting time to stabilize and heat generations other than the heating circuits are prevented.

$$\Delta T_a = \Delta T_b \cdot RC \cdot \{X + Ye^{-\alpha t} + Ze^{-\beta t}\}^{-1} \quad (18)$$

Fig. 24 shows the comparison between the internal temperature measured by *TVM* and the internal temperature calculated from surface temperature by equation (18). In 0-20% activation ratio, calculated and measured temperature coincide very well. However, the error increases with more than 30% of heating ROs operating. This might be because the V value is so large at these rates that it is out of range (see Fig. 24). If the real *T&V* is out of the assumed ranges, improper sub-ranges are selected and the calculated values are incorrect.

D. *Validity of Calibration for Process Variation*

Fig. 25 shows the measured frequencies of the 6 ROs in each chip (see Fig. 18) using 10 fabricated chips. Each chip is kept at 0% activation ratio of the heating circuits. As seen in the figure, the measured frequencies differ significantly despite the same measurement condition. This is caused by the incorrect calculation due to process variation.

Then the proposed variation-aware technique is applied. The initial measurement was performed at 0% activation ratio, where the initial *T&V* are 60℃ and 1.8V for calibration. Ratios of the RO frequencies $\{F_i(60℃, 1.8\text{V})/F_i^{typ}(60℃, 1.8\text{V})\}$ for $i = 1,2,3$ are used in calibration. F_i is the measured frequencies. F_i^{typ} is computed in simulation for $(60℃, 1.8\text{V})$, which has been decided in advance (60℃ is a middle value of the temperature range in simulation). After the calibration, *T&V* are calculated from the difference between the initial and measured frequencies at each activation ratio. Fig. 26(a) shows the measured temperature improved by the calibration. The temperature of each chip at 0% activation ratio shows the same value of 60 ℃ as the initial environment and it increases corresponding to the operating rate. The variance of 10 chips is regarded as the process variation in the heating circuits. Fig. 26(b) shows the measured voltage of each chip. In the same way, the measured voltages at 0% operating rate are the same value of 1.8V for the initial condition. The voltage decreases corresponding to rising activation ratios. Thus, the effect of process calibration is confirmed by the experiments using the 10 fabricated chips.

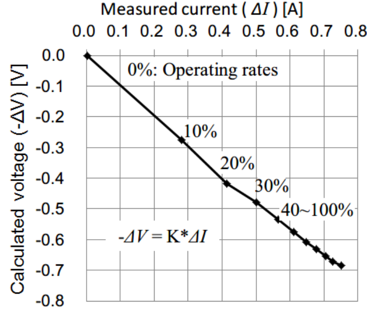
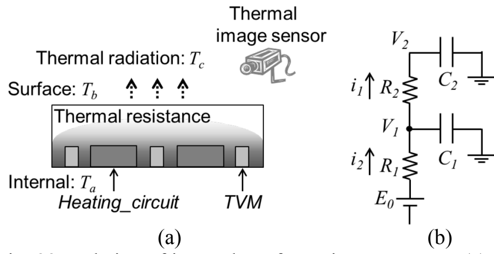
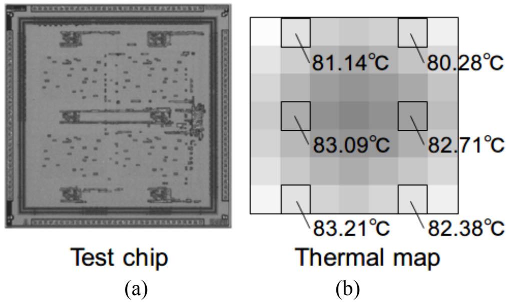


Fig. 21. Validity of voltage measurement



(a) (b)

Fig. 22. Relation of internal, surface, air temperature. (a) Experimental setup of the test chip; (b) Thermal equation circuit model



(a) (b)

Fig. 23. (a) Fabricated test chip. (b) Thermal map of surface temperature by the thermal image sensor and internal temperatures by the *TVM*.

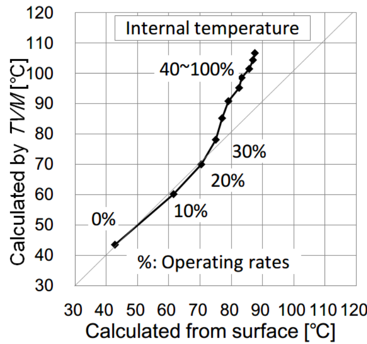


Fig. 24. Validity of temperature measurement

E. Measurement Time

Fig. 27(a) shows the measured RO count in the *TVM*. This is performed under the room temperature and 0% activation ratio of the heating circuits. The value increases as time passes. Fig. 27(b) shows the calculated frequencies in a short period (0-5μs). The frequency is calculated from the counted value in each 40ns interval. It takes about 1μs for stabilizing the frequencies. When the time is too short (0-1μs), a 1 bit error occupies a large

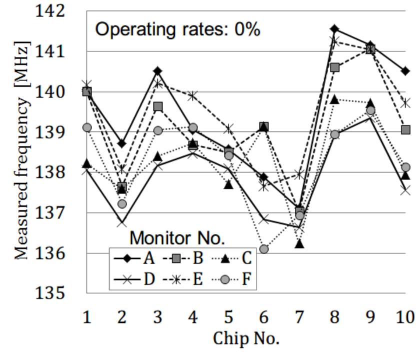
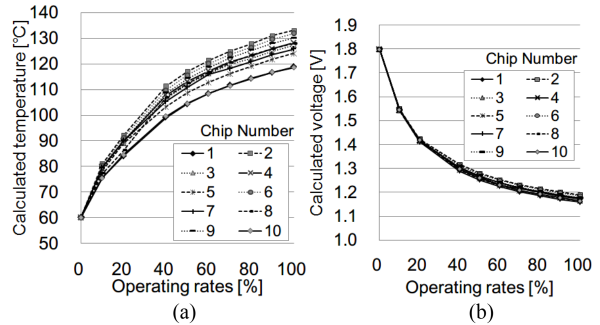
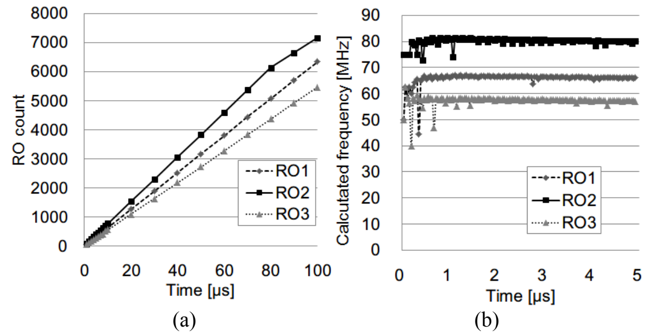


Fig. 25. Measured frequencies of test chips, which include actual process variation. (10 chips, RO1)



(a) (b)

Fig. 26. Evaluation by test chips 10 chips, 1 Monitor, location is top right corner in Figure 17, (a) Temperature Measurement, (b) Voltage measurement.



(a) (b)

Fig. 27. (a) Measured RO count in the test chip, (b) Frequency variation.

part in the counter, and the calculated frequency is not stable. It is also confirmed that the frequency is stable after 1μs.

In this work, the measurement of the ROs is performed inside of the test chip. Then, the calculation processing of *T&V* is performed outside of the test chip. Therefore, the measurement time of this section is not included *T&V* calculation time.

VI. Conclusion

This paper proposed a novel method of temperature and voltage measurement, which is suitable for various purposes in field or in debug. The proposed method measures the chip temperature and voltage simultaneously using multiple regression analysis. The aging-tolerant feature can prevent NBTI-induced degradation in field, and fully digital structure enables easy implementation on chip, where various locations including hot-spots should be monitored to improve reliability of the chip.

The method for improving measurement accuracy consists of three techniques, which are the optimal combination of ROs, calibration of ROs, and hierarchical calculation. The optimal combination method enables to find a highly accurate RO-combination from a variety of cell types only simulating at small number of (T, V) points. The result of 180 *nm* CMOS technology proved that the selected monitor achieves temperature and voltage accuracy almost close to the best one. A hierarchical calculation and calibration enables measurement with high accuracy under process variation. The evaluations using *SPICE* simulation were performed for 180 *nm*, 90 *nm* and 45 *nm* CMOS technologies. In the 180 *nm* CMOS technology, the temperature accuracy was 0.86-0.99℃, and the voltage accuracy was 2.98-4.17 mV. The experiment using test chip in 180 *nm* CMOS technology confirmed the validity of the monitor. The measured temperature and voltage matched well in some ranges to the directly observed ones by an infrared camera (thermal image sensor) and an ammeter.

The final goal of our research is developing an easy-to-use monitor of temperature and voltage that enables measuring them in each clock domain or at each hot-spot on a chip without any special design or any special set-up. However the measurement accuracies still not as good as dedicated analog monitors; the current results need some analysis and improvement, which are remaining for future work.

VII. Acknowledgement

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