# Reduction of NBTI-Induced Degradation on Ring Oscillators in FPGA

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***Abstract*—Ring Oscillators are used for variety of purposes to enhance reliability on LSIs or FPGAs. This paper introduces an aging-tolerant design structure of ring oscillators that are used in FPGAs. The structure is able to reduce NBTI-induced degradation in a ring oscillator's frequency by setting PMOS transistors of look-up tables in an off-state when the oscillator is not working. The evaluation of a variety of ring oscillators using Altera Cyclone IV device (60nm technology) shows that the proposed structure is capable of controlling degradation level as well as reducing more than 37% performance degradation compared to the conventional oscillators.**

***Keywords-component; Ring Oscillator; FPGA; Aging; NBTI***

## I. INTRODUCTION

The FPGA is widely used for various applications including highly reliable systems because of its easiness in system debugging due to its re-configurability. For achieving high reliability, a variety of application-dependent test technologies including logic tests, interconnect tests or path delay tests have been proposed [1-9]. These test methods achieve 100% test coverage in each focused parts utilizing re-configuration capability.

High precision sensors are also important to enhance reliability of a chip by monitoring various physical features. Especially, the ring oscillator is a soft sensor that can be easily implemented and has a lower power than a hard sensor such as diode sensors [10-11]. It is widely applied for monitoring various items such as process variation [12-16], temperature [17], IR-drop [18] or aging effects [19-23]. The authors also presented a field test technology that measures delay margin accurately by monitoring temperature and voltage by a ring-oscillator-based sensor [24].

These technologies should also be applied to FPGA applications. Though there are some technological issues for developing ring oscillators in FPGA due to its inherent logic and layout structures [25-28], many papers already have been published. Ring oscillators for monitoring process variations are introduced in [29-31]. Frequency variation of ring oscillators is measured and utilized to improve yield or to characterize a design. Ring oscillators as a reference clock are presented in [32-34], and are used for Time to Digital Converters (TDC). Thermal sensors using ring oscillators are discussed in [35-37]. They are also used for thermal testing in production test or in field test to improve reliability [38-39].

These many techniques have been used in FPGA; however, aging phenomena such as NBTI (Negative Bias Temperature Instability), PBTI (Positive Bias Temperature Instability) or HCI (Hot Carrier Injection) are becoming serious issues in the latest process technologies [40-41]. NBTI has become serious in less than 90nm processes, PBTI is going to be not negligible in less than 45nm processes, and HCI is known to be accelerated at rather high voltages such as in IO cells. The effect on MTTF (Mean Time to Failure) by several aging phenomena was evaluated in [40], and NBTI degradation was measured in [41]. Therefore, many aging monitors have been proposed [42-45]. They monitor critical paths or other critical parts of a chip in field. For avoiding malfunction in field, some on-line testing techniques also have been proposed [46-48].

Regarding aging impact on ring oscillators in FPGAs, few papers have addressed the problem as far as the authors know. The oscillators will be placed at plural locations on a chip to monitor various variables; therefore, a degraded ring oscillator will operate as an inaccurate sensor. It will worsen system reliability. As each transistor on a chip is prone to degrade, frequent characterizations in field will be needed to guarantee its accuracy. The authors proposed a NBTI-tolerant ring oscillator for ASIC/SoC in [24, 49]. The oscillator reduces NBTI-induced degradation by setting PMOS transistors of CMOS in an off-state when the oscillators are not working. Although it looks beneficial, the method cannot be applied for FPGA because of its distinctive logic structure. If the power supply for ring oscillators will be cut off when they are not working, the degradation will be prevented; however, it requires hardware overhead and it is not feasible for the current architectures of FPGAs.

The purpose of this paper is introducing an aging-tolerant design structure for ring oscillators that are used in FPGA. The structure is able to reduce NBTI-induced degradation in a ring oscillator's frequency by setting PMOS transistors of look-up tables in an off-state when the oscillators are not working. The evaluation of a variety of ring oscillators using Altera Cyclone IV device (60nm technology) shows that the proposed structure is capable of controlling degradation level as well as reducing more than 37% performance degradation compared to the conventional oscillators.

This paper is organized as follows. Section 2 describes the background and basic idea of our research. Section 3 describes the proposed structure of ring oscillators. Section 4 explains experimental results using various ring oscillators. Section 5 concludes the paper.

## II. BACKGROUND

### A. NBTI Degradation

NBTI is a well-known phenomenon, which degrades PMOS transistor performance. The performance of a chip gradually degrades as time elapses. The aging speed is estimated by the reaction diffusion (RD) model [50] or the trapping/de-trapping (TD) model [51]. Although there are some differences in regard to physical behavior and degradation speed, both models claim that the degradation progresses when the PMOS is active (in an on-state), and its speed is rather fast at an early stage and becomes slower as time passes (or quasi-saturates) because it is proportional to $n^{th}$ power of time $t$, where $n$ is less than one. The speed also depends on temperature and on-state ratio of each transistor. Therefore, it is hard to predict its degradation amount [52].

The degradation of transistors in FPGAs will be more serious than that in ASICs/SoCs because wire-routing requires a large number of transistor switches in FPGAs. Therefore, a design method to reduce NBTI-induced degradation is strongly required. Fig. 1 provides an evaluation of a ring oscillator in FPGA, which shows steady degradation in only one hour. The oscillator was implemented in a FPGA of Altera Cyclone IV (60nm technology) and heated at 40 degree in a constant temperature reservoir, and its oscillation frequency was measured at every minute with special care to reduce measuring noise (careful manual layout and isolated placement).

It is known that NBTI is caused when a transistor is stable, whereas HCI is caused when a transistor is transient [52]. As the oscillation time is only 82 $\mu$ seconds per a minute, the main cause of degradation was supposed to be NBTI. Even though the amount of degradation is very small, it will become non-negligible in several years. The data implies seriousness of degradation in FPGA.

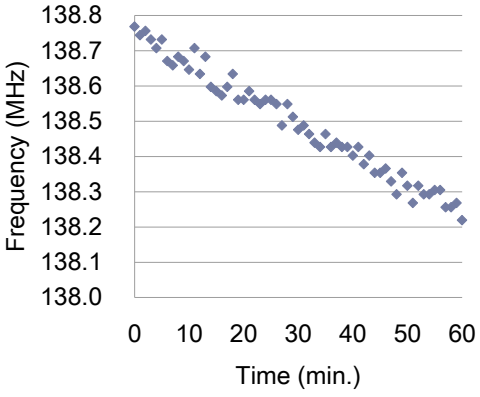


Figure 1 Degradation of Ring Oscillator in 1 Hour

### B. FPGA Structure

Fig. 2 (a) shows a top-level logic structure of Altera Cyclone IV FPGA [25], which was used in our experiment. A FPGA consists of plural logic blocks, which are connected with re-configurable wires with transistor switch boxes. A logic block consists of plural logic array blocks (LABs), each of which includes 16 logic elements (LEs) (Fig. 2 (b)). A LE includes a look-up table (LUT) with 4 input pins and a flip-flop.

Fig. 3 is an example of a logic structure of a LUT. 16 SRAM cells are located on the left side and their outputs are selected by 4-level hierarchical selectors with 4 input control pins. When 4 values of control pins are given, a value of identified SRAM cell will be transferred to the output. For instance, when ($A$, $B$, $C$, $D$) is (0, 1, 1, 0), the value of 7th SRAM is selected as shown in the figure.

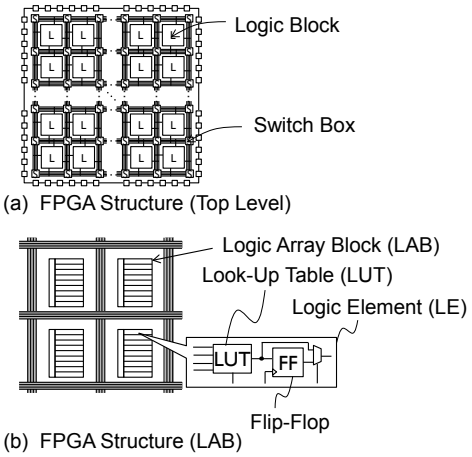


Figure 2 Logic Structure of FPGA

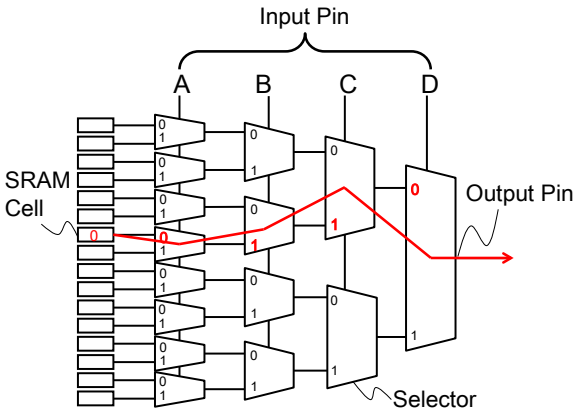


Figure 3 Logic Structure of LUT (Look-Up Table)

### C. Basic Idea

Fig. 4 and 5 show typical circuit implementations of a selector in a LUT. The selector in Fig. 4 is a pair of transmission transistors [53]. When an input value of $A$ is

1, the NMOS transistor will be opened and the PMOS transistor will be closed; consequently, the upper SRAM cell will be selected. When an input value of *A* is 0, the NMOS transistor will be closed and the PMOS transistor will be opened; consequently, the lower SRAM cell will be selected. Therefore, if the input value of *A* is kept at 1, the degradation due to NBTI should be prevented or be reduced very much.

The selector in Fig. 5 consists of a pair of transfer gates [54, 55]. When an input value is 1, the upper gate *G1* will be opened as the value 1 is input to the NMOS transistor of *G1* and the value 0 is input to the PMOS transistor of *G1* through the inverter gate *I1*; consequently, the SRAM cell *S1* will be selected and its value will propagate to the output. When an input value is 0, the lower gate *G2* will be opened as the value 1 is input to the NMOS transistor of *G2* and the value 0 is input to the PMOS transistor of *G2* through the inverter gate *I1*; consequently, the SRAM cell *S2* will be selected and its value will propagate to the output. In both cases, it seems that either PMOS will degrade regardless the input value is 1 or 0; however, the PMOS transistor in the inverter *I1* will degrade when its input value is 0. This concludes that the amount of selector degradation should be larger when the input value is 0 than that when the input value is 1. It is essential that the number of PMOS transistors that are in an on-state is not the same as that when the input values are on the opposite.

As ring oscillator sensing requires only tens of micro seconds, it will be reasonable in many cases to assume that the sensing will be performed at a low frequency and the oscillators will not be working most of the time. This suggests that keeping PMOS transistors in an off-state in non-oscillating time will be effective to reduce NBTI degradation.

In this paper, the selector model in Fig. 4 is used for the explanation of the proposed structure for simplicity; however, the model in Fig. 5 can be easily applied in the same way.

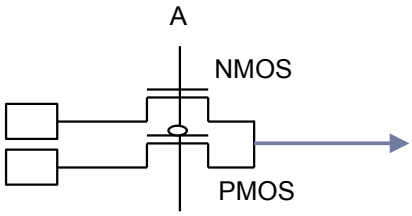


Figure 4 Example of Selector in LUT [53]

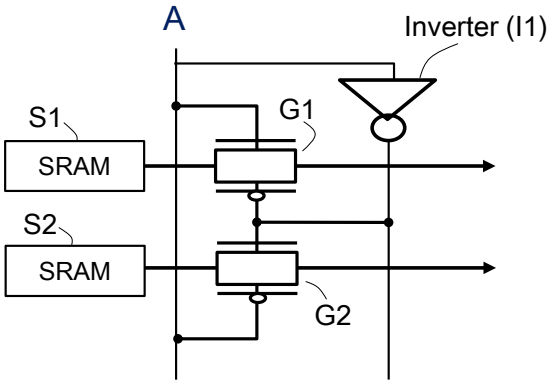


Figure 5 Example of Selector in LUT [54, 55]

## III. PROPOSED STRUCTURE

### A. *Problem of Conventional Ring Oscillator*

A conventional ring oscillator consists of an odd number of inverters in a chain as shown in Fig. 6, where enable signal is input to the first inverter (or an additional AND gate is inserted into a chain). When the enable signal is 1 (an oscillation mode), each output node is at 0/1 alternately (Fig. 6 (a)). As the number of inverter is odd, each LUT will toggle after the first transition has gone round the chain and the ring oscillator will continue to oscillate. When the enable signal is 0 (a sleep mode), each output node will be at 0/1 alternately and be kept stable (Fig. 6 (b)). This means almost the half of gates' outputs will be at 0.

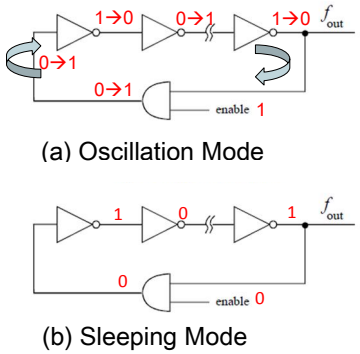


Figure 6 Conventional Ring Oscillator

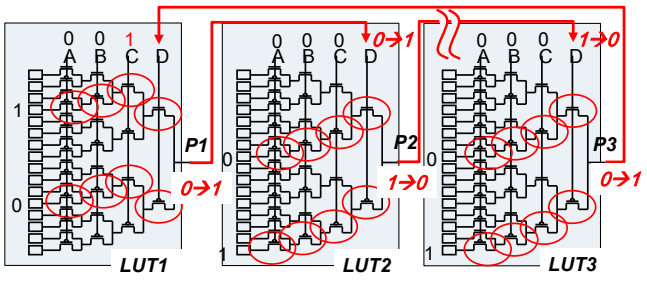


Figure 7 LUT Logic Structure (Oscillation Mode)

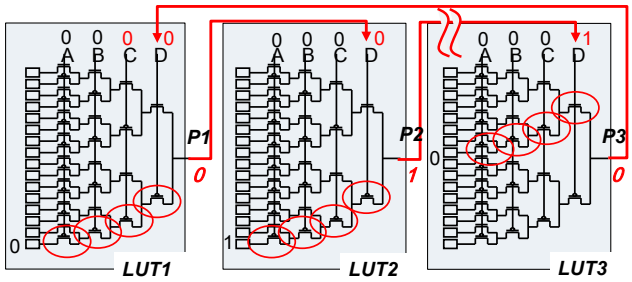


Figure 8 LUT Logic Structure (Sleep Mode)

Fig. 7 and 8 are the corresponding LUT logic structure. Here, LUT1 is combined with the AND gate in Fig. 6. Unused pins (*A* and *B* in LUT1, *A*, *B* and *C* in LUT2 and 3) are set to 0 as defaults. The circles in the figures highlight the selectors that are in an on-state in each mode. In an oscillation mode, pin *D* is assigned as an oscillation pin. The outputs of LUTs (*P1*, *P2* and *P3*) are respectively connected to the oscillation pins of the adjacent LUTs. In Fig. 8, each output node is at 0/1 alternately and is kept stable, and the values of *P1* and *P3* are 0. In a longer chain, almost half of LUTs' outputs will be at 0. This means that PMOS transistors where their gate values are 0 will degrade due to NBTI as described in Section 2.C. In this case, there are 3 or 4 PMOS transistors in each path in a LUT that are related to the oscillation and are in an on-state in a sleep mode.

### *B. Proposed Ring Oscillator*

Fig. 9 shows a proposed structure of a ring oscillator. LUTs consists a chain by connecting each output to the adjacent LUT's pin (for example, pin *A*). The difference from a conventional ring oscillator in Fig. 6 is that the input pins (*B*, *C* and *D*) other than the oscillation pins (*A*) are differently controlled in a sleep mode from that in an oscillation mode so that degradation of PMOS transistors related to the oscillation paths are prevented.

Fig. 10 is an example of LUT design, where pin *B*, *C* and/or *D* are assigned differently in each mode. The circles in the figure highlight selectors that are in an on-state. The input values of (*B*, *C*, *D*) are set to (0, 0, 0) in an oscillation mode (Fig. 10 (a)). As 15$^{th}$ and 16$^{th}$ SRAM cells store the opposite values to the input values at pin *A*, the LUT oscillates. On the other hand, the input values of (*B*, *C*, *D*) are set to (1, 1, 1) in a sleep mode (Fig. 10 (b)). The 1$^{st}$ SRAM value activated in a sleep mode is set to 1 so as it will be the same value of pin *A*. As seen in the figure, all the PMOS transistors in the oscillation path are set to 1 in a sleep mode. Therefore, their degradation will be prevented or be reduced. It should be notified that this is an example and not the only case that satisfies the upper conditions. Some other examples will be demonstrated in Section 4.

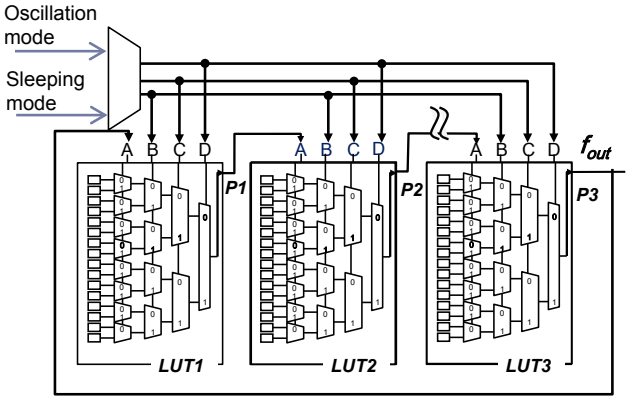


Figure 9 Proposed Ring Oscillator

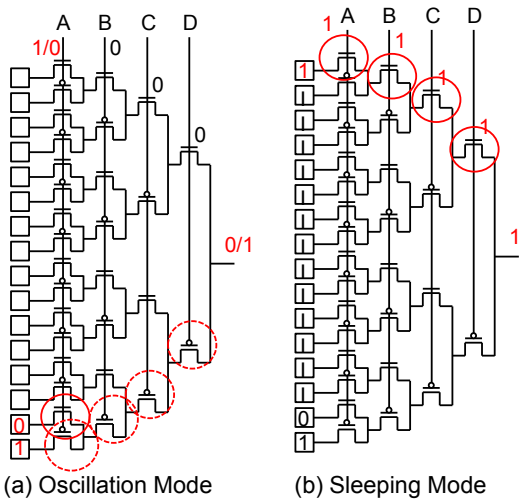


Figure 10 Proposed LUT Design

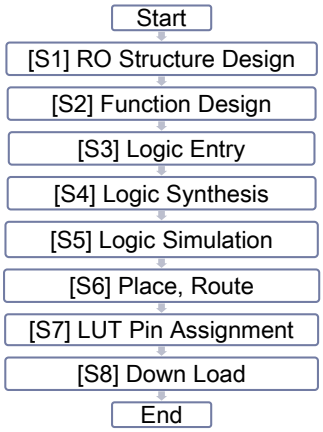


Figure 11 Design Flow

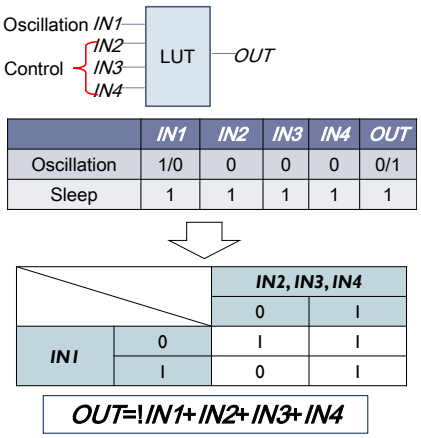


Figure 12 Function Design

### C. Design Flow

Fig. 11 is a design flow for the proposed ring oscillators. The design proceeds as follows:

Step 1 (S1): RO Structure Design.

The structure of a ring oscillator is planned on selector-basis as described in Section 3.B. A logic path in an oscillation mode and a path in a sleep mode are designed with corresponding input values, which make PMOS transistors at off-state in a sleep mode (Fig. 10). The number of LUTs is less than 15 (i.e. more than 1 vacant LUT remaining) so that all LUTs will be placed in a LAB without global wirings in a later step.

Step 2 (S2): Function Design.

The logic function that satisfies the function designed in Step 1 is decided using Karnaugh map (Fig. 12). In Fig. 9, the function will be *OUT*=!*IN1*+*IN2*+*IN3*+*IN4*, where !*OUT* is an inverse of *OUT*. It should be noted that a pin assignment of LUT cannot be specified at this design step, and only its function is specified.

Step 3 (S3): Logic Entry.

A RTL description of the ring oscillator designed in Step 2 is written in Verilog-HDL code. (Non-reduction option is specified so that the original LUTs are remained after compilation.) Then, it is compiled and simulated (Quartus™ and Modelsim™ were used).

Step 4 (S4): Logic Synthesis.

Step 5 (S5): Logic Simulation.

Step 6 (S6): Place, Route.

Before executing placement and routing, specify an option so that all the LUTs are placed in a LAB, and serial placement order of LUTs in a LAB (Fig. 13). Then, automated placement and routing are performed.

Step 7 (S7): LUT Pin Assignment

As only function of LUT was specified in Step 2, assign the correspondence between functional and physical pins. This procedure is executed manually using GUI interface of Quartus™ so that the result will be the same as Fig. 10.

Step 8 (S8): Down Load.

The result of Step 7 is written (downloaded) in FPGA and executed.

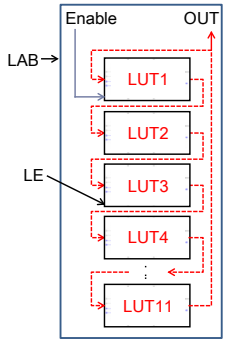


Figure 13 LUT placements in a LAB

## IV. Experimental Result

### A. Ring Oscillator Menu

7 types of ring oscillators in Table I were designed for the experiment. Each one intended to have different sensitivity for NBTI or PBTI. The first column shows a name of ring oscillator types, the second column is an operation mode of a ring oscillator, and the third column shows pin assignments. For instance, in RO_4, "*P*/*N*" of pin *A* in an oscillation mode means that the pin is used as an oscillation input and its value is 0 (PMOS selector) or 1 (NMOS selector) respectively. Other pins' values "*P*" in an oscillation mode means that their values are 0 (PMOS selector). Their "*N*" in a sleep mode means that their values are 1 (NMOS selector). The fourth column ("#of Degrade") shows a number of cases where PMOS selectors or NMOS selectors share an on-state between in an oscillation mode and in a sleep mode. In RO_4, no PMOS selectors at pin *B*, *C* or *D,* are in an on-state both in an oscillation mode and in a sleep mode, but a NMOS selector at pin *A* will be a chance to be in an on-state. The last column shows the function of the ring oscillator by the description of pin assignments.

As described in Section 3.2, "# of Degrade" of PMOS indicates the number of PMOS selectors that might degrade by NBTI. In the same way, "# of Degrade" of NMOS indicates the number of NMOS selectors that might degrade by PBTI. Therefore, Table I shows that a variety of degradation levels are prepared for the experiment. RO_7 is a ring oscillator generated from an inverter chain in Verilog-HDL with a specification of placing all LUTs in a LAB. This one corresponds to a conventional ring oscillator. Checking the LUT pin

assignment, it was known that 2 oscillation pins are assigned to pin C, and others are assigned to pin *D*.

TABLE I. RING OSCILLATOR MENU

| Type | Mode | Pin Assign | | | | # of Degrade | | Function |
|---|---|---|---|---|---|---|---|---|
| | | *A* | *B* | *C* | *D* | PMOS | NMOS | |
| RO_1 | Osc. | P | ***P*** | ***P*** | ***P/N*** | 3 | 0 | *F=!A!B!C!D* |
| | Sleep | N | ***P*** | ***P*** | ***P*** | | | |
| RO_2 | Osc. | N | ***N*** | ***N*** | ***P/N*** | 0 | 3 | *F=!(ABCD)* |
| | Sleep | P | ***N*** | ***N*** | ***N*** | | | |
| RO_3 | Osc. | ***P/N*** | P | ***P*** | ***P*** | 3 | 0 | *F=!(A+B+C+D)* |
| | Sleep | ***P*** | N | ***P*** | ***P*** | | | |
| RO_4 | Osc. | ***P/N*** | P | P | P | 0 | 1 | *F=!A+B+C+D* |
| | Sleep | ***N*** | N | N | N | | | |
| RO_5 | Osc. | ***P/N*** | N | ***N*** | ***N*** | 0 | 3 | *F=!(ABCD)* |
| | Sleep | ***N*** | P | ***N*** | ***N*** | | | |
| RO_6 | Osc. | ***P/N*** | N | N | N | 1 | 0 | *F=!A(BCD)* |
| | Sleep | ***P*** | P | P | P | | | |
| RO_7 | Osc. | * | * | ***(P/N)*** | ***P/N*** | 0.5 | 0.5 | *F=!IN* |
| | Sleep | * | * | ***(P/N)*** | ***P/N*** | | | |

## B. *Experimental Setup*

Trasic DE2-115 development board with Altera Cyclone IV (60nm technology) was used for the experiment. A set of 7 ring oscillators in Table I were placed at two locations on a FPGA, and the board had been set into an Espec SU-241 constant temperature reservoir. It was powered on and was heated at 85 ℃ in day time (nearly 8hours). It was powered off at night for seeing NBTI recovery feature and also for a safety reason (nearly 16 hours). The frequency of the ring oscillators were measured at every minute when the FPGA is powered on. The oscillators operated for 85 $\mu$ seconds in each oscillation mode. The measurement was performed keeping the other circuit quiet to reduce power/ground noise.

## C. *Degradation Ratio*

Fig. 14 shows the frequency degradation ratio of each ring oscillator. The powered on time is plotted on X-axis. Degradation ratio is plotted on Y-axis. The moving average of successive 21 measured values are plotted to reduce randomness in measurement. As seen in the figure, the degradation speed differs very much according the structure of each ring oscillator. It is rather fast at an early stage and gradually become slower as described in literatures [19-23]. It is also seen that degradation recovers somewhat but not all during the powered-off times.

Table Π shows the initial frequency of each oscillator in the meaning of moving average, and the last 21th average degradation ratio. The last column is the order that shows smaller degradation. It shows that RO_4 is the best ring oscillator with the smallest degradation, and RO_2 and RO_5 follow it. RO_2, 4 and 5 are ring oscillators that have 0 degrading PMOS selectors as shown in Table I. The worst is RO_1 or 3, which has the most number of degrading PMOS selectors in Table I. The conventional ring oscillator RO_7 is located in the middle. RO_4 shows 37% reduction to RO_7 (conventional ring oscillator), and 51% to RO_1 and 3 (the worst ones).

There are several discussions.

1. RO_4 is the best: however, it still shows 0.156% degradation. There is possibility that the selector structure might not be Fig. 4 but might be something like Fig. 5, which shows some amount of NBTI degradation for both input values, and/or other degradations such as PBTI and HCI are not negligible.

2. RO_2 and RO_5 also have 0 degrading PMOS selectors, but their degradation ratio is worse than RO_4. The difference is they have 3 degrading NMOS selectors (i.e. NMOS selectors are in an on-state during a sleep mode). This indicates that there is some NMOS-induced degradation such as PBTI.

3. The oscillation pin is *D* in RO_2 and *A* in RO_5. Therefore, their frequencies are quite different, and the degradation ratio is worse in RO_2 than in RO_5.

4. RO_1 and RO_3 are the worst. The oscillation pin is *D* in RO_1 and *A* in RO_3. Therefore, their frequencies are quite different, but the degradation ratio is almost the same.

These are not big amount of differences, but Fig. 14 shows that these features are very steady. More detail experiments including reduction of measuring noise is remained for future work.

TABLE II. COMPARISON OF DEGRADATION

| Type | Initial Frequency (MHz) | Last 20th Ave. Degradation Ratio (%) | Reduction Ratio to Best (RO_5) | Order |
|---|---|---|---|---|
| RO_1 | 168 | -0.235% | 1.51 | 6 |
| RO_2 | 156 | -0.205% | 1.31 | 3 |
| RO_3 | 91 | -0.236% | 1.51 | 7 |
| RO_4 | 90 | -0.156% | 1 | 1 |
| RO_5 | 87 | -0.167% | 1.07 | 2 |
| RO_6 | 95 | -0.217% | 1.39 | 5 |
| RO_7 | 107 | -0.213% | 1.37 | 4 |

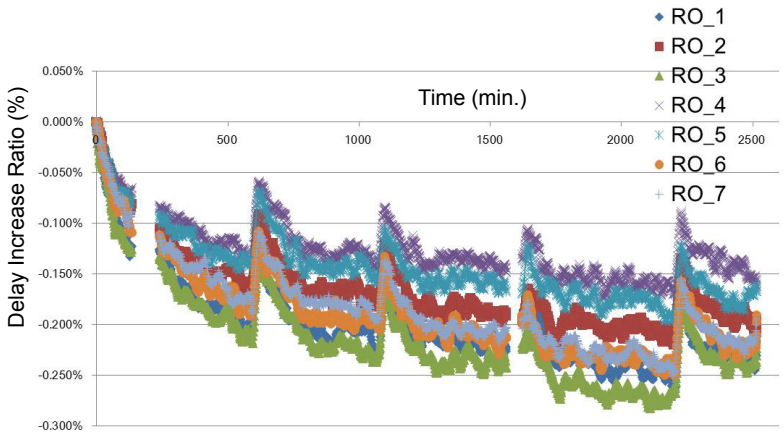


Figure 14 Frequency Degradation of 7 Ring Oscillators

### D. *Numerical Analysis*

A multiple regression technique was applied to analyze the contribution of parameters that define the ring oscillators' structure. As the number of sample ring oscillators is 7, it is required that the structures should be defined with smallest parameters less than 7.

Table III is a data for a multiple regression. The table shows names of ring oscillators in the 1st column, degradation ratios in the 2nd column, properties (parameters) of ring oscillators in 3rd, 4th, 5th and 6th columns, respectively. These 4 properties are defined as follows:

"*Osc. Sel.*" = 1: Oscillation pin is 0 in a sleep mode,

"*Osc. Sel.*" = 0: Oscillation pin is 1 in a sleep mode,

"*Osc. Loc.*" = 1: Oscillation pin uses pin *D* (output-side).

"*Osc. Loc.*" = 0: Oscillation pin uses pin *A* (SRAM-side).

"*Deg. P-Sel.*" = 1: A number of *P*-selectors that degrade in a sleep mode other than the oscillation pin.

"*Deg. N-Sel.*" = 1: A number of *N*-selectors that degrade in a sleep mode other than the oscillation pin.

A multiple regression (i.e. least squares method) was performed where *Deg. Ratio* is an objective variable, and 4 parameters are descriptive variables. Equation (1) shows the extracted relationship between the degradation ratio and 4 properties. The multiple-correlation coefficient was 0.96641, which proofs strong relationship. Table IV is the errors of estimation using Equation (1).

$$Deg.Ratio = 0.155 + 0.064 \times Osc.Sel + 0.018 \times Osc.Loc + 0.003 \times Deg.P\_Sel + 0.011 \times Deg.N\_Sel \quad (1)$$

Equation (1) shows that the minimum degradation is 0.155. The degradation of the oscillation pin affects mostly the ring oscillator's degradation. The case in which the oscillation pin used pin *D* shows larger degradation than the case of pin *A*. This might be because the degradation ratio when pin A is used for an oscillation will be alleviated by the other delays on selector *B*, *C* and *D*. Degradation on the other P/N selectors other than the oscillation pin also affects the ring oscillator's degradation although their effects are smaller than the oscillation pin's. The fact that the number of *N*-selectors affects the degradation ratio indicates that some degradation phenomena other than NBTI might also exist. Although the physical analysis was not performed, the experiment shows the controllability and reduction of degradation.

TABLE III. DATA FOR MULTIPLE REGRESSION

| *Ring Osc.* | *Deg. Ratio* (%) | RO. Property | | | |
|---|---|---|---|---|---|
| | | *Osc. Sel.* | *Osc. Loc.* | *Deg. P-Sel.* | *Deg. N-Sel.* |
| RO1 | 0.235 | 1 | 1 | 2 | 0 |
| RO2 | 0.205 | 0 | 1 | 0 | 2 |
| RO3 | 0.236 | 1 | 0 | 2 | 0 |
| RO4 | 0.156 | 0 | 0 | 0 | 0 |
| RO5 | 0.167 | 0 | 0 | 0 | 2 |
| RO6 | 0.217 | 1 | 0 | 0 | 0 |
| RO7 | 0.213 | 0.5 | 1 | 3 | 0 |

TABLE IV. ERROR OF ESTIMATION

| RO No. | Estimation (%) | Error (%) | Standard Error |
|---|---|---|---|
| 1 | 0.2433 | -0.0083 | -1.023 |
| 2 | 0.1950 | 0.0100 | 1.235 |
| 3 | 0.2252 | 0.0108 | 1.341 |
| 4 | 0.1551 | 0.0009 | 0.106 |
| 5 | 0.1770 | -0.0100 | -1.235 |
| 6 | 0.2187 | -0.0017 | -0.212 |
| 7 | 0.2147 | -0.0017 | -0.212 |

## V. CONCLUSIONS

An aging-tolerant design structure for ring oscillators that reduces NBTI-induced degradation on FPGA is introduced. The structure is able to reduce NBTI-induced degradation in a ring oscillator's frequency by setting PMOS transistors of look-up tables in an off-state during the oscillators are not working. The proposed ring oscillator shows 37% reduction to the conventional ring oscillator, and 51% to the worst structure. The main cause of degradation will be NBTI; however, the data indicates that there might be other mechanism of degradation such as PBTI. The experimental evaluation of a variety of ring oscillators using Altera Cyclone IV device (60nm technology) shows that the proposed structure achieves controlling degradation level as well as reducing performance degradation. The numerical analysis has shown each property's effect on a ring oscillator's degradation. The proposed method will contribute to enhancing reliability and also to analyzing degradation mechanism.

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