Low-Temperature Carrier Transport in Ionic-Liquid-Gated Hydrogen-Terminated Silicon

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We fabricated ionic-liquid-gated field-effect transistors on the hydrogen-terminated (111)-oriented surface of undoped silicon. Ion implantation underneath electrodes leads to good ohmic contacts, which persist at low temperatures down to 1.4 K. The sheet resistance of the channel decreases by more than five orders of magnitude as the gate voltage is changed from 0 to -1.6 V at 220 K. This is caused by the accumulation of hole carriers. The sheet resistance shows thermally activated behavior at temperatures below 10 K, which is attributed to hopping transport of the carriers. The activation energy decreases towards zero with increasing carrier density, suggesting the approach to an insulator-metal transition. We also report the variation of device characteristics induced by repeated sweeps of the gate voltage.

1. Introduction

The electric field effect is a central basis for semiconductor electronics. Field-effect transistors act as an electrical switch and are a fundamental component of memories and processors. Recently, growing interest has been focused on the electric field control of high carrier densities such that it leads to a considerable change in the properties of the channel material, including its phase transition. This is because it will be applicable to novel electronic devices with low power consumption and high performance. Such control of high carrier densities has often been performed using electric double-layer transistors (EDLTs), which use an ionic liquid as a gate dielectric. It is possible to control the carrier density to over 10^{14} cm^{-2}

($\approx 10^{21}$ cm^{-3}) due to the formation of an electric double layer on the channel surface.[1,2] Electric-field-induced superconductivity[3,4] and ferromagnetism[5] have been reported using this EDLT technique.

Silicon, the most widely used semiconductor, becomes metallic by doping boron with concentration higher than 4×10^{18} cm^{-3}.[6] It also shows superconductivity at low temperatures at a boron concentration higher than 3×10^{21} cm^{-3}.[7] It is of great interest whether such phase transitions can be induced by electric field effects. A superconducting switch compatible with the current semiconductor industry will provide a wide range of applications. There have been many studies of EDLTs on layered compounds such as MoS_2[8] and organic molecular crystals such as rubrene[9] and pentacene[10,11]. In contrast to these systems, silicon is a three-dimensional crystal with covalent bonds and its clean surface has dangling bonds. Passivation of these dangling bonds is required for the fabrication of EDLTs because dangling bonds lead to surface states and prevent the accumulation of carriers. Hydrogen termination is suitable for such passivation since hydrogen-terminated silicon has an atomically controlled surface[12] and chemical stability[13]. There have been reports about EDLTs on hydrogen-terminated silicon[14-17], but their low-temperature characteristics were not reported. In the case of diamond, which is also a covalently bonded crystal, EDLTs on a hydrogen-terminated surface have been fabricated and the accumulation of high-density carriers[18] close to the critical density for the occurrence of superconductivity[19] has been demonstrated. Shubnikov–de Haas oscillations[20] and anomalous magnetoresistance effects[21] have also been reported for EDLTs on hydrogen-terminated diamond at low temperatures. Recently, silicon EDLTs with silicon dioxide as a passivation layer were also fabricated and low-temperature transport properties were studied.[22] However, the oxide layer may reduce the surface capacitance. In addition, EDLTs on (111)-oriented silicon were reported not to work[22].

In our previous study, we fabricated EDLTs on (111)-oriented hydrogen-terminated silicon and successfully controlled the carrier density at the channel.[23] However, the contact resistance between the electrodes and channel was significantly large at low temperatures (> 5 GΩ), which hampered accurate measurement of the electric resistance and Hall coefficient. In this study, we have reduced the contact resistance by more than four orders of magnitude by boron implantation underneath the electrodes. This enabled us to measure the temperature dependences of the electric resistance, Hall carrier density, and Hall mobility accurately and discuss low-temperature carrier transport in detail. The temperature dependence of the resistance showed that the low-temperature transport was governed by thermally activated hopping conduction.

2. Experimental Details

We fabricated EDLTs on undoped (111)-oriented silicon substrates (≥ 1000 Ωcm). The device fabrication process is as follows. (1) SiO_2 was grown on the surface of a substrate to prevent the channel from contamination during ion-implantation and activation-annealing processes. (2) The substrate was covered with resist (AZ-5214E) except for the region where the electrodes were fabricated. Boron ions were implanted into the substrate using ion-implantation equipment. After the removal of the resist, the substrate was annealed at 1000°C for 1 s in an Ar atmosphere to activate the boron ions. (3) A Ti/Pt film was deposited on the substrate and annealed at 500°C for 5 min in an Ar atmosphere to produce ohmic electrodes. (4) A SiO_2 insulating film was deposited to insulate the substrate electrically from the gate electrode and bonding pads fabricated in the next process. (5) A Ti/Au film was

deposited as a gate electrode and bonding pads. (6) The surface of the device was covered with a SiO_2 insulating film except for the channel, the gate electrode, and the bonding pads to accumulate carriers on the channel efficiently. Figure 1 shows an optical microscope image of the substrate after process (6). (7) The substrate was covered with resist (AZ-5214E) except for the channel. The substrate was dipped in buffered hydrofluoric acid (NH_4F:HF = 50:1) for 5 min to remove the natural oxide film on the channel and to make the channel hydrogen-terminated. After that, the resist was removed. To make the channel clean, the substrate was dipped in dilute hydrofluoric acid [H_2O:HF(46%) = 80:1] for 30 s. (8) The ionic liquid DEME-TFSI [*N*, *N*-diethyl-*N*-methyl-*N*-(2-methoxyethyl)ammonium bis(trifluoromethanesulfonyl)imide] was applied on the channel and the gate electrode in an Ar-filled glove box, which completes the fabrication process of the Si EDLT. The ionic liquid was dried using a turbomolecular pump before use. The sample holder was sealed in an Ar atmosphere using indium wire.

The measurement was performed in a refrigerator with a superconducting magnet. The resistance and Hall coefficient were measured using a current preamplifier (DL Instruments 1211) and a voltage preamplifier (DL Instruments 1201). In the Hall coefficient measurements, the magnetic field was swept between -2 and 2 T. The temperature was controlled between 300 and 1.4 K using a temperature controller (Cryocon 44C). In the measurement of the temperature dependence of the resistance, the electrodes except for the

gate electrode were grounded at temperatures around the freezing point of the ionic liquid (170 – 220 K) to prevent the distribution of ions in the ionic liquid from changing due to the in-plane electric field.

3. Results and Discussion

Figure 2(a) shows the gate voltage dependence of the sheet resistance of the Si EDLT at 220 K. The resistance at zero gate voltage is two orders of magnitude higher than that observed in our previous study[23], which may be related to the improved cleaning process in device fabrication. When a negative voltage is applied, the resistance decreases by more than five orders of magnitude. This is caused by the accumulation of hole carriers in the channel, as shown below. The minimum sheet resistance induced by the field effect is nearly the same as that observed in the previous study[23], which indicates no significant degradation of the channel due to the boron ion implantation. Figure 2(b) shows the gate voltage dependence of the sheet conductance of the Si EDLT at 220 K. The conductance shows a maximum at $V_g \approx$ -1.6 V. This maximum conductance is related to the maximum sheet carrier density obtained from the Hall measurement. Figure 2(c) shows the gate voltage dependence of the Hall sheet carrier density of the Si EDLT at 220 K. The sign of the Hall coefficient indicates that the carriers are holes. When a negative gate voltage is applied, the sheet carrier density increases at $V_g >$ -1.6 V. The interface capacitance estimated from the maximum slope is 0.67 $\mu F/cm^2$ as shown by a blue line. The maximum Hall sheet carrier density reaches 4×10^{12} cm^{-2}. The average depth of accumulated holes from the surface for this sheet carrier density is estimated to be 2 nm from the Fang–Howard approximation.[24,25] Therefore, the volume carrier density is estimated to be $\approx2\times10^{19}$ cm^{-3}. This value is comparable to the critical carrier density for the insulator-metal transition of boron-doped silicon[6]. At $V_g <$ -1.6 V, the sheet carrier density

decreases with increasing negative gate voltage, which is attributed to the increase in the density of surface states due to an electrochemical reaction. Figure 2(d) shows the gate voltage dependence of the Hall mobility at 220 K. The mobility at a low gate voltage is higher than that observed in the previous study. This indicates better quality of the hydrogen-terminated surface, probably due to the improved cleaning process. The decrease in the mobility with increasing gate voltage is attributed to the enhancement of acoustic phonon scattering with increasing carrier density[26].

Figure 3 shows the gate voltage dependence of the sheet conductance of the Si EDLT measured while sweeping the gate voltage repeatedly at 220 K. First, a negative gate voltage was applied from 0 to -2.4 V. The Hall measurements were performed at different gate voltages with an increment of 0.2 V during this first sweep [Fig. 2(c) and 2(d)]. After that, the gate voltage was swept back to 0 V. Then, the gate voltage was again swept to -2.4 V and back to 0 V. Then, the gate voltage was swept to -3 V and back to 0 V. Similar sequences were carried out for higher gate voltages. As the maximum gate voltage increases, the sheet conductance–gate voltage curve is shifted in the negative gate voltage direction and the maximum sheet conductance decreases. This behavior is attributed to the increase in the density of surface states with increasing maximum applied gate voltage due to an electrochemical reaction. As the gate voltage is increased, charges first fill the surface states. These trapped charges do not contribute to the electrical conduction, and therefore, the sheet conductance does not change. After the surface states are filled, the charges that contribute to the conduction start to accumulate, which leads to an increase in the sheet conductance. The larger the density of surface states, the larger the voltage required to introduce the conductive charges. When a larger gate voltage is applied, the sheet conductance decreases again due to the increase in the density of surface states caused by the electrochemical reaction. Once these surface states are created, the maximum carrier density in the previous gate voltage sweep is

not obtained again.

Note that the gate voltage dependence of the sheet conductance for a pristine sample was nearly reversible for -1 V < V_g < 0 V. Therefore, the electrochemical reaction is weak in this regime, and it becomes stronger at higher gate voltages. This is also consistent with the observation that the gate leakage current is noticeable (on the order of a few tens of nA) at V_g < -1 V. Note also that the capacitance value shown above is slightly lower than 0.86 μF/cm^2 obtained in the previous study. This is probably because the voltage range in this study is slightly larger than that in the previous study and the effect of the electrochemical reaction may be larger. The capacitance value is also smaller than ~1.3 μF/cm^2 estimated from an impedance spectroscopy measurement[27]. This is probably due to the fact the capacitance in our study is estimated from the Hall carrier density and the charges trapped in the surface states do not contribute to the capacitance value.

Figure 4 shows the temperature dependence of sheet resistance of the Si EDLT at T > 1.4 K at different gate voltages. The applied gate voltage is incrementally changed from 0 to -2.4 V at 220 K. At V_g = 0 V, the sheet resistance increases rapidly with decreasing temperature. This indicates that the ungated Si channel is insulating. When V_g = -1.6 V is applied, the increase in the sheet resistance is suppressed at temperatures above 10 K. Below 10 K, however, the sheet resistance increases rapidly for all gate voltages. Note that the current-voltage characteristics measured with the two-point configuration are linear at temperatures down to 1.4 K. The zero-bias resistance value (e.g., 530 kΩ for V_g = -1.6 V at 4 K) obtained from the current-voltage characteristics is also much smaller than that (> 5 GΩ) in the previous study. These observations indicate that the ion implantation beneath the electrode yields good electrical contacts even at low temperatures. Figure 5(a) shows the temperature dependence of the Hall sheet carrier density. At V_g = -0.4 V, the Hall sheet carrier density decreases by more than four orders of magnitude. At V_g = -1.6 V, however, the

decrease in the Hall sheet carrier density at low temperatures is suppressed. Figure 5(b) shows the temperature dependence of the Hall mobility. Above 100 K, the Hall mobility increases with decreasing temperature since the phonon scattering is suppressed. Below 50 K, the Hall sheet carrier density increases and the Hall mobility decreases by more than one order of magnitude. This may be caused by hopping conduction at low temperatures. Figure 6(a) shows the sheet resistance of the Si EDLT as a function of inverse temperature. The data are on straight lines in the Arrhenius plot at low temperatures, which indicates thermally activated transport. At low temperatures, carriers induced by ionic-liquid gating are localized by an inhomogeneous Coulomb potential caused by anions in the ionic liquid accumulating near the Si channel. The thermally activated transport at low temperatures is attributed to the hopping conduction of carriers between the localized states. The prefactor σ_0 of the activated transport, $\sigma = \sigma_0 \exp(-\varepsilon/k_B T)$, is almost the same for V_g = -0.8, -1.2, and -1.6 V, but it decreases for V_g = -2.0 and -2.4 V, as shown by the ordinate intercepts of the solid lines in Fig. 6(a). The decrease in σ_0 may be related to the increase in the density of surface states. The activation energy can be determined from the slope in Fig. 6(a). Figure 6(b) shows the activation energy plotted as a function of the square root of the Hall sheet carrier density at 50 K. The activation energy decreases towards zero with increasing Hall sheet carrier density. A similar decrease in the activation energy was also observed in a Si MOSFET[26] and an oxide-film-passivated Si EDLT[28]. The decrease in the activation energy is caused by the overlap of the wave functions of the localized states, which eventually leads to an insulator-metal transition. Figure 6(b) thus indicates the approach to an insulator-metal transition in the hydrogen-terminated silicon.

4. Conclusions

We fabricated a Si EDLT in which boron ions were implanted underneath Hall bar

electrodes. The application of a negative gate voltage leads to the accumulation of hole carriers and a decrease in sheet resistance by more than five orders of magnitude at 220 K. Repeated sweeps of the gate voltage shift the threshold voltage for carrier accumulation to more negative values. This behavior is ascribed to the increase in the density of surface states due to an electrochemical reaction at $V_g < -1$ V. The current-voltage characteristics measured with the two-point configuration are linear and show a small zero-bias resistance at temperatures down to 1.4 K. This indicates a good electrical contact and allows us to obtain detailed low-temperature transport properties. The sheet resistance of the Si EDLTs measured with the four-point configuration shows thermally activated behavior at temperatures below 10 K. This is attributed to the hopping transport of carriers between localized states, caused by the inhomogeneous Coulomb potential of anions at the channel surface. The activation energy decreases towards zero with increasing carrier density, which indicates the approach to an insulator-metal transition in the hydrogen-terminated silicon.

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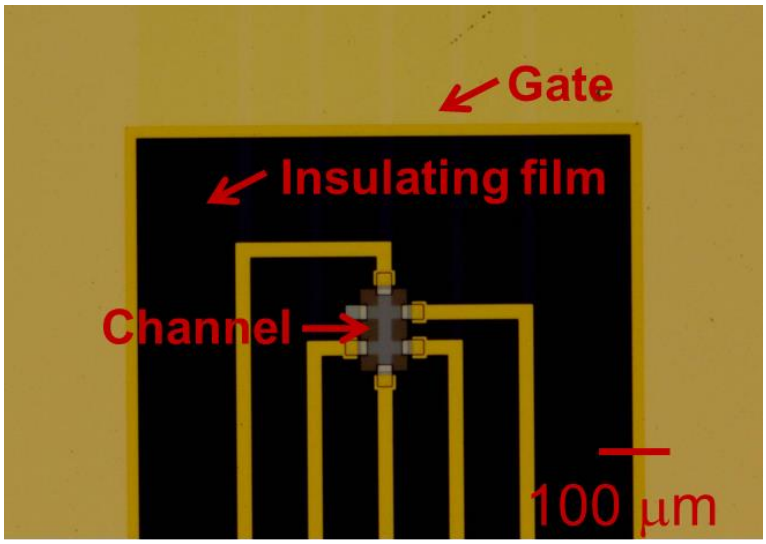

Fig. 1. (Color online) Optical microscope image of a silicon EDLT before the hydrogenation of the channel and the application of ionic liquid.

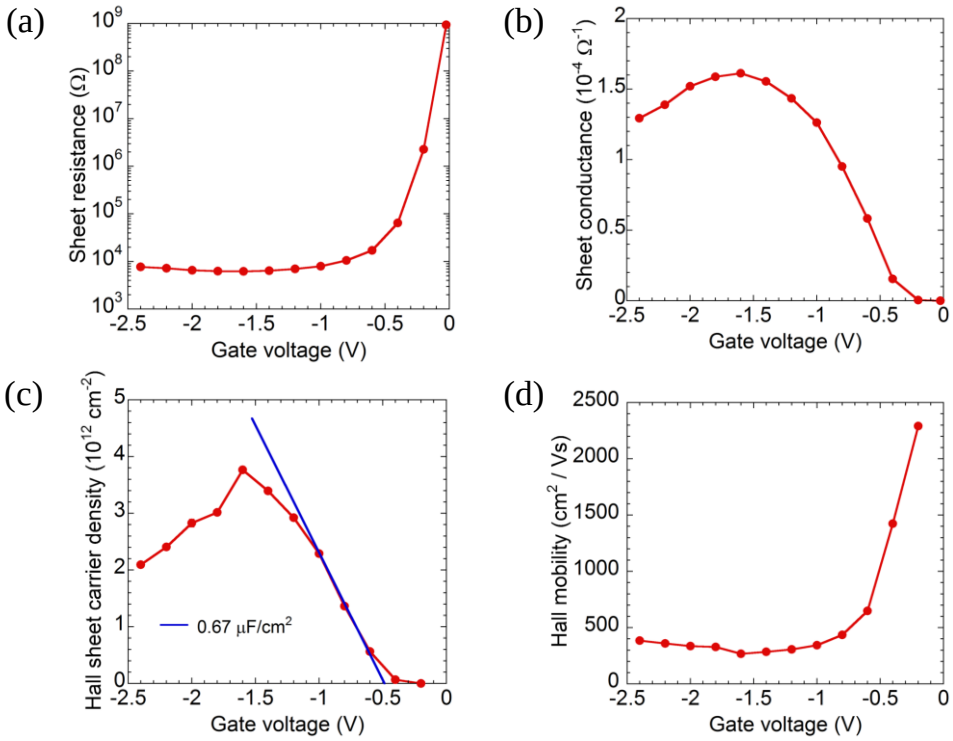

Fig. 2. (Color online) Gate voltage dependences of sheet resistance (a), sheet conductance (b), Hall sheet carrier density (c), and Hall mobility (d) at 220 K.

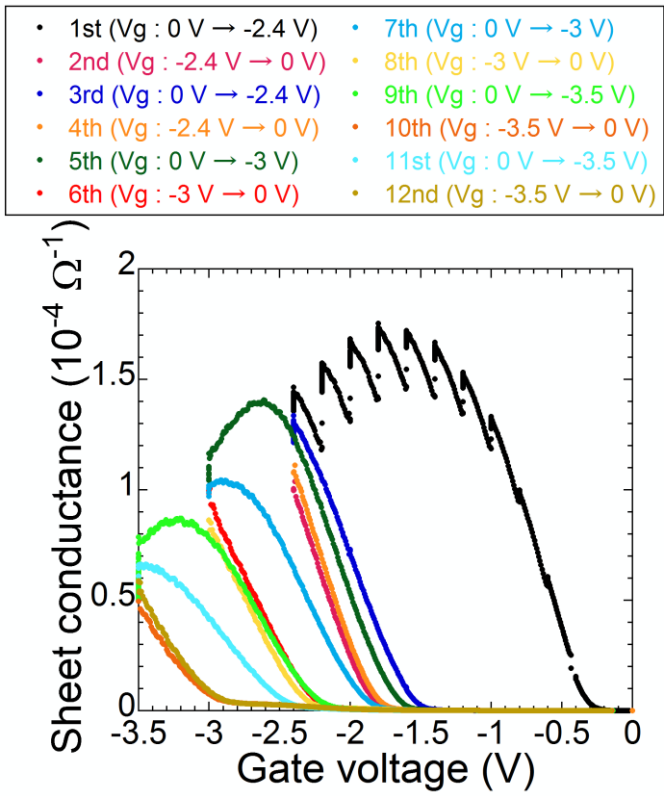

Fig. 3. (Color online) Gate voltage dependence of sheet conductance at 220 K measured while sweeping gate voltage repeatedly.

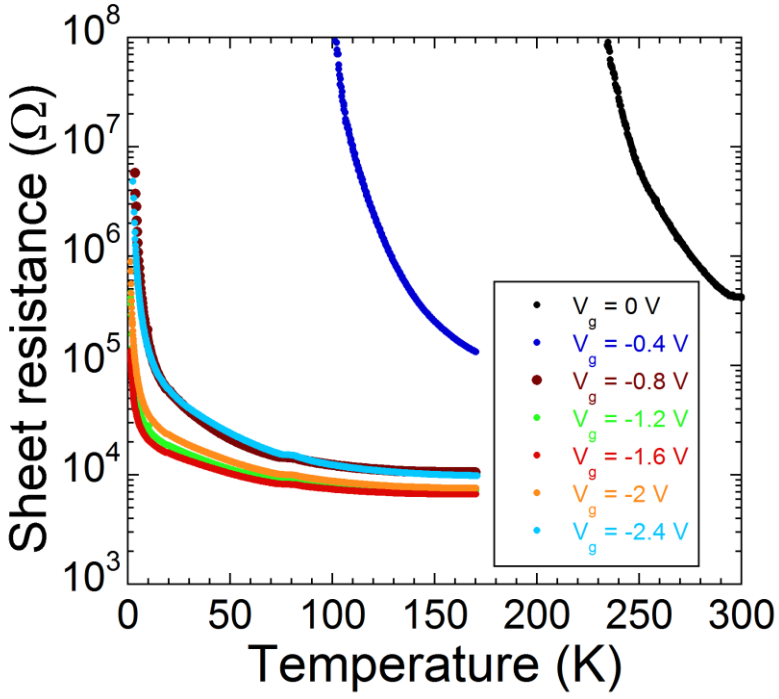

Fig. 4. (Color online) Temperature dependence of sheet resistance at different gate voltages.

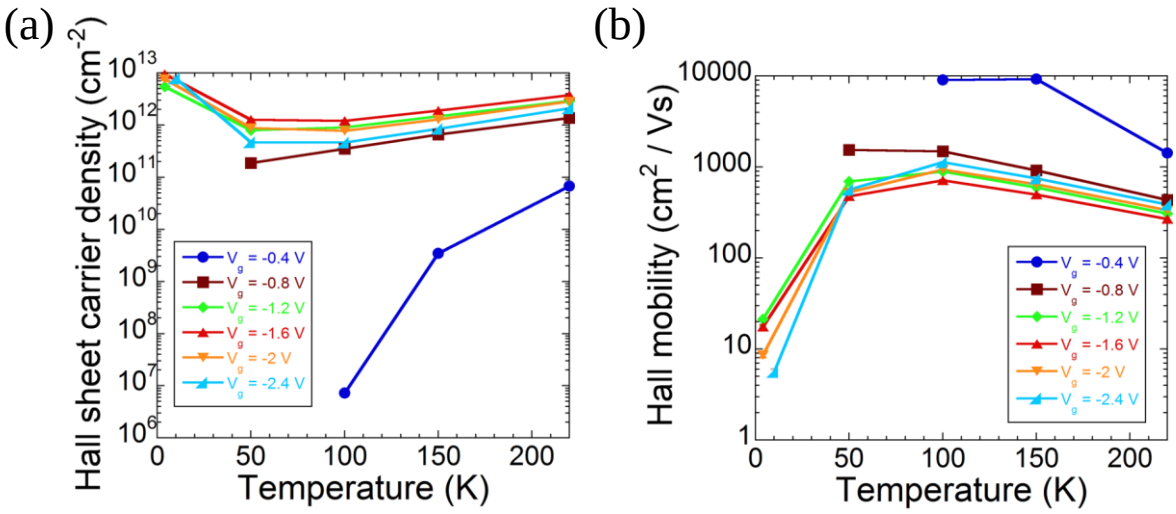

Fig. 5. (Color online) Temperature dependences of Hall sheet carrier density (a) and Hall mobility (b) at different gate voltages.

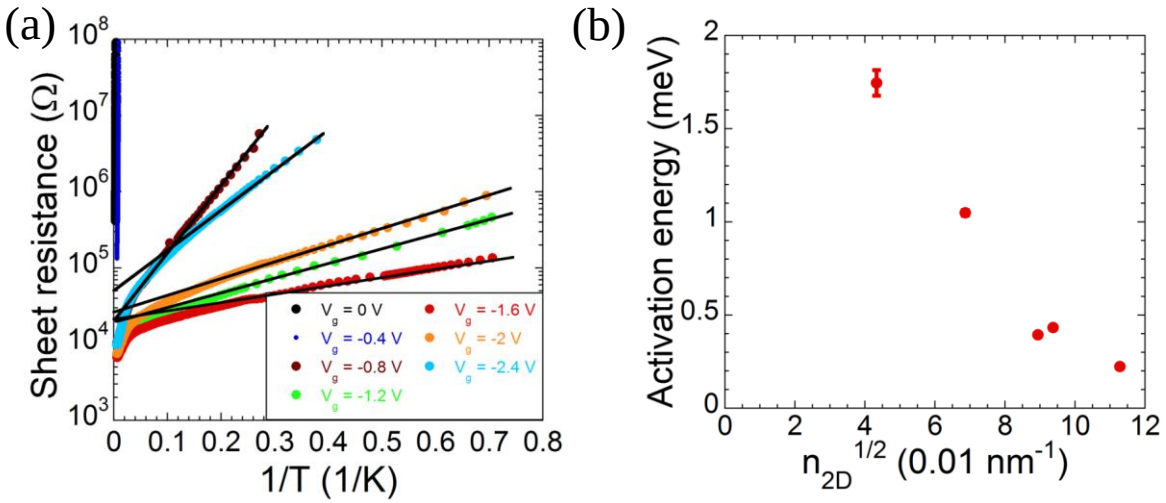

Fig. 6. (Color online) (a) Sheet resistance plotted as a function of inverse temperature at different gate voltages and (b) activation energy plotted as a function of square root of Hall sheet carrier density at 50 K.