High-performance vertical Si PiN diode by hole remaining mechanism

Masanori Tsukuda[a,b], Akiyoshi Baba[c], Yuji Shiba[b] and Ichiro Omura[b]

[a] *Advanced Power Devices Laboratory, Green Electronics Research Institute, 1-8 Hibikino, Wakamatsu-ku, Kitakyushu-shi, Fukuoka, Japan*
[b] *Next Generation Power Electronics Research Center, Kyushu Institute of Technology, 1-1 Sensui-cho, Tobata-ku, Kitakyushu-shi, Fukuoka, Japan*
[c] *Center for Microelectronic Systems, Kyushu Institute of Technology, 680-4 Kawazu, Iizuka-shi, Fukuoka, Japan*

Corresponding author: tsukuda@grik.jp

Abstract

A novel diode with a unique trench shape is predicted by TCAD simulation to have high performance. The novel 600 V vertical PiN diode with hole pockets by the Bosch deep trench process shows a better trade-off curve between reverse recovery loss and forward voltage. The reverse recovery loss is reduced by half. In addition, the active chip size of the novel diode is reduced to two-thirds that of the conventional PiN diode in the same forward voltage. Thanks to the hole pockets with an electric field in the diagonal direction, the remaining hole suppresses the surge voltage with noise for high performance. The novel diode structure is a strong candidate when developing the fabrication process after silicon trench etching is established.

1. Introduction: Requirement for the diode and the purpose of this study

Power semiconductor devices such as diodes, IGBTs and power MOSFETs are widely applied to various power electronics products, such as electric home appliances, hybrid electric vehicles, trains, and wind power generators. Therefore, further efficiency improvement and the prevalence of power electronics products are key factors for efficient energy usage in our more electric-oriented society [1]. For these key factors, reverse recovery loss reduction (fast reverse recovery) and low cost are required for the diodes in power electronics products. To meet these demands, remarkable progress in developing diodes has been made in recent decades and many technologies have been studied to enable next-generation power electronics.

The market of power semiconductor devices continues to grow (see Fig. 1). In the market, silicon power devices are mainly supplied in collaboration with SiC and GaN devices because silicon power devices are superior to wide-bandgap power devices in terms of low cost by mass production technology with large silicon ingots [2]. Consequently, silicon power devices are expected to have more than 90% of the market share for the next ten years [3]. However, it was believed that the physical properties of silicon make it difficult to further reduce reverse recovery loss. To overcome the limitations of this silicon device, many researchers have

endeavored to reduce reverse recovery loss by novel diode structures with hole pockets or deep trenches [4-14]. However, no simple and fast fabrication process has been established for such diodes.

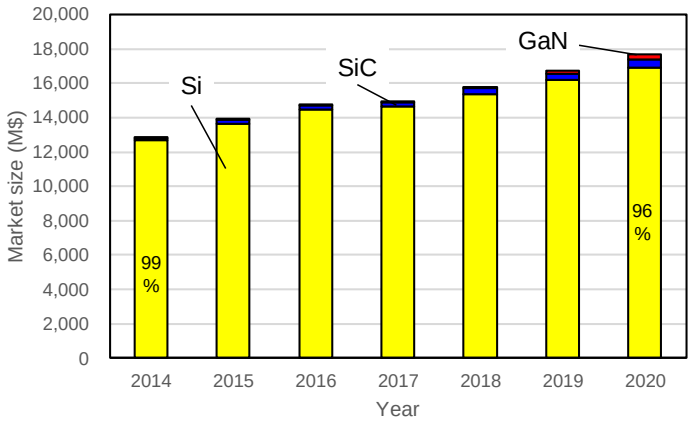


Fig. 1. Growing power device market [2].

We previously proposed a lateral SOI PiN diode with hole pockets as a novel diode structure to revise recovery loss reduction [15, 16]. Unique hole pockets are formed at the border between the silicon on insulator (SOI) and the buried oxide (BOX). The reverse recovery loss and the chip size of the lateral PiN diode and conventional PiN diode is compared by TCAD simulation. In the simulation, the required minimum amount of stored carrier for the conventional PiN diode is controlled by the chip thickness of 80 μm for noiseless waveform comparison. Incidentally, the minimum amount is controlled not only for the thickness but also for the doping concentration of the anode or cathode and lifetime. Thanks to the noise suppression by hole pockets, the diode successfully reduces reverse recovery loss by half by the short current path (see Fig. 2). In addition, it has compatibility between low reverse recovery and low surge voltage with noise compared with a non punch-through diode, punch-through diode and superjunction diode as the conventional and applicable diode. However, the cost of a lateral diode is predicted to be high because a diode with a thin silicon layer requires a large chip size at a certain forward voltage (see Fig. 3). It is about three times larger than conventional vertical diodes. Therefore, a vertical PiN diode with hole pockets is proposed with novel technology of the Bosch deep trench process [17, 18].

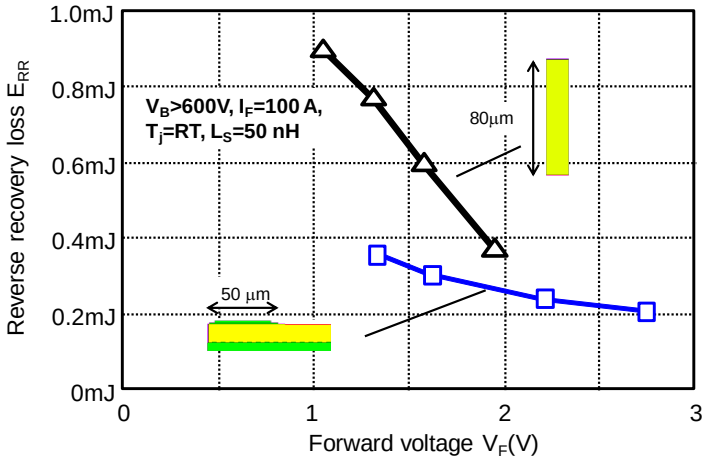


Fig. 2. Trade-off curves between reverse recovery loss and forward voltage including proposed lateral diode [15].

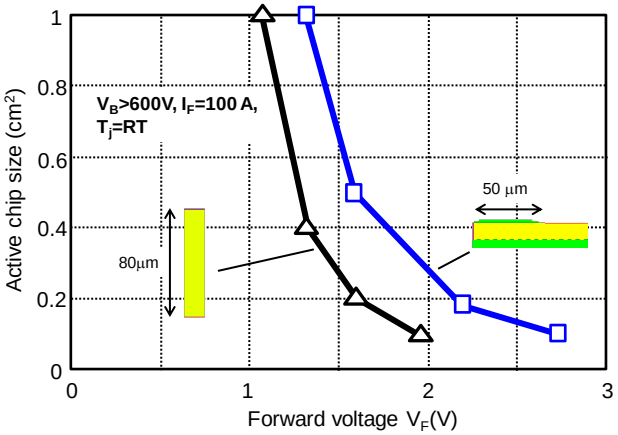


Fig. 3. Trade-off curves between active chip size and forward voltage including proposed lateral diode [15].

2. Hole pocket shape by Bosch deep trench process

We propose the employment of a fast deep trench technology called the Bosch process, which is widely applied for Micro Electro Mechanical Systems (MEMS) and Large-Scale Integration (LSI) technology such as 3-dimensional (3D) capacitors and Through-Silicon Via (TSV). The Bosch deep trench process enables high aspect ratio etching by the alternation of passivation and two kinds of etching cycle (see Fig. 4). In each cycle, a chemically inert polymer layer is uniformly deposited. This passivation layer prevents the sidewalls from being attacked in the subsequent etching step. By feeding high-frequency plasma with etching gases, the passivation layer at the bottom of the trench is rapidly removed by anisotropic etching. After that, the silicon substrate is chemically etched isotopically. The process cycle continues until the target etching depth is reached. Generally, the unique shape called scallop is considered an intruder in the semiconductor field like MEMS and LSI because the scallop decreases the ease of the process after the Bosch process and reduces the device reliability. Therefore, low scallop etching by short etching time per cycle and/or sidewall smoothing by after-treatment is employed now. However, we utilized the scallop as hole pockets based on compensation with thick silicon oxide film.

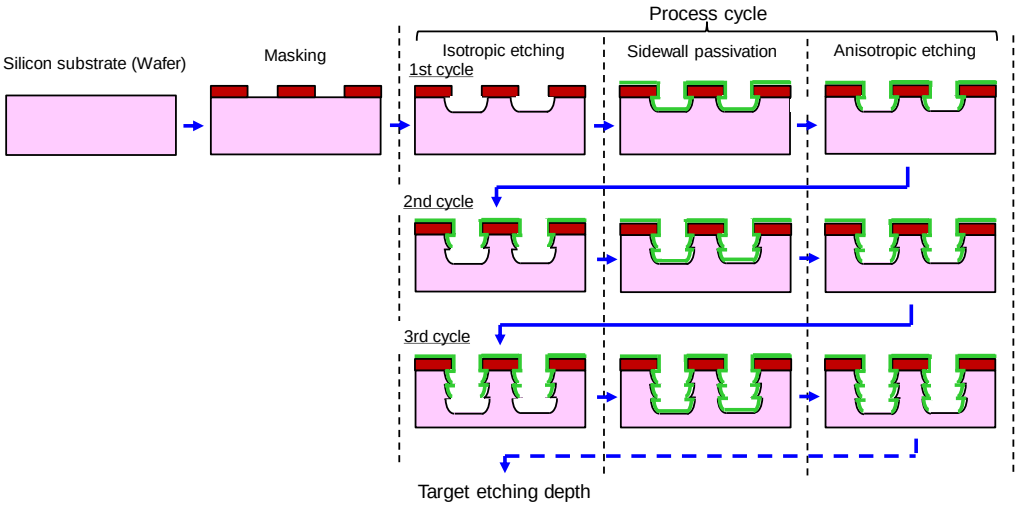


Fig. 4. Cross-section for each step in the Bosch process.

We made deep trenches by the mask of 5 μm, 10 μm, 20 μm and 40 μm Line and Space (L/S) on a trial basis. The time is around 4 minutes per 40 μm deep trench with a sufficiently large scallop (see Fig. 5). The difference in the level of the scallops was successfully shaped for all L/S deep trenches. The difference was about 0.5 μm regardless of the L/S size and continues in the back (see Fig. 6). The scallop shape can be controlled by the etching process. A larger scallop is formed by the larger amount of silicon etching per 1 cycle with longer etching time. The crystal defects near the sidewall are not observed by TEM analysis (see Fig. 7). The subsequent fabrication process for thick oxide film and electrode in the deep trench will be developed next.

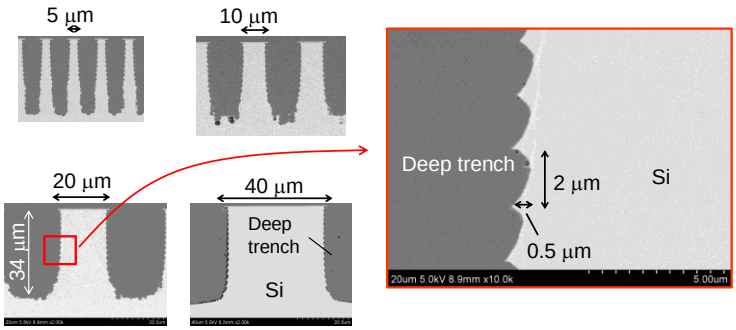


Fig. 5. Cross-section of as-etched trench in the Bosch process by SEM.

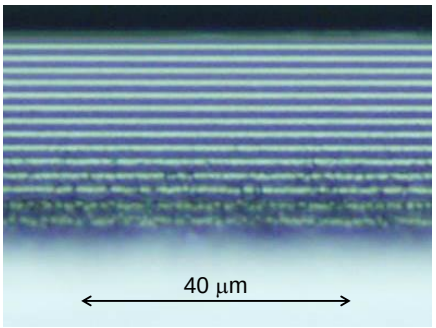


Fig. 6. As-etched trench sidewall in the Bosch process by AFM.

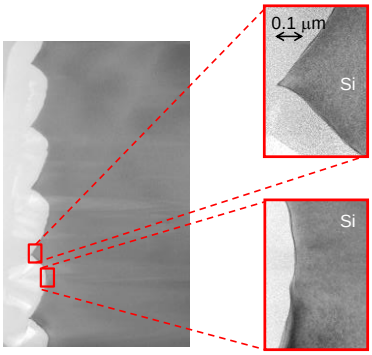


Fig. 7. Cross-section of as-etched trench sidewall in the Bosch process by TEM.

3. Performance prediction of novel diode by TCAD simulation

The as-etched trench shape of the Bosch process was revealed by the trial silicon etching described in Chapter 2. The features of the trench shape are as follows (see Fig. 8).

- The bottom shape has roundness.
- The sidewall shape is a saw blade.
- The pitch of the saw blade shape is about 2 μm.
- The difference in the level of the saw blade shape is about 0.5 μm.

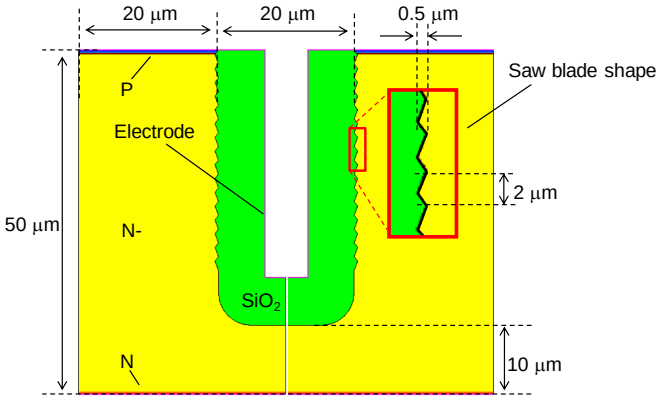


Fig. 8. Cross-section of TCAD simulation.

The performance of the novel diode with the characteristic trench shape was predicted by TCAD simulation. The novel diode has a higher doping concentration of the N- layer. The trench and the higher doping concentration equalize the electric field to maintain high blocking voltage in the off state and eventually realize thinner N-(base) layer thickness. The simulation results indicate a better trade-off curve of reverse recovery loss and chip size. Thanks to the noise suppression with hole pockets, the diode with the thin N-base layer successfully reduces the reverse recovery loss by half (see Fig. 9). If it is possible to employ a thinner N-layer, the reverse recovery loss is further decreased. Furthermore, the active chip size of the novel diode is reduced to two-thirds that of the conventional PiN diode at a certain forward voltage (see Fig. 10). If it is possible to employ a thinner N- layer and/or narrower trench, the chip size is further reduced. In the simulation, the required minimum amount of stored carrier for the conventional PiN diode is controlled by the chip thickness of 80 μm for noiseless waveform comparison as mentioned in Chapter 1.

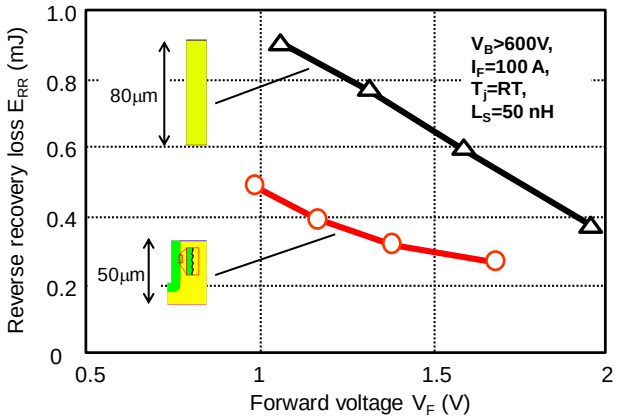


Fig. 9. Trade-off curves between reverse recovery loss and forward voltage including proposed vertical diode.

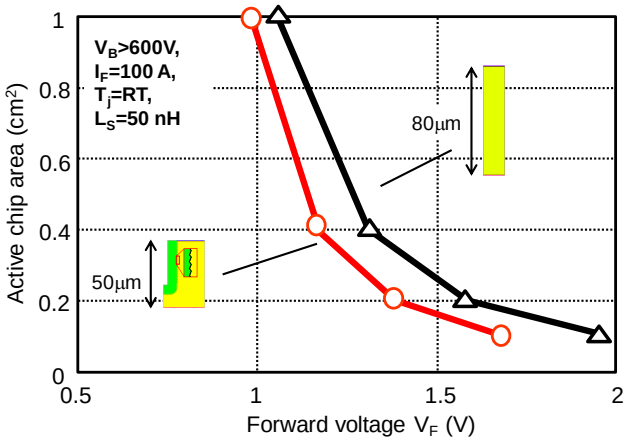


Fig. 10. Trade-off curves between active chip size and forward voltage including proposed vertical diode.

The effect of hole pockets is confirmed with diodes employed at the same N- layer thickness (see Fig. 11). The surge voltage with noise is dramatically suppressed by the novel structure compared with the waveform of the conventional punch-through structure and the simple deep trench diode without hole pockets. Interestingly, the simple deep trench diode has the opposite effect and enhances the surge voltage. The effect for surge voltage suppression is confirmed by the simulation with different pocket height (see Fig. 12). The effective absolute height of the hole pocket is more than 0.1 μm and the effective ratio of pocket height to pocket pitch is more than 0.05. The results indicate that higher pockets strongly suppress surge voltage during reverse recovery.

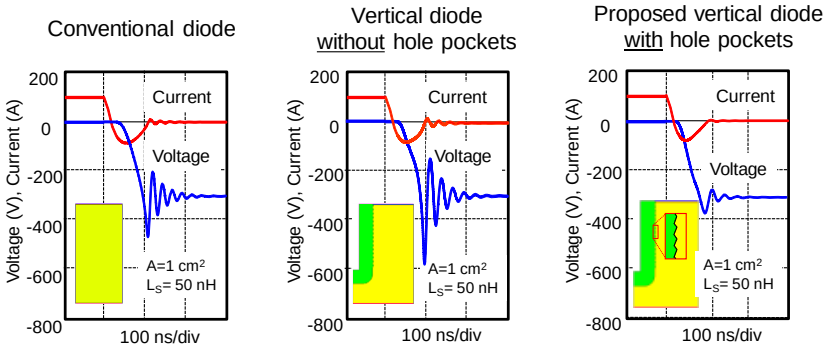


Fig. 11. Reverse recovery waveforms of vertical diodes.

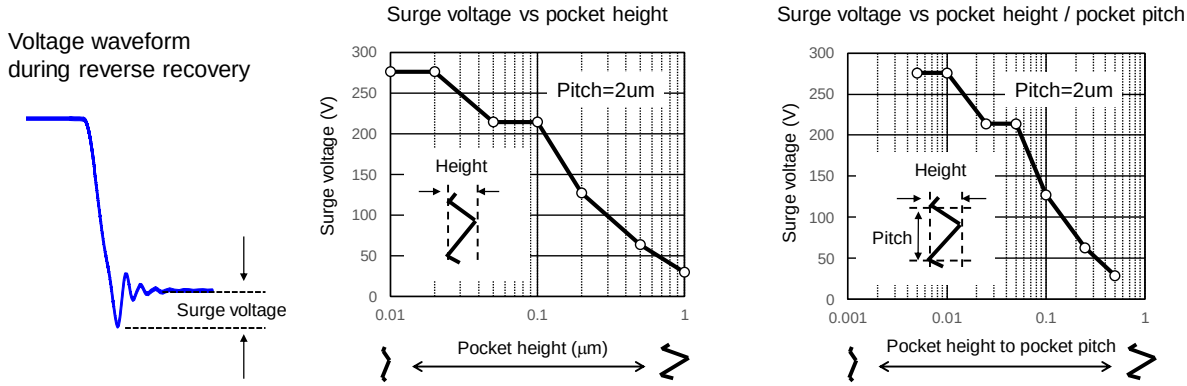


Fig. 12. Effect for surge voltage suppression by each hole pocket design.

4. Hole remaining mechanism by hole pockets to noise suppression

After reverse recovery start, the stored carrier is swept out from the N-base layer. In this reverse recovery process, when the stored carrier is swept out rapidly, surge voltage and noise are generated intensely [19, 20]. Under certain conditions, the conventional diode generates noise and the simple trench diode generates intense noise because the stored carrier in the simple trench diode sweeps out faster (see Fig. 13). The stored carrier of the novel diode successfully remains for a long time after reverse recovery start. The electric field during reverse recovery is analyzed with equipotential lines (see Fig. 14). The electric field for the conventional diode is directed in the depth direction. But it is revealed that the electric field near trench sidewall for simple trench diode and novel diode is diagonal.

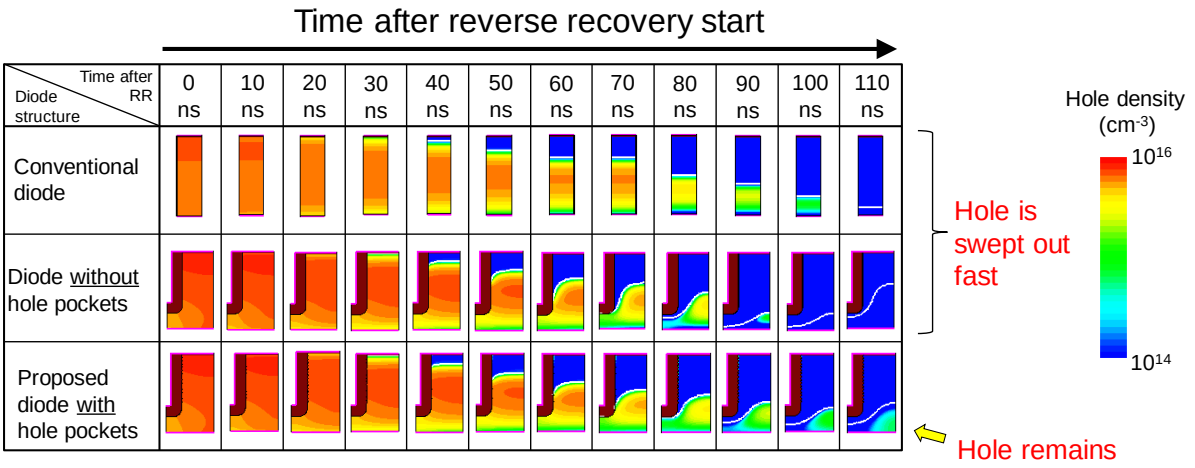


Fig. 13. Hole density during reverse recovery.

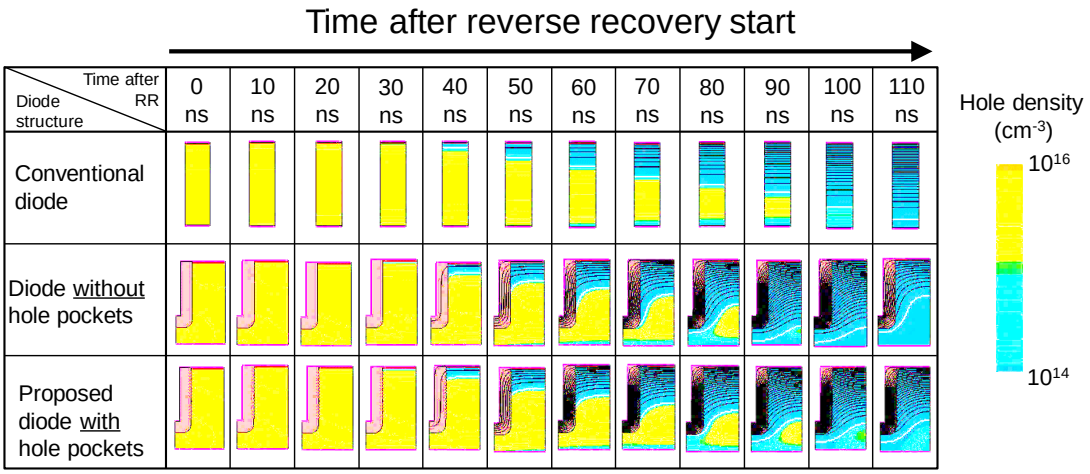


Fig. 14. Equipotential lines with hole density during reverse recovery.

Next, we present the mechanism for remaining hole under hole velocity analysis. In the case of the conventional diode structure, the hole velocity is fast because the electric field is directed in the depth direction (see Fig. 15). For a simple deep trench without hole pockets, the hole velocity is fast as with the conventional diode because the sidewall is smooth even though the electric field is directed in the diagonal direction. On the other hand, the hole velocity of a deep trench with a hole pocket is completely different. The hole velocity of the novel diode is slow because the sidewall is rough and the electric field is directed in the diagonal direction. The hole is expected to drift along the rough sidewall and lose velocity.

On the basis of the results in Chapter 2 to Chapter 4, a narrow (many) trench with higher hole pockets has the best hole remaining effect on the reduction of reverse recovery loss, conduction loss (forward voltage), and chip size.

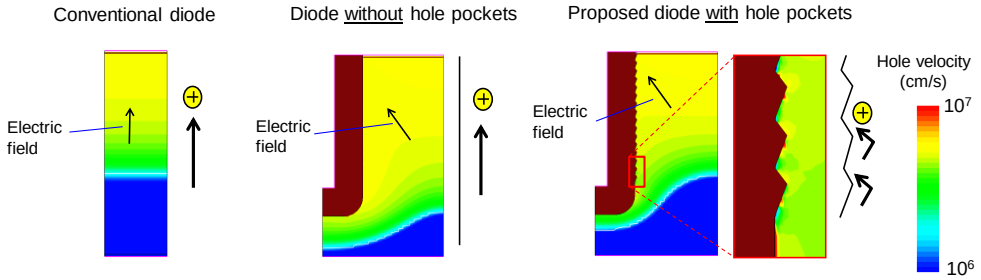


Fig. 15. Hole velocity and schematic diagram of hole drift during reverse recovery.

5. Conclusion

The performance of a novel diode with a characteristic trench shape was predicted by TCAD simulation. A novel 600 V vertical PiN diode with hole pockets by the Bosch deep trench process is proposed for a better trade-off curve between reverse recovery loss and forward voltage. The reverse recovery loss is reduced by half. In addition, the active chip size of the novel diode is reduced to two-thirds that of the conventional PiN diode. Conventional, applicable and proposed diode structures for the PiN diode are non punch-through, punch-through, superjunction, and PiN diode with hole pockets (see Fig. 16). In the three subjects of the reverse recovery loss and active chip size at a certain forward voltage, and surge voltage with noise during reverse recovery, no diode structure satisfies the three subjects without a vertical PiN diode with hole pockets. The novel diode structure is a strong candidate when the simple fabrication process under development is established. The diode structure and fabrication process can be applied to all bipolar devices such as PiN diodes and IGBTs.

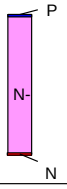
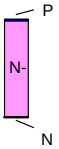
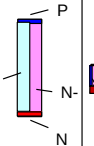
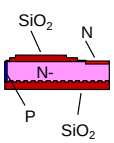
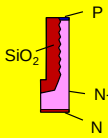
Structure of vertical diode	Non punch-through	Punch-through	Superjunction	Lateral diode with hole pockets	Vertical diode with hole pockets (Novel)
Structure					
Reverse recovery loss	Large	Small	Small	Small	Small
Surge voltage with noise	Small	Large	Large	Small	Small
Active chip size	Small	Small	Small	Large	Small
Fabrication process	Simple	Simple	Complex	Complex	Fabrication process after Si etching is next subject

Fig. 16. Summary of results for proposed diode with benchmarks.

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