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Design and Testing of Electrical Power Subsystem of a Lean Satellite, HORYU-IV

By Mohamed Yahia EDRIES, Atomu TANAKA, HORYU-IV Team and Mengu CHO

Kyushu Institute of Technology, Kitakyushu, Japan

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HORYU-IV is a lean satellite weighing 10 kg or less designed at the Kyushu Institute of Technology. It is planned to be launched with the ASTRO-H in FY2015 as a piggyback on an H-IIA rocket. The main mission of HORYU-IV is to acquire on-orbit data of discharge phenomena occurring on high-voltage solar arrays. An electrical power subsystem (EPS) is one of the HORYU-IV bus subsystems. The function of the EPS is to provide uninterrupted power to all subsystems during the satellite's lifetime. High reliability, high efficiency and simplicity are the main requirements to be considered in the design of an EPS. Generally, an EPS consists of solar arrays, rechargeable batteries, and a power control and distribution unit (PCDU). A peak power tracking topology is preferred to extract the maximum power generated by the solar arrays. The extra energy is stored in nickel-metal hydride batteries. The simple design and usage of available commercial-off-the-shelf components are the main features of the PCDU which controls the battery charging and load voltage regulation. Functional tests under different operating conditions were carried out on the designed EPS to qualify its performance. The aim of this paper is to explain the design of the EPS, and to present and analyze the test results.

Key Words: Commercial-off-the-shelf, Electrical Power Subsystem, HORYU-IV, Lean Satellite

Nomenclature

C	:	Battery discharge capacity (mAh)
E	:	Energy (Whr)
P	:	Power (W)
V	:	Cell voltage (V)
T	:	Time (h)
η	:	Efficiency (non)

Subscripts

B	:	Battery
BCR	:	Battery charge regulator
EPS	:	Electrical power system
e	:	Eclipse period
o	:	Orbit period
off	:	Open-circuit cell voltage
on	:	Cell voltage at 100-mA load
PPT	:	Peak power tracking
s	:	Sunlit period
SA	:	Solar array
Harr	:	Harness
Conv	:	Converter

1. Introduction

In the last 10 years, the electrical power subsystem (EPS) for 15 out of 33 small satellites has been developed based on a peak power tracking (PPT) topology.[1] Although 13 of those were developed based on a direct energy transfer (DET) topology, a PPT has greater advantages such as the possibility of individually extracting the maximum available power from solar arrays, even if they have different configurations and are operating under different thermal and illumination conditions.[2]

HORYU-IV is a 30x30x30-cm satellite developed at the Kyushu Institute of Technology and planned to be launched in 2015. The primary mission of HORYU-IV is to investigate the effect of electrical arcing phenomena caused by the space environment on high-voltage solar panels. The on-orbit acquired satellite discharge data will promote the usage of high-voltage space power systems. According to mass/size aspects, HORYU-IV is considered a Nano scale satellite, but a new term, "lean", has been suggested, which defines satellites that utilize an untraditional risk-accepting development methodology to achieve a low cost and faster delivery.[3]

Due to its small size and the surface occupied by mission payloads, the power generation capability of HORYU-IV is limited to 5.5 W on average, while the heaviest consumption approaches 8 W on average. Seeking system simplicity, efficiency, and reliability, with consideration of lean satellite concepts, we designed the HORYU-IV EPS based on a simple controlled PPT topology using high-efficiency commercial-off-the-shelf (COTS) components.[2] The proposed design also provides reliable operation in case of latch-up failures, safe cold launching, and end-of-life (EOL) satellite deactivation.

This paper presents an EPS design with a description of the key components, and the results of the tests that have been conducted either for individual components or for the system as a whole. The paper is organized as follows: In Section 2, we presented the EPS design description and specifications. In Section 3, we explain the derived formulas to calculate the overall system efficiency. Section 4 gives

the details of IV curve measurement of the solar panels using a sunlight simulator. Section 5 presents the screening test procedures for the NiMH cells. Section 6 shows the radiation hardening test of three different types of field-effect transistors (FETs) used in EPS design. Section 7 demonstrates the functionality of the EPS through integrated testing. Section 8 concludes the outcomes and recommends a prospective plan.

2. EPS Design Description

In this section, the requirements and design of the EPS are briefly presented.

The EPS was designed to meet the requirements of HORYU-IV. The main requirements are to supply all subsystems with uninterrupted power at +5 and +3.3 V, to provide measurements of system health, and to ensure EPS deactivation during launching and at EOL. The power consumption of HORYU-IV was calculated and is summarized in Table 1. The average values were calculated on an orbital basis, whereas the peak value was calculated by assuming that all involved subsystems were working at the same time. The EPS power capability has to cover the budget mainly by the power generated from solar panels or by the battery in off-nominal cases, such as eclipse or overloading.

The EPS includes current and voltage sensors to monitor the system operation. All measurements will be sent to an on-board computer (OBC) subsystem in analog form for decoding. The measured parameters are shown in Table 2.

Table 1. HORYU-IV power budget.

Mode	Ppeak (W)	Pav (W)
Housekeeping Download	5.01	4.03
Full-Duty Mission Operation	8.21	7.31
Half-Duty Mission Operation	8.21	5.87

Table 2. EPS telemetry parameters.

Parameter	No. of sensors	Actual range	Measurement range
Solar Array Current	5	0 – 0.5 A	0 - 2.5 V
DC_Bus Current	1	0 – 2 A	0 – 3 V
Battery Current	1	-2 – 2 A	1.88– 2.2 V
+5V_Bus Current	1	0 – 2 A	0 – 3 V
+5V_S_TX Current	1	0 – 2 A	0 – 3 V
+3.3V_Bus Current	1	0 – 2 A	0 – 3 V
Solar Array Voltage	5	0 – 20 V	0 – 3 V
Battery Voltage	1	0 – 10 V	0 – 3 V
+5V_Bus Voltage	1	0 - 5.5 V	0 – 3 V
+5V_S_TX Voltage	1	0 - 5.5 V	0 – 3 V
+3.3V_Bus Voltage	1	0 – 3.6 V	0 – 3 V

Deactivation during launching (cold launch) is achieved by three switches (separation switches) which inhibit the connection between solar arrays, battery, and loads before separation of the satellite from the launch vehicle. After separation, those switches will be turned ON to allow the EPS to function. At EOL, a normally closed switch (kill switch) will be commanded from the ground station to disconnect the solar arrays from the EPS, hence the battery will fully discharge.

According to functionality, the EPS can be divided into three main parts, as follows:

- Power generation and conditioning
- Energy storage and deactivation switches
- Power distribution and load protection

2.1. Power generation and conditioning

Fig. 1 shows a block diagram of the power generation and conditioning. The power will be generated by five solar arrays (panels), mounted on the +X, +Y, -Y, +Z and –Z faces of the satellite; each panel includes a series connection of triple-junction solar cells of type CTJ-30,[4] assembled by ATSB® on Al substrates. Table 3 shows the specifications of each panel at the maximum power point (MPP), according to the test report [5] prepared by ATSB®. Blocking diodes are added to protect from current flow into shaded panels from the parallel connected illuminated panels; i.e., if the +Y panel is illuminated, the –Y panel is shaded because it is on the opposite side. A shunting system was proposed for safety reasons, to prevent the possibility of power flow to the satellite power bus due to payload fairing jettison and the possible illumination of the solar panels. The shunting switches will connect the solar panels' positive terminals normally to ground through low forward voltage diodes, until the complete separation of the satellite from the launcher. At that time, the shunting switches will be opened and the solar panels' positive terminals will be disconnected from ground.

The power generated from the solar panels will be conditioned by three battery charge regulators (BCRs): BCR1 will be connected to the +X solar panel, BCR2 will be connected to +Y and –Y panels, and BCR3 will be connected to +Z and –Z panels. The BCRs are located in the power control and distribution unit (PCDU). They are designed based on COTS components to operate all panels at their MPP, while simultaneously regulating the output voltage from panels to safely charge the battery. The maximum output voltage from a BCR will be 9.3 V, which will be reduced by a Schottky diode to 9 V. Simple PPT control of BCRs was implemented and tested by the author in Ref. 2). The resulting conditioned power from the three BCRs will be injected through Schottky diodes to a common bus (DC_Bus). A power distribution module (PDM) is a part of the PCDU dedicated to power distribution to load. The PDM and battery will be connected to the DC_Bus. The voltage of the DC_Bus fluctuates between 6 to 9 V according to the battery's state of charge (SOC).

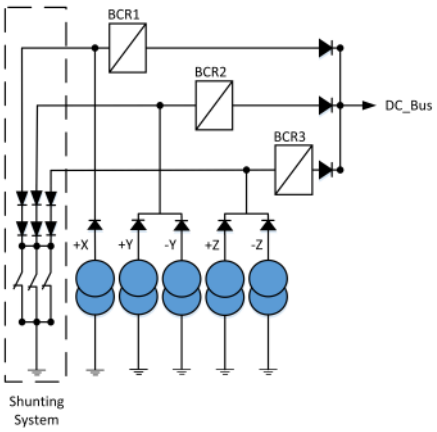

Fig. 1. Power generation and conditioning .

Table 3. Solar panel maximum power specifications at 27ºC and AM0.

Solar Panel	No. of Cells	Pmp(W)	Vmp (V)	Imp (A)
+X	8 in series	8.02	16.6	0.48
+Y and –Y	7 in series	7.18	14.95	0.48
+Z and -Z	6 in series	5.91	12.41	0.48

2.2. Energy storage and deactivation switches

The extra power generated will be stored in a NiMH battery. The battery is composed of three parallel packs, each consisting of six Eneloop® [6] NiMH cells in series. The rated capacity of one cell is 1900 mAh, and for this battery it will be 5700 mAh at 7.2 V. To achieve a longer lifetime, it is better to discharge only 40% of the rated value. Fig. 2 shows the battery and a block diagram of the battery and deactivation switches.

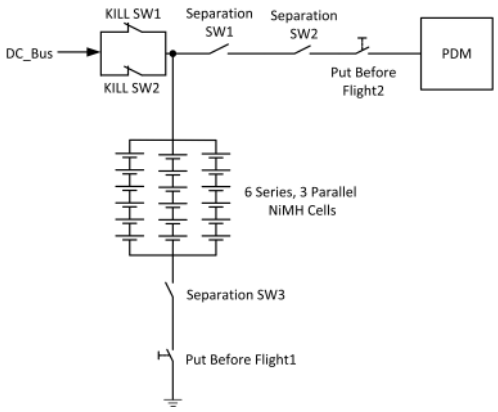

Fig. 2. Battery and deactivation switches.

As shown, the deactivation switches consist of two before flight normally open switches (Put Before Flight1 and Put Before Flight2), three separation switches (Separation SW1, Separation SW2, and Separation SW3) in a normally open state, and two kill switches (KILL SW1 and KILL SW2) in a normally close state. At the launch site, the before flight switches will be permanently closed. The three open SS ensure that the battery is disconnected from the DC_Bus and from the PDM, and the DC_Bus is disconnected from the PDM. After separation of the satellite from the launcher, the three SS will be closed and the EPS will supply power to all subsystems. At EOL, the two kill switches will be open to disconnect the DC_Bus from the battery, which will be deep discharged, and the satellite will stop working.

2.3. Power distribution and load protection

The PDM will consist of three DC/DC converters to regulate the battery voltage to +5 V and +3.3 V. A dedicated DC/DC converter will supply +5V to the S-band transmitter, the second one to supply +5 V to the other subsystems, and the last one to supply +3.3 V to all subsystems. The converters were implemented using high-efficiency COTS components.

Overcurrent protection was implemented for two reasons, namely, to give the OBC control of switching ON/OFF of any subsystem, and to disconnect the load lines in case of overcurrent. Another feature of the PDM is the possibility to reset the OBC and the communication system by external command to recover after a latch-up occurrence. Fig. 3 shows a block diagram of the PDM.

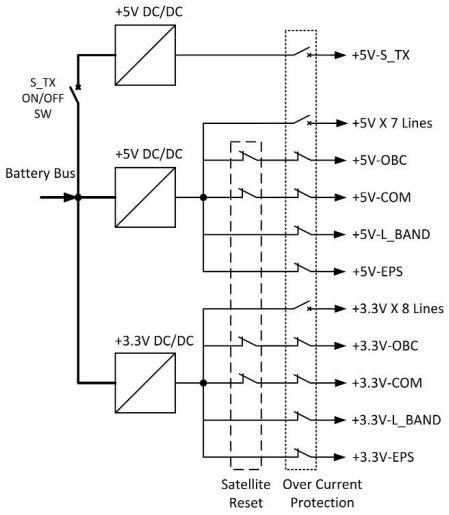

Fig. 3. Power distribution module.

3. EPS Efficiency Analysis

In this section, we derive simple formulas to calculate EPS efficiency and reliability. The EPS can be simplified as shown in Fig. 4. The efficiency of the BCR is represented as two efficiencies, the tracking efficiency (η_{PPT1}, η_{PPT2} and η_{PPT3}) and the converter efficiency (η_{BCR1}, η_{BCR2} and η_{BCR3}). The tracking efficiency indicates the ratio between the extracted power from the solar array and the peak power that can be generated. The converter efficiency is the ratio between the output power from the converter to the DC_Bus and the input power to the converter from the solar array. The battery charge/discharge efficiency is assumed to be equal and combined in one value for simplicity (η_B).

Losses in the blocking diodes, separation and kill switches, and the harness are combined and denoted as η_{Harr} whereas the PDM DC/DC converter losses are represented in η_{Conv1} η_{Conv2} and η_{Conv3}.

In the following formulas, we derive the EPS efficiency in terms of the average generated solar array power (P_{SA_X}, P_{SA_Y} and P_{SA_Z}), stored battery power (P_B), and average delivered load power (P_1, P_2 and P_3).

The power generated by X, Y and Z solar arrays depends on the number of solar cells in each panel. The load will consume the required power, and the extra energy will be stored in the batteries.

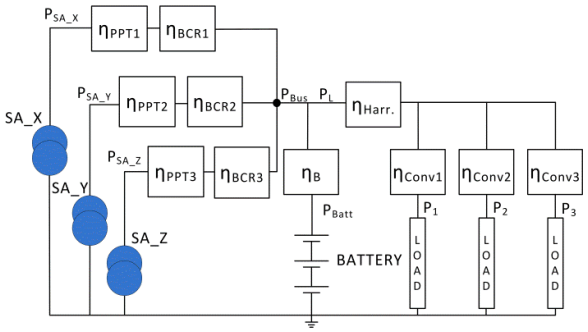

Fig. 4. HORYU-IV EPS efficiency equivalent circuit.

The overall system efficiency is calculated as follows:
The key equation of the calculation is the system energy balance equation. In case of a positive, balanced system, during a sunlit period (T_s) of the orbit, the total generated energy by solar arrays (E_S) will be equal to the energy delivered to the load (E_{L_Sunlit}) in addition to the energy stored in the battery (E_{B_ch}). During the eclipse portion of the orbit (T_e), the previously stored energy in the battery will be discharged to the load. Obviously, the orbital period (T_o) is equal to the sum of T_e and T_s. Eqs. (1) to (3) are the energy balance equations of the system.

$$T_o = T_s + T_e \tag{1}$$

$$E_S = E_{L\_Sunlit} + E_{B\_ch} \tag{2}$$

$$E_{B\_disch} = E_{L\_Eclipse} \tag{3}$$

During the sunlit period, the total energy generated by solar arrays and delivered to the DC_Bus can be calculated as in Eqs. (4) and (5), assuming that all BCR efficiencies are equal.

$$E_S = P_{Bus}T_s = \left(\eta_{PPT1}\eta_{BCR1}P_{SA\_X} + \eta_{PPT2}\eta_{BCR2}P_{SA\_Y} + \eta_{PPT3}\eta_{BCR3}P_{SA\_Z}\right)T_s \tag{4}$$

$$\eta_{PPT1} = \eta_{PPT2} = \eta_{PPT3} = \eta_{PPT}$$

$$\eta_{BCR1} = \eta_{BCR2} = \eta_{BCR3} = \eta_{BCR}$$

$$\eta_{SA} = \eta_{PPT}\eta_{BCR}$$

$$E_S = \eta_{SA}(P_{SA\_X} + P_{SA\_Y} + P_{SA\_Z})T_s \tag{5}$$

In Eqs. (6) and (7), the total load energy is calculated. Because of the similarity of the working conditions of the converters, i.e., power delivered and environment, their efficiencies are considered the same. The charged energy of the battery is calculated in Eq. (8). From Eq. (2), the overall DC_Bus power delivered can be derived as Eq. (9).

$$E_{L_{Sunlit}} = P_L T_s = \frac{T_s}{\eta_{Harr.}}\left(\frac{P_1}{\eta_{Conv1}} + \frac{P_2}{\eta_{Conv2}} + \frac{P_3}{\eta_{Conv3}}\right) \tag{6}$$

$$\eta_{Conv1} = \eta_{Conv2} = \eta_{Conv3} = \eta_{Conv}$$

$$E_{L_{Sunlit}} = \frac{1}{\eta_{Harr.}\eta_{Conv}}(P_1 + P_2 + P_3)T_s \tag{7}$$

$$E_{B\_ch} = \frac{P_{B\_ch}T_s}{\eta_B} \tag{8}$$

$$P_{Bus} = P_L + \frac{P_{B\_ch}}{\eta_B} \tag{9}$$

To calculate the battery power in terms of load power, we assumed that:

$$E_{B\_ch} = E_{B\_disch}$$

$$P_{B\_ch} = \frac{P_{B\_disch}T_e}{T_s} \tag{10}$$

From Eq. (3), we deduce that

$$\eta_B P_{B\_disch} = P_L \tag{11}$$

From Eqs. (5), (8), (9), (10) and (11), the overall EPS efficiency can be calculated as

$$\eta_{EPS_{Sunlit}} = \frac{(P_1 + P_2 + P_3)}{(P_{SA_X} + P_{SA_Y} + P_{SA_Z})}$$

$$= (\eta_{PPT}\eta_{BCR}\eta_{Harr.}\eta_{conv})\frac{\left({}^{T_s}/_{T_e}\right)\eta_B^2}{\left(1 + \left({}^{T_s}/_{T_e}\right)\eta_B^2\right)}$$

$$= \eta_{PCDU}\eta_{St\_Sunlit} \tag{12}$$

$$\eta_{EPS\_eclipse} = \frac{(P_1 + P_2 + P_3)}{P_{B_{disch}}}$$

$$= (\eta_B\eta_{Harr.}\eta_{conv}) = \eta_{St\_eclipse}\eta_{PDM} \tag{13}$$

Eq. (12) revealed that the overall efficiency of the EPS during the sunlit period can be divided into two parts: the overall PCDU efficiency (η_{PCDU}) and the storage element efficiency during the sunlit period (η_{St_sunlit}) . η_{PCDU} depends on the losses in converters and series components on the power line, e.g., diodes, switches, etc. The load conditions, the working temperature, and the value of power line resistance are the factors that affect the value of η_{PCDU}. The type of storage elements, state of charge, depth of discharge (DOD), number of charge/discharge cycles, working temperature, and the eclipse period are the main factors that η_{St_sunlit} depends on.

Eq. (13) shows that EPS efficiency during the eclipse period is higher because it depends on the efficiency of PDM (η_{PDM}) and storage element efficiency during the eclipse period ($\eta_{St\_eclipse}$). From the previous derivation, η_{PDM} is higher than η_{PCDU}, and $\eta_{St\_eclipse}$ is higher than η_{St_sunlit}.

Efficiency improvement using COTS components and a simple design was an aim for the HORYU-IV EPS. Selection of appropriate high-efficiency buck DC/DC converters with simple control techniques, low on state

resistance MOSFET, and Schottky diodes were the solutions to increase η_{PCDU}. Using space heritage NiMH cells, low DOD operation and thermal control were the solutions to improve storage element efficiency.

The estimated efficiency of HORYU-IV was calculated according to the following:

- $\eta_{PPT} = 0.94$ [7)]
- $\eta_{BCR} = 0.9$ [7)]
- $\eta_{Harr.} = 0.95$ (estimated)
- $\eta_{conv} = 0.9$ [7)]

Hence,

$$\eta_{EPS\_Sunlit} = 0.94 * 0.9 * 0.95 * 0.9 = 0.723$$

$$\eta_{EPS\_eclipse} = 0.95 * 0.9 = 0.855$$

In Section 7, we calculate the actual system efficiency based on the test measurements.

4. Solar Panel Testing

In this section, we present the results of the verification test of one solar panel. The objective of the test is to check the IV characteristics of Y solar panels at AM0 irradiance (approximately 1367 W/m^2). A sunlight device made by SERIC [8)] was used to generate the real energy level of AM0. From a 600-mm distance, the solar simulator can generate an irradiance of 1400 W/m^2 within the spectrum of 300-2500 nm, which matches the required AM0 value. The solar simulator will be located in front of a solar panel of seven cells and a lux meter. We used a lux meter to roughly measure the radiance. The reading was 110,000 lux instead of 128,000 lux at AM0.

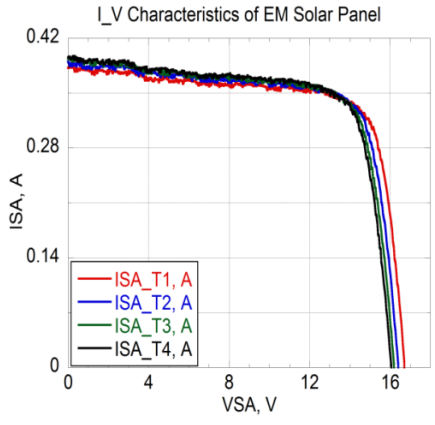

Fig. 5. Seven cell panel IV characteristics.

The solar panel was connected to a KEITHLEY 2400 Source Meter® [9)] to measure the IV characteristics. The source meter swept the panel's voltage with a 42 mV step, and read the current flow out of it. Fig. 5 shows the IV characteristics. The sweeping process was repeated every 2 min to see the effect of temperature change on the characteristics.

A temperature rise caused a noticeable decrease in the open-circuit and MPP voltage, whereas it caused an insignificant increase in the short-circuit and MPP current. Consequently, the MPP power was decreased. It was also noticed that the short-circuit current was 0.4 A instead of 0.49 A, because the irradiance was 0.85 AM0.

5. Battery Testing

In this section, the battery screening test is described. The aims of the test were to characterize the NiMH cells and to select those most identical to make three packs of six series cells. The three packs will be connected in parallel to work as the EPS battery. Each cell has a maximum discharge capacity (C) of 2000 mAh. Fig. 6 shows one battery pack after assembly. The characterization process included two tests: the first was a charge/discharge test, and the second was internal impedance measurement.

Fig. 6. A pack of six series connected Eneloop® NiMH cells.

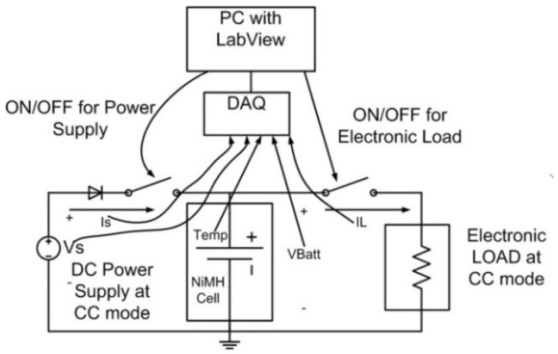

Fig. 7. Battery characterization test circuit.

Fig. 7 shows the test setup that was prepared to test 40 cells, to select the 18 most identical. The test was controlled by LabVIEW®, which controls the charge/discharge of the cells.

The test results from one pack are presented in Fig. 8 and 9 for voltage and temperature, respectively. The charge/discharge test sequence was as follows:

- [1] Discharge at 1 C (2 A) until the cell reaches 1 V.
- [2] Wait after discharge until the cell temperature is 25°C.
- [3] Charge preparation at 0.25 C (0.5 A) for 10 min.
- [4] Rapid charge at 0.5 C (1 A) until the voltage drops by 0.12 V or the temperature reaches 40°C.
- [5] Trickle charge at 0.05 C (0.1 A) for 5 min.

- [6] Wait after charge until the temperature reaches 25°C.

To calculate the internal impedance, we used the DC method. The following procedures were done:

- Fully discharge the cells at a current equal to 1 C (2 A).
- Turn OFF the electronic load (E-Load) and measure the cell's open-circuit voltage.
- Adjust the E-Load at CC mode of 100 mA.
- Turn ON the discharge switch and measure the new cell voltage value.
- The internal impedance is calculated as in Eq. (14):

$$R\_internal = \frac{V_{off} - V_{on}}{0.1} \quad (14)$$

- Repeat the test many times and calculate the average value.

Fig. 10 shows the impedances of 18 cells which vary from 0.076 Ω to 0.082 Ω. Table 4 shows the total impedance of each pack.

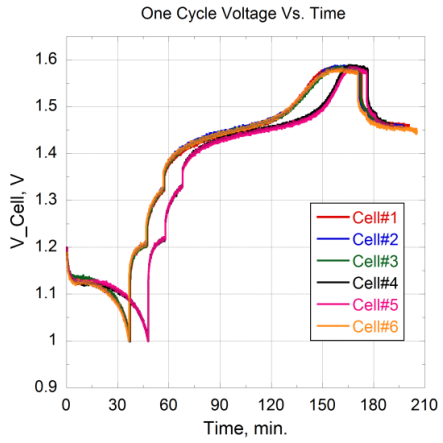

Fig. 8. One pack (6 cells) charge/discharge voltage profile.

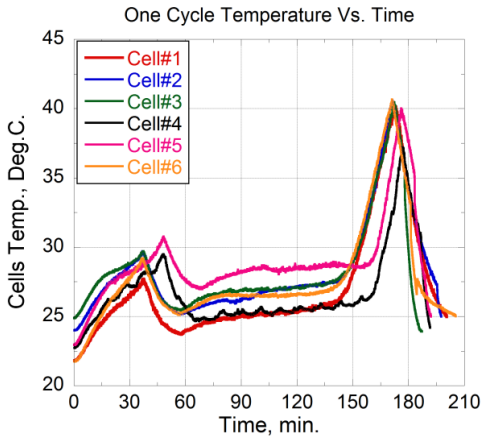

Fig. 9. One pack (6 cells) charge/discharge temperature profile.

Table 4. Total impedance of battery packs.

Pack Number	Total Internal Impedance (Ohm)
1	0.4704
2	0.4704
3	0.4705

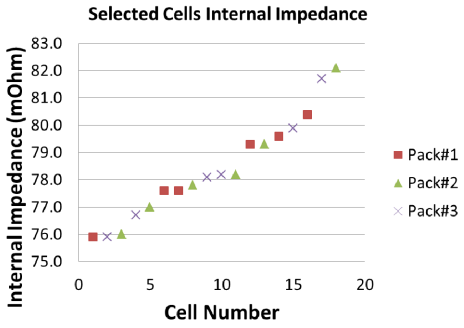

Fig. 10. Individual cell internal impedance.

6. MOSFET Radiation Hardening Test

In this section, we present the results of the total ionizing dose (TID) test for three different MOSFETs which are used in EPS design. The objective of the test was to investigate the functionality of MOSFETs during exposure to a radiation dose up to 20 krad. The test method was to measure the drain-source IV characteristic at different values of gate-source voltage. If the target MOSFET could operate properly up to a radiation level of 10 krad, it was considered to have successfully passed the test.

With a 3-year expected lifetime, at an altitude of 575 km and an inclination of 31°, the expected TID of HORYU-IV was calculated using SPENVIS® [10] for a thickness between 0.5–1 mm, and the maximum dose is 16 krad. The test was held at the Center for Accelerator and Beam Applied Science, Kyushu University. The DUT boards were placed 90 cm apart from a 60 Co gamma-ray irradiation unit to have a radiation dose of 4 krad/h. The cause of the TID damage to the MOSFET [11] is trapped holes in the insulator layer. Accordingly, the transistor threshold voltage will be influenced.

Measurements at every 2 krad were recorded and analyzed. Fig. 11 shows the TID effects on the MOSFETs. For N-MOSFET IRF7910, the gate threshold voltage (Vth) decreased while the dose rate increased, which means the transistor will be easier to switch ON. On the contrary, for P-MOSFET TPC8114, it was noticed that the Vth increased as the radiation dose increased. This means that the transistor tends to switch OFF. These results prove that the accumulated charges in MOSFET gates due to a radiation effect are positive charges (holes). These charges cause a gate-biasing effect, which will help the applied gate voltage in case of the N-MOSFET, and opposes that of the P-MOSFET. In case of depletion-type N-MOSFET BSP135N, the Vth increased with an increased radiation dose. So the device needs a higher voltage to switch OFF, because it is normally ON. Another phenomenon was observed during the OFF state of BSP135N, namely, an increase of leakage current as the radiation dose increased. From the test results, the three types of MOSFETs worked

properly under a radiation dose up to 20 krad, hence they can be used in the EPS.

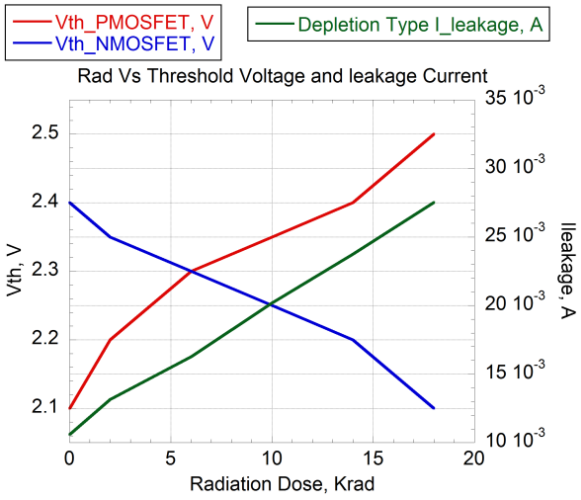

Fig. 11. TID effect of MOSFET.

7. EPS Functionality Tests

In this section, we present the procedures and results of EPS functionality tests. The aims of the tests were to check the system functionality under simulated electrical conditions similar to the real ones that might be faced during HORYU-IV operation. The tests were carried out at room temperature and under atmospheric pressure. Two tests were carried out: the first was the BCR functionality test, the second was to check the whole system functionality. In both tests, the setup will include:

- HORYU-IV EPS engineering model board (EPS_EM v1).
- Two solar array simulators (SAS; Agilent E4350B) [14)]
- Two electronic loads (KIKUSUI PLZ164W) [12)]
- One National Instruments 32-analog-input-channel data acquisition module (NI 9205) [14)]

The two SAS were used to generate the expected power from the Y and Z solar panels. Each SAS simulated one direction power profile, i.e., +Y and –Y or +Z and –Z. The +X solar panel was not considered, to demonstrate the worst case for generated power. The left axis in Fig. 12 shows the expected power profile of both Y (red) and Z (blue) solar panels. The right axis shows the total power (green). From that, the average expected power value is 5.2 W. The power profile did not consider the satellite rotation around the X-axis. The solar irradiance on each face of the satellite was calculated; hence, the maximum generated power from each panel was derived according to the number of cells on each. Assuming that one cycle is composed of a 60-min sunlit period, and a 30-min eclipse period, the power profiles at the MPP for +Y, -Y, +Z and -Z were implemented to be fed to the SAS. From that, the average generated power from the Y and Z solar panels would be 5.2 W.

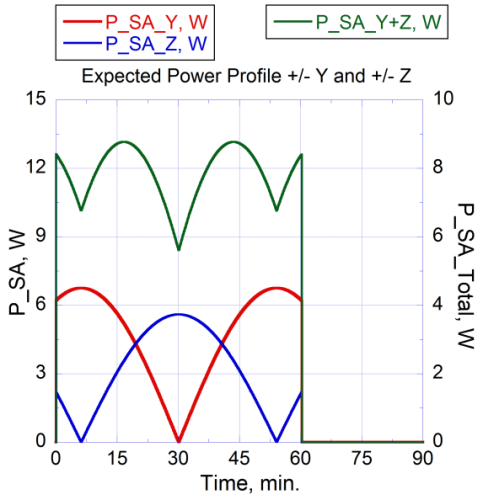

Fig. 12. Expected power profile of Y and Z solar panels.

7.1. BCR stand-alone test

The objective of the test was to prove the advantages of using a PPT-based BCR. The detailed design of the BCR is presented in Ref. 2). The test circuit is shown in Fig. 13. The +Y and +Z solar panels were replaced by SAS-1 and SAS-2, respectively. For two sunlit/eclipse cycles, each SAS was programmed to generate the power profile of the corresponding panels; Y for SAS-1, and Z for SAS-2. The shunting system switches are forced to open, to connect the solar arrays to BCRs. Instead of connecting the battery and PDM to the DC_Bus end, the E-Load was connected and adjusted to work in constant resistance (CR) mode, for two reasons: the first was to ensure the linear relation between the BCR output voltage and current, which creates a more stable performance; the second was to investigate the minimum BCR output voltage that would be reached at minimum input power. The CR mode characteristic is to keep a constant ratio between voltage and current. During the test, the value of the resistance was selected to provide at least 5 W at 6 V; hence, the resistance has to be 7.2 Ω. A voltage of 6 V was desired because it matches the minimum safe working voltage of the battery, and to ensure that the BCR can deliver 5 W at that value. Fig. 14 shows that the desired point could be achieved only in the case of a PPT-controlled BCR. Also, it can be noticed that the minimum output voltage of the BCR was 5.64 V in the PPT case, and 3.32 V in the non-PPT case. This means, even if the battery is open circuited, or its SOC is very low, the BCR can provide enough voltage to operate PDM converters. PDM converters can operate normally in a case where the input voltage is higher than the maximum output (5 V).

Fig. 15 and 16 show the input and output power of the BCR in cases with and without PPT control, respectively. It is seen that more power can be extracted from the SAS in the case of a PPT-controlled BCR. It is also noticed that the power profile in the case of a non-PPT-controlled BCR was more distorted than that of PPT controlled because of the change in SAS-1 and SAS-2 voltages with a variation in

withdrawing currents. In the PPT-controlled BCR case, only the currents were changed, but the voltages were very close to the designed maximum power value (14.8 V for SAS-1 and 12.3 V for SAS-2). Fig. 17 and 18 show the profiles of BCR input and output.

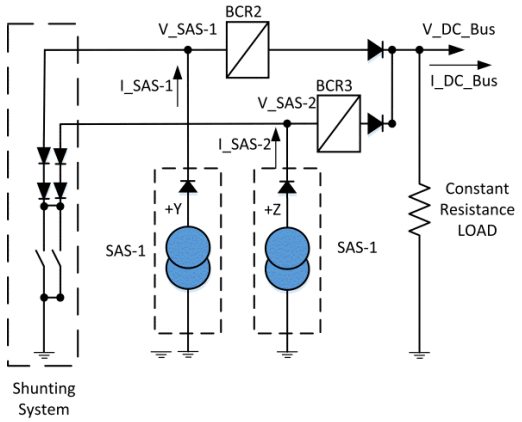

Fig. 13. BCR stand-alone test circuit.

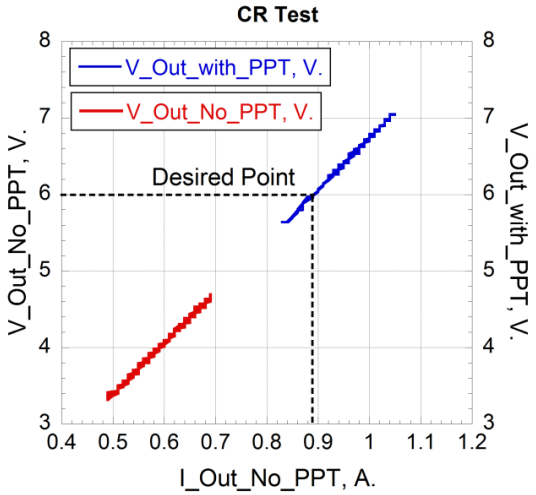

Fig. 14. BCR stand-alone test circuit.

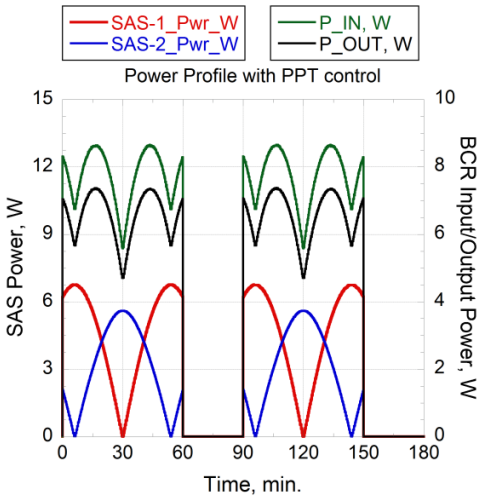

Fig. 15. Input and output power of BCR with PPT control.

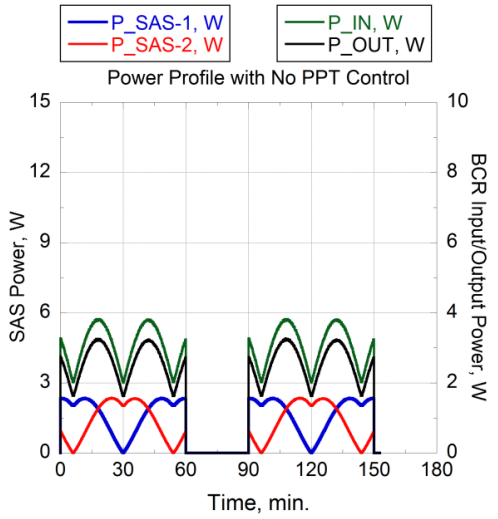

Fig. 16. Input and output power of BCR without PPT control.

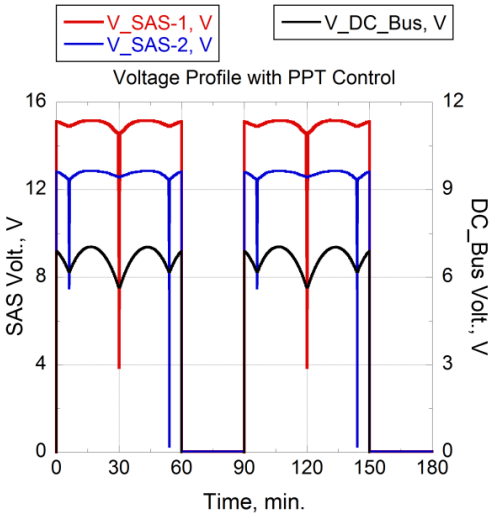

Fig. 17. Input and output voltage of BCR with PPT control.

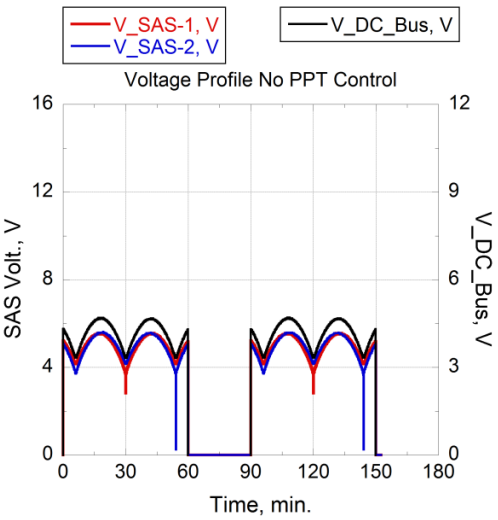

Fig. 18. Input and output voltage of BCR without PPT control.

7.2. EPS integrated test

HORYU-IV's EPS_EMv1 was tested to check the functionality of all individual parts after integration within the same board. As mentioned in the EPS design section, the +Y and –Y solar panels consist of seven triple-junction solar cells connected in series, whereas +Z and –Z consist of six series cells. To compensate for the temperature effect on the panels, the MPP voltage will be less than the value at 27°C by 0.1 V, assuming a +10°C temperature increase. Simulating HORYU-IV in-orbit operation, the PPT controllers were permanently adjusted to let BCR-2 and BCR-3 work at the MPPs of 14.8 V and 12.3 V, respectively. A real battery was used to check its performance in case of charge or discharge. The EPS sensor readings were collected by a DAQ module. The test was supervised and controlled from a PC by a dedicated LabVIEW® program. The test was carried out for three cycles, each 90 min in duration. For the first 60 min, SASs and E-Loads were switched ON, and for the remaining 30 min, SASs were switched OFF, and E-Loads remained ON and supplied by the battery.

The integrated test circuit is shown in Fig. 19. The test sequence was as follows:

- Connect SAS to +Y solar array input, and SAS-2 to +Z solar array input.
- Simulate three cycles of the generated power by Y and Z solar panels as shown in Fig. 12, and program SAS-1 and SAS-2 to work accordingly.
- Connect the battery to the dedicated input. The battery's state of charge was 90%, and the initial voltage was 7.89 V.
- Connect E-Load-1 to +5V_Bus Output, and E-Load-2 to +3.3V_Bus.
- Set E-Load to constant current (CC) mode of 0.6 A to have an output power of almost 5 W on the load side.
- Disable solar array shunting and enable the separation switches.
- Using the LabVIEW® test control program, start SAS-1 and SAS-2 cycles and record the measurements acquired by DAQ.

Fig. 20 shows EPS total input power (green), DC_Bus power (black), and output power profiles. The calculated average value of the input power was 4.9 W, which means that, out of 5.2 W (the expected generated average power (Fig. 12)), 4.9 W could be extracted using BCRs with PPT control. Hence, a BCR with a PPT controller could extract 94.2% of the generated power. Of that 4.9 W, 4 W was converted to the bus by BCRs, hence, the combined conversion efficiency (η_{SA}) approaches 81.6%. As shown in Table 1, the nominal power consumption for HORYU-IV will be 4.03 W, which means that the generated power in the worst case will be sufficient to supply power to the loads. At 30, 120, and 210 min, the DC_Bus power was not sufficient to supply the load power (4.65 W), so the battery was discharged to compensate for that shortage. The sum of the DC_Bus power and battery discharged power resulted in a total power of 5.8 W, which was converted to the load through PDM DC-DC converters. The conversion efficiency approached 80%. From Fig. 21, the solar array voltages of both Y and Z panels were very close to the designed MPP (14.8 V and 12.3 V, respectively). There is a severe drop in SAS-1 voltage at 30, 120 and 210 min, because these are the transition moments from shadow to illumination. That was also the case for SAS-2 voltage at 10, 50, 100, 140, 190, and 230 min. The battery voltage was decreasing because of discharging during both SAS ON and OFF periods. The +5V_Bus and +5V_S_TX voltages were 4.99 V and 5 V, respectively. The +3.3V_Bus voltage was 3.2 V. In Fig. 22, the battery current was negative almost all the time because it was in a discharging state. The DC_Bus current, which was measured after BCRs, varied according to the changing of the input current from the SASs. The input voltage from the SASs was fixed at the MPP, hence, the current variations were similar to the power profile variations. The +5V_Bus and +3.3V_Bus currents were constant at 0.6 A.

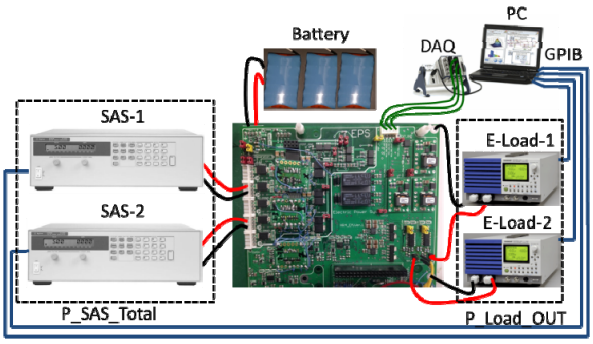

Fig. 19. EPS integrated test setup.

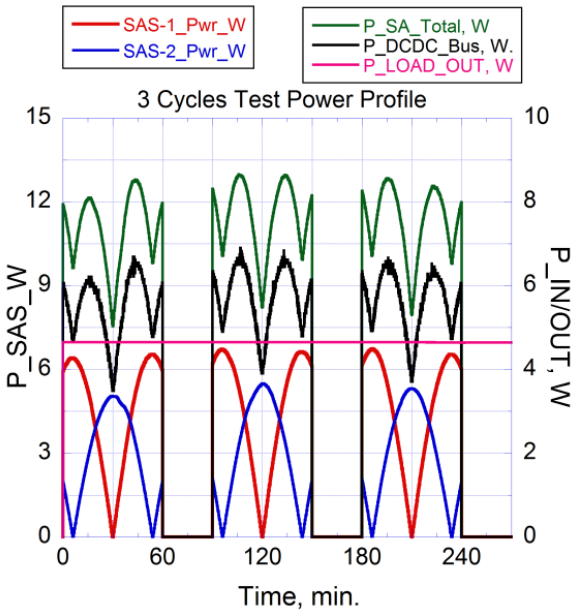

Fig. 20. EPS integrated test input and output power profile.

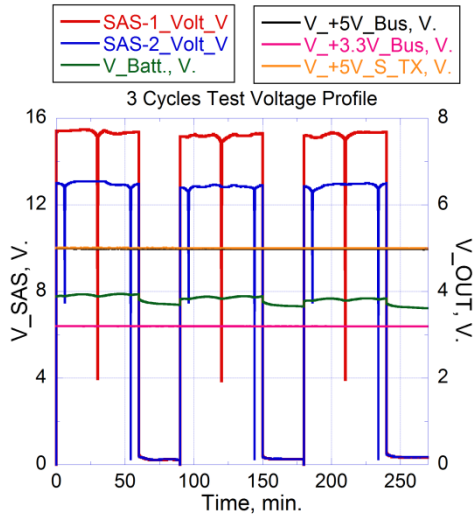

Fig. 21. EPS integrated test input and output voltage profile.

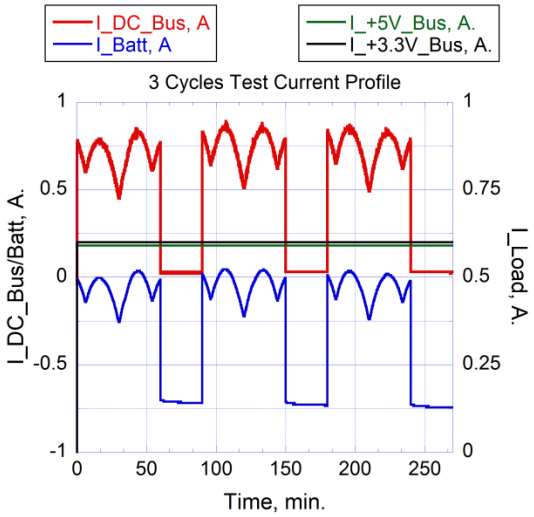

Fig. 22. EPS integrated test input and output current profile.

8. Conclusion

Simplicity and cost reduction are the main advantages of lean satellites. After testing our EPS, we found that using a simple design based on available COTS sub-units with acceptable performance is faster and cheaper than building a system from scratch. A PPT-controlled BCR and PDM DC/DC converters are clear examples of the lean concept.

The EPS functionality tests revealed that the designed simple PPT controller could achieve a tracking efficiency of 94.2% (η_{PPT}). Indeed, the efficiency of PPT topology needs to be improved by minimizing losses in series components, i.e., converters, diodes, transistors and current sense resistances. On average, the overall system efficiency, which is the ratio of the input power from solar panels to the output power to the loads, would be 70% to 75% at most. It represents a multiplication of BCR and PDM converter efficiencies.

In the worst case of generated power, the EPS can provide enough power to operate at housekeeping download mode.

Satellite cold launching and EOL deactivation could be achieved by using a shunting system, separation and kill switches.

EPS sensors show a linear performance all over the expected operating range.

The results of testing solar panels with a sunlight simulator were consistent with the manufacturer datasheet. The battery screening test consumed a lot of time, on average 4 h/cell. The test procedures were strictly performed, hence, the accuracy of the results is very high.

MOSFETs included in the EPS design, could well tolerate a harsh radiation environment. The radiation test results consolidate the knowledge of the TID effect on MOSFETs.

In the future, the EPS board, solar panels and battery will be integrated into an engineering model structure, and undergo thermal vacuum, vibration, and shock tests. According to the results, an EPS flight model (EPS_FM) will be developed. The EPS_FM will be functionally tested as engineering model.

Acknowledgments

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