Modelling of the shoot-through phenomenon introduced by the next generation IGBT in inverter applications

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Abstract

The shoot-through phenomenon has not been fully discussed for high-power inverters with IGBTs. This is because a negative gate voltage is applied to IGBTs during off states. Recently, attention is paid to an improved gate driver with only a positive gate voltage in order to meet demands for simplification, integration, and reduction in power consumption as well as in cost of the gate driver. Moreover, the threshold voltage of the next-generation IGBT will decrease with microfabrication techniques of the gate structure. This will make the shoot-through phenomenon severer and degrade the inverter reliability with the next-generation IGBTs. The influence of the parasitic parameters in both the IGBT and circuit on the shoot-through mechanism has not been investigated so far.

This paper clarifies the shoot-through mechanism and investigates the impact of the next generation IGBTs on the inverter reliability. The influence of the internal capacitance of IGBT including stray inductance on inverter reliability is experimentally confirmed.

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1. Introduction

Applications of power semiconductor devices like automotive, power delivery, and industrial motor drive always face a significantly long operating time and high reliability [1]. Attentions have been paid to reliability-oriented issues such as failure analysis in open- or short-circuit [2], thermal design of power modules [3], life-time estimation [4], and the so-called shoot-through phenomena [5-9]. The gate drivers of present IGBTs in inverters usually provides a negative gate voltage during off intervals to prevent the shoot-through phenomenon. As shown in Fig. 1 (a), the negative gate voltage results in no net reverse transfer capacitance C_{CG} because a hole inversion layer is formed between the N-base layer and gate oxide interface, and the reverse transfer capacitance C_{CG} is shielded from the gate terminal. Thus, the negative gate voltage not only prevents the shoot-through problem but also improves the reliability of the inverter operation.

On the other hand, in case that the gate voltage is zero during off intervals, a large amount of reverse transfer capacitance exists, and there will be a path of the noise current as shown in Fig. 1 (b). Hence, only a positive gate-driving voltage will suffer from the shoot-through phenomenon. Moreover, attention has been paid to microfabrication techniques for the next-generation IGBT toward CMOS compatible wafer processes [10]. This IGBT has a lower threshold voltage when compared with the conventional IGBTs, so that it has higher sensitivity to the high-frequency noise current flowing through C_{CG}. Therefore, the shoot-through phenomenon will be severer for the next-generation IGBTs, and a significant reduction of the reliability is concerned by inverters with next generation Si-IGBTs. However, the influence of the parasitic parameters in both the device and circuit on the shoot-through mechanism has not been investigated so far.

This paper clarifies a shoot-through mechanism and investigates the impact of the next generation IGBTs on the inverter reliability. The shoot-through mechanism is obtained from an intensive analysis of a one-leg inverter, considering parasitic circuit parameters including stray inductances and junction capacitances in the IGBT.

2. Mechanism of Shoot-Through Phenomenon

This section discusses the mechanism of the shoot-through phenomenon for a simple one-leg inverter. When a high-frequency noise current occurs in the high-side switch with a high dv/dt, it flows into the reverse transfer capacitance C_{CG} of the low-side switch, of which the gate voltage varies. This gate noise voltage causes the shoot-through phenomena when the gate noise voltage exceeds the gate threshold voltage of the low-side switch.

Existing models for shoot–through phenomenon consist only of parasitic capacitances of power devices [1-5].

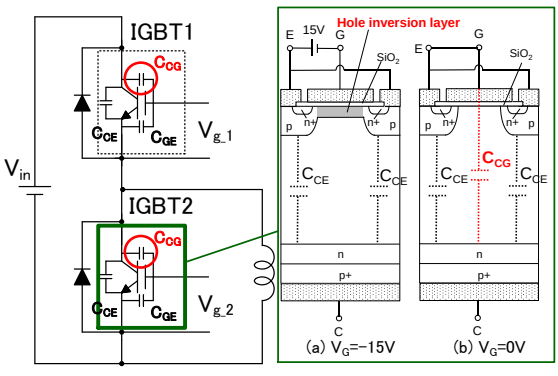


Fig. 1. Shoot-through occurrence for IGBT.

In this case, the peak value of the noise voltage across gate and emitter terminals V_{GE}_peak is given by the following equation [8];

$$V_{GE\_peak} = \frac{C_{GC}}{C_{GE} + C_{GC}} V_{in} \quad (1)$$

In actual inverters, parasitic inductances exist around everywhere on the circuit pattern, so the parasitic inductance may have an influence to the noise voltage.

This paper investigates the mechanism of the gate noise voltage including parasitic inductances, and also examines the noise model not only in time domain (waveforms) but also in frequency domain (spectrums). An analytical model is built in order to clarify the shoot-through criterion. Figure 2 shows a one-leg inverter used for analysis and experiment, and the gate voltage waveform of each switch. The noise voltage occurs at the gate terminal of the low-side switch Q_2 as shown in Fig. 2 (b).

3. Shoot-Through Analysis

At first, the following conditions are assumed:

1. The switching speed (dv/dt) is enough fast, so that the input source Vin is a step voltage source.
2. The load behaves as a current source because the noise voltage happens in a greatly short time interval compared with a period of the inverter output current frequency.
3. The low-side switch is completely turned off when the noise voltage occurs, so it consists of a capacitor network.
4. A silicon carbide Schottky barrier diode (SiC-SBD) is used for the freewheeling diode, which has no net reverse recovery current. Therefore, the freewheeling diode acts as an ideal switch and its equivalent model after turning off consists only of its junction capacitance.

Figure 3 shows an analytical model of the one-leg inverter. The circuit equations are given as follows:

$$\begin{cases} V_{in} = L_{bus}\dfrac{di_{bus}(t)}{dt} + L_{CE}\dfrac{d}{dt}\left(i_D(t)+i_Q(t)\right) + l_D\dfrac{di_D(t)}{dt} + \dfrac{1}{C_{AK}}\int i_D(t)dt \\ l_D\dfrac{di_D(t)}{dt} + \dfrac{1}{C_{AK}}\int i_D(t)dt = \left(l_C + l_E\right)\dfrac{di_Q(t)}{dt} + \dfrac{1}{C_Q}\int i_Q(t)dt \\ i_{bus}(t) = I_o + i_D(t) + i_Q(t) \end{cases} \quad (2)$$

where,

$$C_Q = \frac{C_{GE}C_{GC}}{C_{GE}+C_{GC}} + C_{CE} \quad (3)$$

the initial condition of Eq. (2) is given by,

$$\begin{cases} i_{bus}(0) = I_o \\ i_D(0) = i_Q(0) = 0 \end{cases} \quad (4)$$

The Laplace transform of Eq. (2) is given by

$$I_Q(s) = L_{bus}\left(sI_{bus}(s) - I_o\right) + L_{CE}\left(I_D(s) + I_Q(s)\right) \quad (5)$$

The inverse Laplace transform of Eq(5) gives the current flowing through the low-side switch $i_Q(t)$ in time domain. as follows:

$$i_Q(t) = A_{HF}\sin\omega_{HF}t + A_{LF}\sin\omega_{LF}t \quad (6)$$

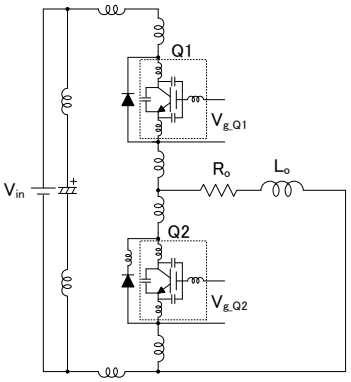
The resonant angular frequency ω_{HF} and ω_{LF} are given as follows:

$$\omega_{HF} = \sqrt{\frac{h+\sqrt{h^2-4g}}{2g}}, \quad \omega_{LF} = \sqrt{\frac{h-\sqrt{h^2-4g}}{2g}} \quad (7)$$

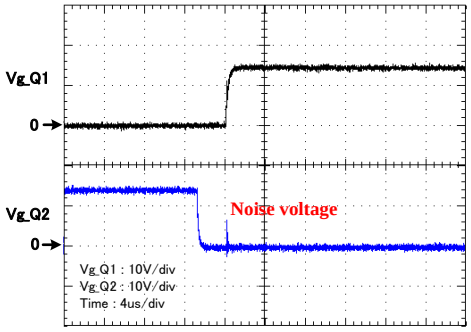
where, h and g are approximately given by the following equations:

$$\begin{cases} h \approx C_{AK}\left(L_{bus}+L_{CE}\right) + C_Q\left(L_{bus}+L_{CE}\right) \\ g \approx C_Q C_{AK}\left\{l_D\left(L_{bus}+L_{CE}\right) + \left(l_C+l_E\right)\left(L_{bus}+L_{CE}\right)\right\} \end{cases} \quad (8)$$

From these results, the resonant angular frequency ω_{HF} and ω_{LF} are approximated by the following equations:



(a) Circuit diagram



(b) Gate voltage waveforms

Fig. 2. One-leg inverter.

$$\begin{cases} \omega_{HF} \approx \sqrt{\dfrac{h}{g}} = \dfrac{1}{\sqrt{\dfrac{C_{AK}C_Q}{C_{AK}+C_Q}\cdot\left(l_D+l_C+l_E\right)}} \\ \omega_{LF} \approx \dfrac{1}{\sqrt{h}} = \dfrac{1}{\sqrt{\left(C_{AK}+C_Q\right)\cdot\left(L_{bus}+L_{CE}\right)}} \end{cases} \quad (9)$$

The amplitudes of A_{HF} and A_{LF} are given as follows:

$$A_{HF} = \frac{M - K\omega_{HF}^{\ 2}}{\omega_{HF}\left(\omega_{LF}^{\ 2} - \omega_{HF}^{\ 2}\right)}, \quad A_{LF} = \frac{M - K\omega_{LF}^{\ 2}}{\omega_{LF}\left(\omega_{HF}^{\ 2} - \omega_{LF}^{\ 2}\right)} \quad (10)$$

where,

$$\begin{cases} M \approx \dfrac{V_{in}}{C_{AK}\left\{l_D\left(L_{bus}+L_{CE}\right)+\left(l_C+l_E\right)\left(L_{bus}+L_{CE}\right)\right\}} \\ K \approx \dfrac{l_D V_{in}}{l_D\left(L_{bus}+L_{CE}\right)+\left(l_C+l_E\right)\left(L_{bus}+L_{CE}\right)} \end{cases} \quad (11)$$

The current flowing through the low-side switch has two frequency components as shown in Eq. (6) - (11). The high-frequency component ω_{HF} is generated by the switch loop formed from the low-side switch and its free-wheeling diode, whereas the low-frequency component ω_{LF} is generated by the main loop including bus line inductances.

Although the gate noise voltage contains the high-frequency component, the impedance of gate capacitance at the high frequency is significantly small. Therefore, the voltage variation of gate terminal resulting from the high-frequency component can be neglected. Hence, the gate noise voltage can be approximately given by Eq. (12) which includes only low-frequency component.

$$v_{GE}(t) = \frac{C_{GC}}{C_{GC}+C_{GE}} V_{in}\left(1-\cos\omega_{LF}t\right) \quad (12)$$

Moreover, the peak value of the gate noise voltage is given by the following equation:

$$V_{GE\_peak} = \frac{C_{GC}}{C_{GC}+C_{GE}} 2V_{in} \quad (13)$$

The gate noise voltage is the product of twice the input voltage $2V_{in}$ and a division ratio of C_{GC} and C_{GE}.

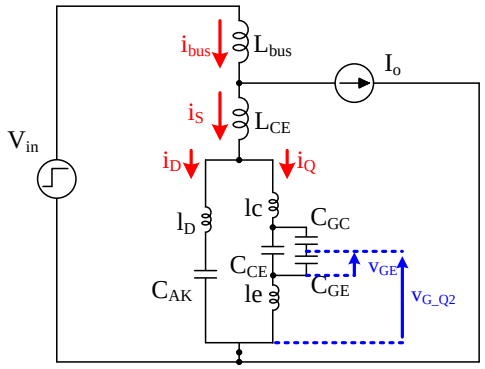


Fig. 3. Analytical model for the shoot-through criterion.

In practice, the inductance between the gate and emitter terminals includes the common emitter inductance for measurement as shown in Fig. 3, so the measurement gate voltage is given as follows:

$$v_{G\_Q2}(t) = \alpha A_{HF}\cos\omega_{HF}t + \beta A_{LF}\cos\omega_{LF}t \quad (14)$$

where,

$$\alpha = \left(l_E\omega_{HF} - \frac{1}{C_{GE}\omega_{HF}}\right), \quad \beta = \left(l_E\omega_{LF} - \frac{1}{C_{GE}\omega_{LF}}\right) \quad (15)$$

The high-frequency component appears between the gate and emitter terminals even though the actual gate-emitter voltage v_{GE} has only the low-frequency component as shown in Eq. (12). Hence, the high-frequency component would confuse an observer. Even though the shoot-through phenomenon does not occur, it seems to occur from the measurement waveform.

In order to evaluate the mentioned above discussions, a numerical analysis is performed using the circuit parameters as shown in Table 1, which are the same parameters of the experiment described in the next section. Figure 4 shows the time-domain waveforms and its spectrum obtained by the analytical results. The gate noise spectrum of the time-domain waveform, as well as that of the measurement gate-source voltage, has two peaks at 16 MHz and 143 MHz as shown in Fig. 4 (a). The amplitude of the 143 MHz component of the time-domain waveform is around 4.0 V, whereas that of the actual gate-source voltage waveform is around 0.2 V. Moreover, actual gate voltage peak is around 1.7 V as shown in Fig. 4 (b).

4. Experimental Verifications

In order to evaluate the validity of the analytical model, a prototype test board was constructed and tested.

Table 1
Circuit parameters

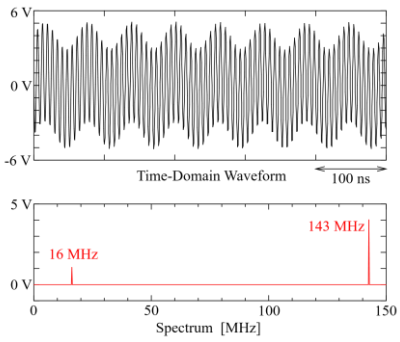
Symbol	Descriptions	Value
V_{in}	Input voltage	100V
f_{sw}	Switching frequency	12kHz
L_{bus}	Bus line inductance	160nH
l_D	Diode internal inductance	10nH
l_C	Collector internal inductance	3nH
l_E	Emitter internal inductance	6nH
L_{CE}	Collector-Emitter line inductance	30nH
C_{AK}	Diode junction capacitance	390pF
C_{GE}	Gate-Emitter capacitance	4700pF
C_{GC}	Gate-Collector capacitance	25pF
C_{CE}	Collector-Emitter capacitance	55pF

To improve the consistency of experimental noise measurement, the test board has been constructed by a printed-circuit board (PCB), the line inductance is calculated by vector potential in theory. Moreover, the capacitances of switching devices are obtained from their date sheet.

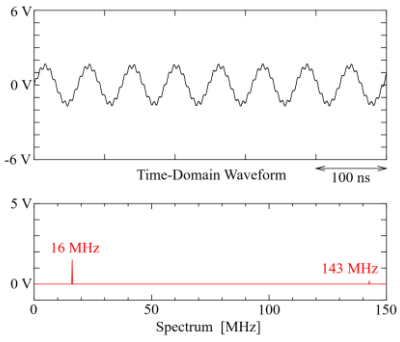
Figure 5 shows the gate voltage waveform and its spectrum of the low-side switch Q_2. The gate noise voltage contained a high-frequency component of 120 MHz and a low-frequency component of 22 MHz.

Moreover, a band limitation function of the oscilloscope enabled to show almost the same waveforms as the actual gate-emitter voltage V_{GE} because the high-frequency component caused by the common emitter inductance was almost removed as shown in Fig. 5 (b). This waveform was not exactly the same as actual waveform but would be a reference for the shoot-trough phenomenon. The peak voltage of the band-limitation gate voltage was around 4 V.

The threshold voltage of the IGBT used for the experiment is around 6 V that is obtained from its data sheet. From the analytical result, the gate noise voltage peak is 4.5 V. In this case, the shoot-through phenomenon do not occur.



(a) Gate voltage



(b) Actual gate voltage

Fig. 4. Analytical results of gate noise voltage.

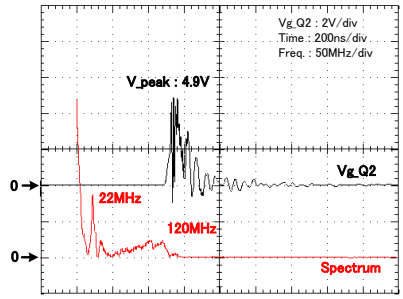
In order to confirm the shoot-through phenomena, a capacitor was intentionally added between the collector and gate terminals.

Figure 6 shows the experimental waveforms which confirmed the influence of additional capacitors.

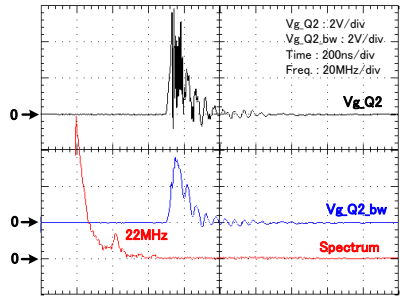
The noise voltage peak without any additional capacitors was around 3.5 V, and that with an additional capacitor of 50 pF was around 4.5 V as shown in Fig. 6 (a) and (b), respectively.

The voltage peak with an additional capacitor of 200 pF was around 9 V, where the noise voltage peak was over the threshold voltage, then the shoot-through phenomena occurred and a short current flowed through the IGBT as shown in Fig. 6 (c).

Figure 7 shows the relationship between the gate noise voltage peak and the additional capacitances. When the larger additional capacitor was introduced, the difference between analytical and experimental results became larger. This is because the additional capacitor was connected in parallel between the collector and gate terminals including the collector inductance L_C. The gate noise voltage peak reached the threshold voltage at 150 pF additional capacitor.

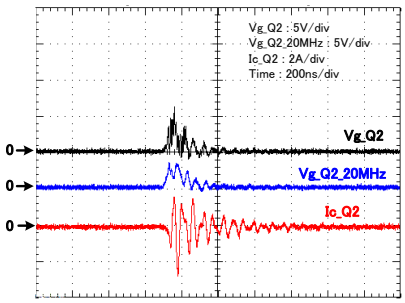


(a) Gate voltage

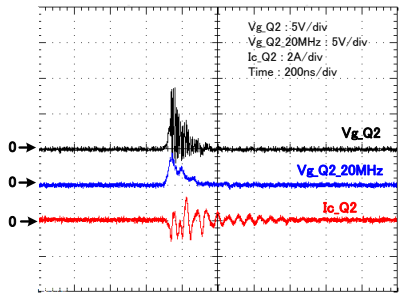


(b) Gate voltage with band limit.

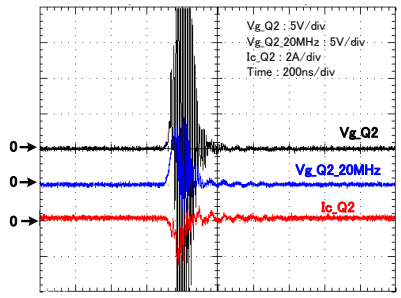
Fig. 5. Experimental results of gate noise voltage



(a) 0pF



(b) 50pF



(c) 200pF

Fig. 6. Gate voltage waveforms with additional capacitors.

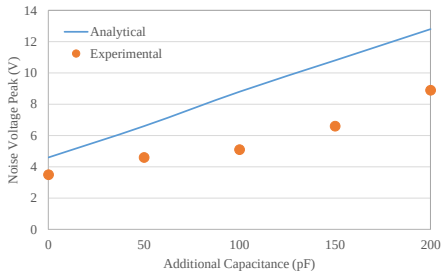


Fig. 7. Gate noise voltage peak with additional capacitors

5. Conclusions

This paper has clarified a shoot-through mechanism. Moreover, the influence of the parasitic inductances on inverter reliability was analytically investigated and examined by a simplified one-leg noise model.

As a result, the validity of the one-leg simplified model has been experimentally confirmed.

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