Mutual inductance influence to switching speed and TDR measurements for separating self- and mutual inductances in the package

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***Abstract*—Parasitic inductances in power semiconductor packages affect the device switching speeds. The self-inductance of the source terminal has been considered to be the main factor that limits the switching speed, but mutual inductances among the three terminals also influence the speed. This paper proposes a method to measure the source self-inductance and the mutual inductances in the package using time-domain reflectometry (TDR) and time-domain transmissometry (TDT) that reveals the limitation of the switching speed. The measurement results agreed well with those of Q3D simulation.**

Keywords—mutual inductance, switching speed, power semiconductor package, TDR, TDT

I. INTRODUCTION

As power semiconductor devices attain higher switching frequencies and higher current capabilities, the parasitic inductances in these devices are having increasingly strong effects on their switching characteristics [1-5]. The self-inductance of the source terminal mainly influences the switching speed in larger devices, while mutual inductance mainly affects the speed in smaller devices.

Mutual inductances among the gate, drain and source terminals affect the switching speed of the device package. Figure 1 shows the current density and the magnetic field of a TO-247 package. The source current i_S increases and decreases rapidly during the turn-on and turn-off periods, respectively. The source self-inductance L_S and the magnetic field add an induced voltage to the gate-source voltage V_{GS} in proportion to the slew rate of i_S. The effect of the magnetic field is changed by both the direction and the switching speed of the current. The magnetic effect and the source inductance limit the switching speed of power semiconductor packages, but the relationships between the two inductances and the switching speed have not been investigated theoretically to date.

Two points must be addressed to evaluate the effects of the parasitic inductances on the switching speed. The first involves clarification of the effects of the self- and mutual inductances from a theoretical viewpoint and acquisition of the corresponding equations. The second point is that the self- and mutual inductances among the three terminals must be measured separately.

This paper analyzes the limitations of the switching speed of a power device package based on consideration of the source self-inductance and the three mutual inductances and then introduces a measurement method using time domain reflectometry (TDR) and time domain transmissometry (TDT) that gives these four parameters separately.

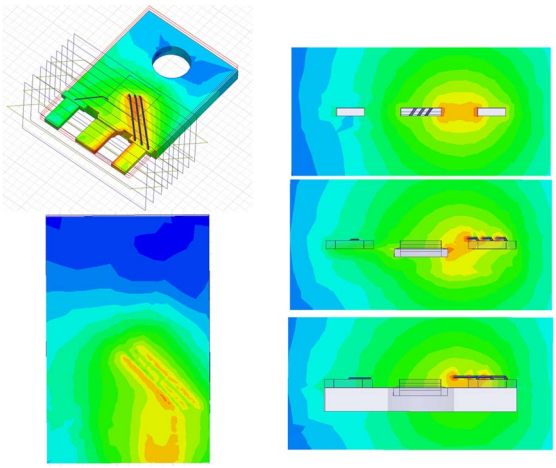

Fig. 1. Current density and magnetic field of TO-247 package.

II. SWITCHING SPEED LIMIT

The mutual inductances in a power semiconductor package influence its switching speed. The source self-inductance and the mutual inductances among the three terminals add an induced voltage to the gate-source voltage V_{GS} during the turn-off period. V_{GS} is expressed using the following equation in the equivalent circuit shown in Fig. 1.

$$\mathrm{V_{gg}} - \mathrm{V_{GS}} = \mathrm{L_G C_{GS}} \frac{d^2 V_{GS}}{dt^2} + \{(L_S + M_{GD} + M_{GS} + M_{DS})\mathrm{gm} + R_G C_{GS}\} \frac{dV_{GS}}{dt} \quad (1)$$

From this equation, the authors defined a time constant composed of $(L_S+M_{GD}+M_{GS}+M_{DS})gm+R_GC_{GS}$ as the "M-factor". When the mutual conductance gm is sufficiently high, the maximum value of the slew rate of the drain current I_D is given by the following equation:

$$\left[\frac{dI_D}{dt}\right]_{max} \cong \frac{(V_{gg} - V_{th})}{L_S + M_{GD} + M_{GS} + M_{DS}} \quad (2)$$

The switching speed limit can be estimated based on the M-factor and $[\mathrm{d}I_D/\mathrm{d}t]_{\max}$, and its value is dependent on the package structure. Based on these equations, the limit of the switching speed of the package is determined by measuring $L_S+M_{GD}+M_{GS}+M_{DS}$.

III. Simulation

A. SPICE Simulation

In this work, a SPICE simulation was used to confirm the influence of the M-factor and $[dI_D/dt]_{max}$. We measured the parasitic inductances in some example packages and these inductance values were input into the SPICE circuit model for a double pulse test. The switching speeds determined using equations (1) and (2) were then compared with the speeds given by SPICE simulation of the inductance model.

B. Q3D Simulation

Quasi-3D (Q3D) simulations are used to confirm the accuracy of the parasitic inductance measurements. Fig. 2 shows a TO-247 package and the model of the package used for the Q3D simulation. The gate terminal and the source terminal are connected to the front side of the chip through bonding wires. In this case, the left side is the gate, the center is the drain, and the right side is the source.

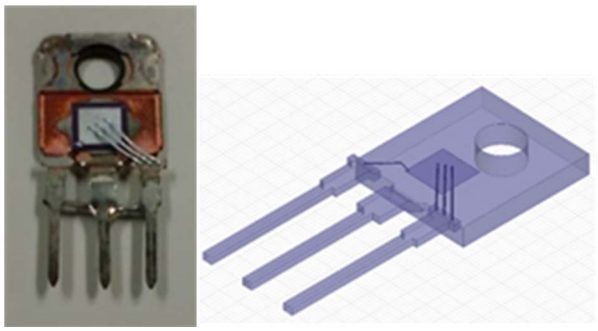

Fig. 2. TO-247 package and model used for the Q3D simulation.

IV. Measurement

A. Three-Port Measurement

This method measures six inductances from the three terminals. The authors have introduced a "neutral point" in the package [1] that separates the three terminals into six inductances. This neutral point is placed at the center of the metal-oxide-semiconductor field-effect transistor (MOSFET) chip in the package and is grounded. Fig. 3 shows the proposed TDR and TDT measurement setup. Two of the three terminals were connected to a digital oscilloscope through 50 Ω microstrip lines and the other is terminated at 50 Ω. The neutral point is connected to the ground on the back side of the strip line. The digital oscilloscope provided a high-speed step voltage for input into one of the terminals. The reflected and transmitted waves, denoted by e_r and e_t, respectively, were then observed via the oscilloscope. The following equations give the self-inductance L and the mutual inductance M [5].

$$\mathrm{L} = \frac{z_0}{2e_i}\int_0^\infty (e_i + e_r)\,dt \tag{3}$$

$$\mathrm{M} = \frac{z_0}{2e_i}\int_0^\infty e_t\,dt \tag{4}$$

The self-inductances and mutual inductances of each terminal are calculated from the reflected and transmitted waves.

B. Two-Port Measurement

Another measurement method using TDR and TDT [6] was also used in this paper. The value of $L_S+M_{GD}+M_{GS}+M_{DS}$ can be measured directly without a "neutral point" when using this method. Fig. 4 shows the two-port measurement setup. This method grounds the source and connects the other two terminals to the digital oscilloscope through the 50 Ω microstrip line. The digital oscilloscope then inputs a high-

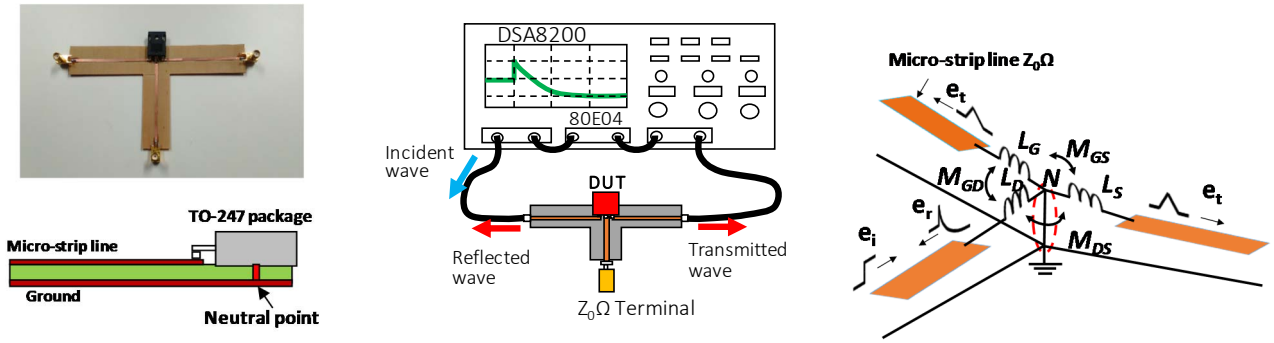

Fig. 3. Self- and mutual inductance measurement setup (DSA8200 oscilloscope with 80E04 TDR sampling module and microstrip line) and reflected/transmitted waves on the strip lines.

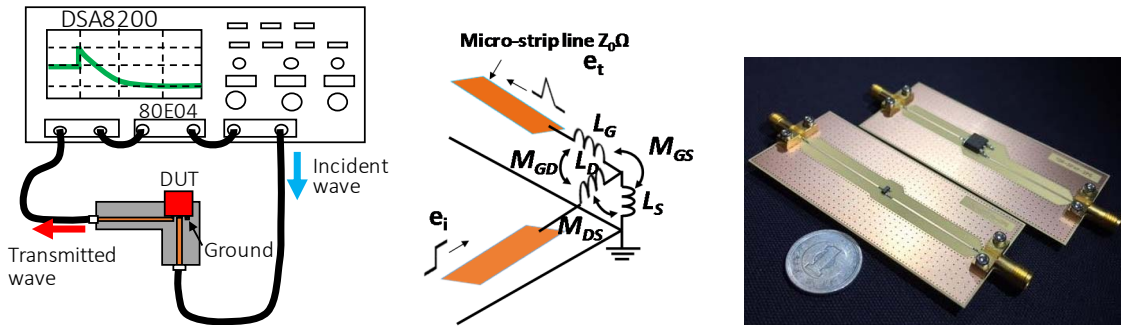

Fig. 4. Two-port measurement setup (DSA 8200 with 80E04 module and microstrip line) and reflected/transmitted waves on the strip lines. Photograph shows an example of microstrip line for the two-port setup for surface-mount packages.

speed step voltage to the drain terminal and measures the transmitted voltage. The following equation gives L_S+M_{GD}+M_{GS}+M_{DS}:

$$L_S + M_{GD} + M_{GS} + M_{DS} = \frac{Z_0}{2e_i}\int_0^\infty e_t\,dt \qquad (5)$$

L_S+M_{GD}+M_{GS}+M_{DS} are calculated from the transmitted wave.

C. Results and Influence of Mutual Inductance

The measurement results were evaluated via SPICE and Q3D simulations. Fig. 5 shows an example of the reflected and transmitted waveforms from the strip line connected to the drain that were measured using the three-port measurement method. Fig. 6 shows a comparison between the results of the experiments and the simulations. The error was less than 1 nH. SPICE circuit simulations and double pulse testing confirmed the influence of the mutual inductance. Figs. 7 and 8 show the simulated results with value of measured inductances when using low- and high-voltage MOSFETs, respectively. These figures show the turn-on period waveforms, which were compared in the cases of zero inductance, self-inductance only and both self- and mutual inductances. V_{DS} falls most rapidly in the case without inductance, and falls most slowly in the case with self-inductance. The turn-on speed with the self- and mutual inductances is faster than that with self-inductance only. The mutual inductances increased the switching speed during the turn-on period. Measurement results are provided for several packages in this work. Table 1 shows the results for L_S+M_{GD}+M_{GS}+M_{DS} for five packages. The two measurement methods gave different values and the two-port measurement results were closer to those of the Q3D simulations than the three-port measurements. The error is caused by the conductor that connects the package to the ground and the capacitance of the chip. Fig. 9 shows the SPICE simulation results for the turn-on time of the TO-247 package as a function of the M-factor for both LV-MOSFETs and HV-MOSFETs. Fig. 10 shows the limits of the drain current slew rate.

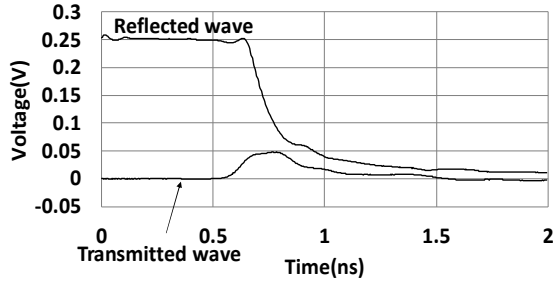

Fig. 5. Example of measured reflected waveform for strip line connected to drain.

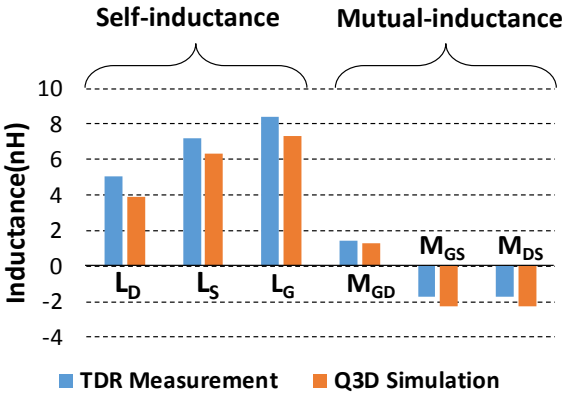

Fig. 6. Comparison of experiments and simulations.

TABLE 1. Results for L_S+M_{GD}+M_{GS}+M_{DS}

	3 ports measurement L_S+M_{GD}+M_{GS}+M_{DS}	2 ports measurement L_S+M_{GD}+M_{GS}+M_{DS}	
	Measurement(nH)	Measurement (nH)	Q3D (nH)
TO-247 1000V MOSFET (FQH8N100C)	5.2	5.3	4.0
TO-220 120V MOSFET (TK32E12N1,S1X)	9.7	3.4	3.5
DPAK 250V MOSFET (IRFR224PBF)	5.51	2.7	3.4
SOT-223 60V MOSFET (NVf3055L108T1G)		2.9	2.5
SOT-23 60V MOSFET (2N7002ET1G)		0.94	0.85

V. Conclusion

This paper has clarified the source self-inductance and the mutual inductances among three terminals to give switching speed limits for power semiconductor device packages. Measurement methods were proposed and their accuracy was confirmed using Q3D simulations and SPICE simulations.

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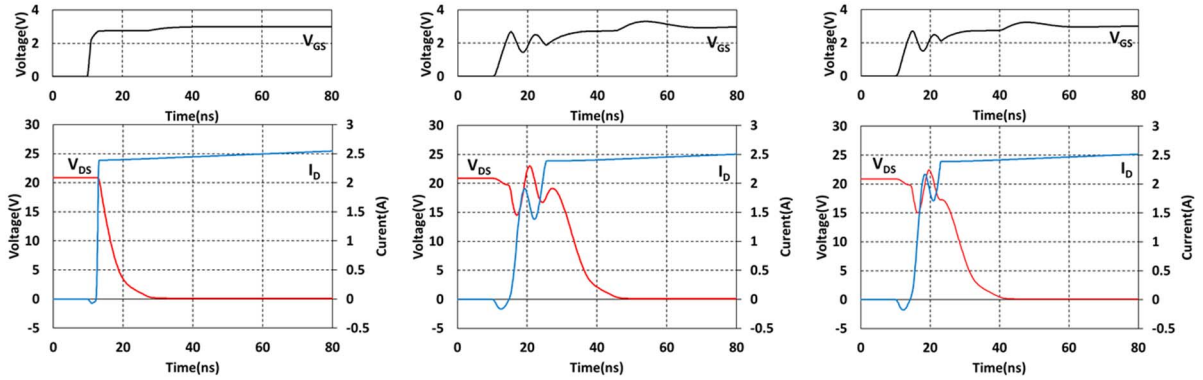
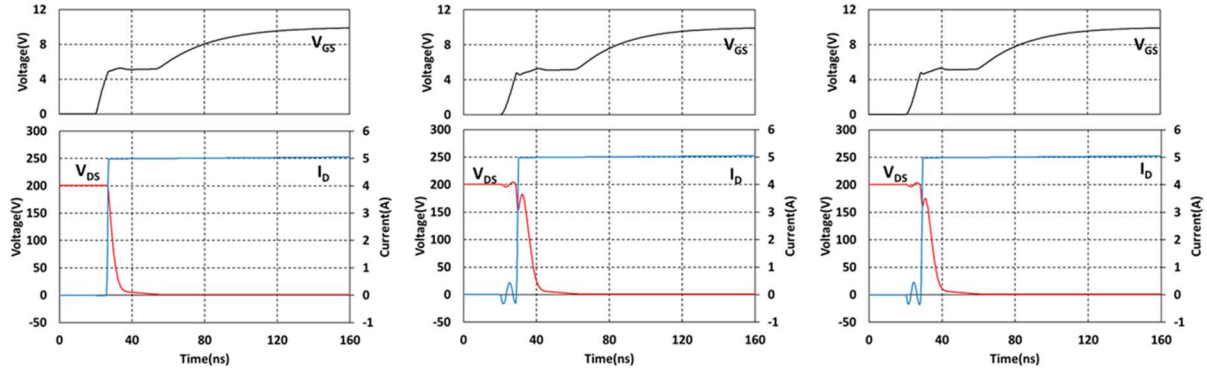


(a) Waveform without stray inductance. (b) Waveform with self–inductance. (c) Waveform with self and mutual inductances.

Fig. 7. Simulated results with various measured inductances (low-voltage MOSFET).



(a) Waveform without stray inductance. (b) Waveform with self- inductance. (c) Waveform with self and mutual inductances.

Fig. 8. Simulated results with various measured inductances (high-voltage MOSFET).

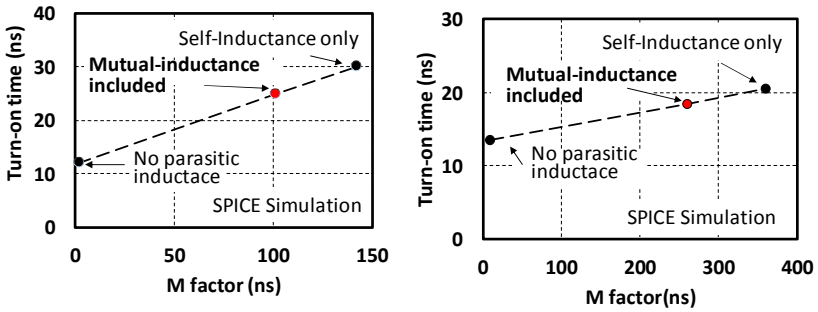


Fig. 9. Turn-on time SPICE simulation results as functions of M-factor $=(L_S+M_{GD}+M_{GS}+M_{DS})gm+R_GC_{GS}$ for LV-MOSFET and HV-MOSFET.

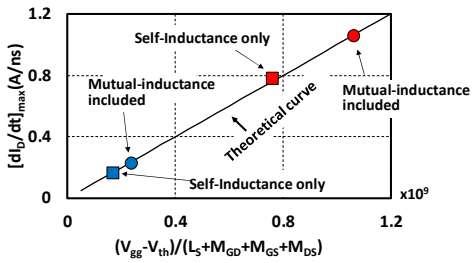


Fig. 10. Limits of drain current slew rate (blue: LV-MOSFET; red: HV-MOSFET).