Active Voltage Balancing for Series Connected IGBT System using Gate Delay Control

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Abstract

Series-connected Insulated Gate Bipolar Transistor (IGBT) devices are used to meet the essential high-voltage requirements for power electronic converters. Nevertheless, series operation of these devices can easily result in an uneven distribution of voltage stress among the devices. This paper presents a gate delay control method to achieve uniform voltage distribution among devices connected in series. This active voltage balancing is based on peak detection of collector-emitter voltages to implement gate delay control.

1. Introduction

Solid state devices are used in high power applications and possessing distinctive characteristics corresponding to the material of a device. Si-IGBTs are among the most extensively developed and commercially matured solid-state devices. This has been used in various high power applications such as high-voltage transmission, solid-state transformers, and circuit breakers and in many other applications in high power systems [1]-[2]. Over the last decades, a rapid increase in demand for power led to essential need of power converters with a higher voltage rating for power generation and transmission that exceed the capabilities of state-of-the-art devices.

High-voltage power systems ranging from tens to hundreds of kilovolts can be realized through the series connected operation of IGBT devices. However, the uneven distribution of voltage stress among the devices is a crucial concern caused by asymmetrical system layouts and non-identical system parameters [2]. Moreover, voltage overshoot during switching may result in the breakdown of the devices due to.

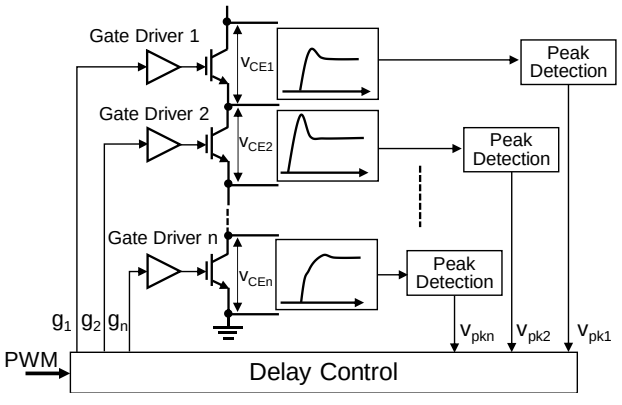

Fig. 1 Schematic diagram of gate delay control (GDC) for 'n' series connected IGBT devices.

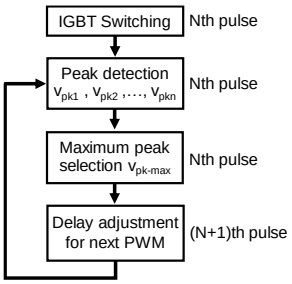

Fig. 2 Implementation steps of GDC.

Various methods have been presented in the literature to suppress the overshoot and unbalancing of voltages and that can be summarized as being active and passive methods. Active methods can be preferable over passive ones, that suffer from increased losses and inadequate active balancing

An active gate current control is presented in [2]- [3], however, significantly complex gate drive circuitry and control are required for implementation. The gate delay control (GDC) method based on peak detection and minimization in [4] is presented for active current balancing of paralleled IGBT devices. The effectiveness of control is demonstrated for two parallel IGBTs in [4] and four parallel IGBTs in [5] for overshoot minimization and active balancing of current.

In this extended abstract, the GDC scheme shown in Fig.1 is presented for a series connected IGBT system for active voltage balancing (AVB). Peak detection of collector-emitter voltage during switching transients is used to manipulate the gate delay as summarized in Fig.2. The attractive features of this GDC are as follows:

1) Easy implementation using general-purpose gate drivers.
2) Dynamic balancing through peak minimization.
3) Low cost: analog-digital hybrid/ fully digital control.

2. Gate Delay Control (GDC)

General

Non-identical system parameters perturb the gate signal switching timings, which lead to asynchronous switching of the devices. The unbalancing in the devices owing to async-

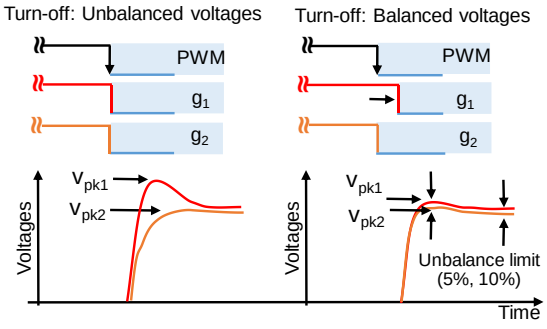

Fig. 3 Delay adjustment for AVB of two series connected IGBT.

hronous switching can be compensated through manipulation of the gate signal timings as represented in Fig.3.

Operating Principle

The collector-emitter voltage (v_{CE}) corresponding to each IGBT is required for GDC. The series connected IGBT system in Fig.4 consists of a resistor voltage divider circuit to measure v_{CE}. The output of voltage divider is further fed to the buffer and analog circuit based peak detection is used to measure peak voltage (v_{pk}) for each IGBT. For the case of turn-off condition, the gate signal corresponding to IGBT possessing higher v_{pk} is delayed to suppress the unbalancing.

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3. Experimental Validation

The series connected IGBT system in Fig.4 was developed for experimental validation of the GDC using photocoupler-based gate driving unit to realize AVB. The controlled digital gate drive signals generated considering a unit time delay adjustment of 10ns corresponding to each iteration.

Initially, significant dynamic unbalancing occurred in v_{CE} as shown in Fig.5 during turn-off. The same current flowed through the devices as given in eq. (1). The device current consists of hole current (j_{holes}) and displacement current (j_{disp}) as shown in eq. (2). The devices possess unequal current components as presented in eq. (3).

$$j^1 = j^2 \ (for\ series\ connected\ devices) \quad (1)$$

$$j^1_{holes} + j^1_{disp} = j^2_{holes} + j^2_{disp} \quad (2)$$

$$j^1_{holes} < j^1_{disp}\ therefore\ j^1_{disp} > j^2_{disp} \quad (3)$$

IGBT1 has a lower hole current, which result in higher displacement current. Higher displacement current causes a higher rate of change of electric field, which consequently leads to an overshoot in v_{CE} during turn-off, as demonstrated in Fig.5. In addition, the switching overshoot time of v_{CE} is governed by the junction capacitance and parallel resistances used for voltage divider circuit for each IGBT devices.

The stored hole carriers of IGBT2 are reduced by delayed switching of IGBT1 to balance the j_{holes} which ultimately leads to more balanced j_{disp}. After 2nd iteration, the devices have an almost uniform voltage distribution (unbalancing <5%) as well as minimized peak overshoot as shown in Fig.6.

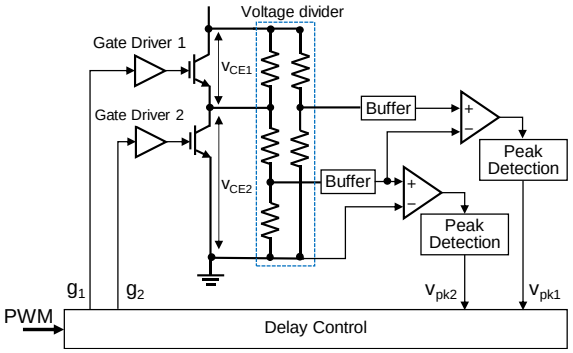

Fig. 4 Series connected IGBT system for the experimental implementation of the GDC.

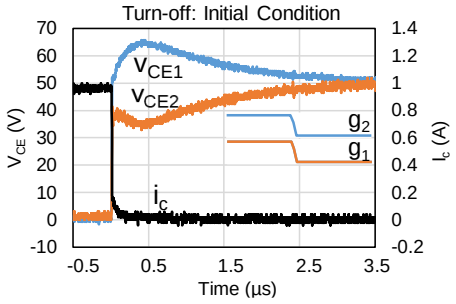

Fig. 5 Turn-off waveforms without GDC: unbalanced voltage stress.

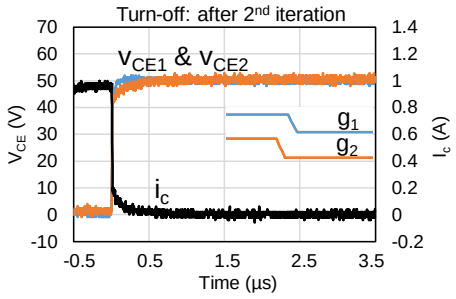

Fig. 6 Turn-off waveforms with GDC: balanced voltage stress.

4. Conclusions

In this abstract, the peak detection based GDC is implemented for two-series connected IGBT devices. The balanced voltage stress distribution is achieved using GDC. The implementation of GDC based on the highest peak is crucial in minimizing overshoot voltage to prevent the device breakdown.

Acknowledgments

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