Numerical Study of 4H-SiC PiN Diode to Enable Forward Bias Degradation Prediction Considering BPD-TED Conversion Position in the SiC Epitaxial Wafer

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Abstract

Forward bias degradation caused by basal plane dislocations (BPDs) in the substrate is the critical issue in the SiC bipolar devices operated under high current density conditions. In this work, we proposed the calculation model of the current density in the PiN diode using the injection hole density at the buffer/substrate interface to enable the forward bias degradation prediction. We found out the critical current density which occurs stacking faults expansion from BPDs at buffer/substrate interface could be improved by shortening the carrier lifetime of the substrate or densifying the dopant concentration of the buffer layer. In the case of the conversion of BPD to threading edge dislocation (TED) located inside the SiC substrate, we estimated more than twice improvement of critical current density using the BPD-TED conversion effect of the Si-vapor etching process.

1. Introduction

Basal plane dislocations (BPDs) in the SiC epitaxial wafer expand to single Shockley stacking faults (SSFs) under the forward bias operation in the SiC bipolar devices, resulting in an increase in on-voltage called the forward bias degradation[1]. Generally, BPDs in the SiC substrate can be mostly converted to harmless threading edge dislocations (TEDs) at the epi/substrate interface with the progress of epitaxial growth technology, and can eliminate BPDs in the epitaxial films. However it has been reported that the SSF expansion occurs when excess carriers reach the BPD in the substrate under high current conditions. According to ref[2], the critical injection hole density for the SSF expansion originating the BPD in the substrate is reported about 1.6-2×10^{16} cm^{-3} at the buffer/substrate interface.

In this study, we aim to propose the model to enable predict the forward bias degradation caused by BPDs numerically in the PiN diode structure and to describe the current density from the injected hole density at the buffer/substrate interface. In addition, we estimate the critical current density of the forward bias degradation in the case of a BPD-TED conversion located in the substrate. Calculation of the critical current density is performed by taking BPD-TED conversion in the Si-vapor etching (Si-VE) method[3-4] as an example.

2. Device structure and physical models for calculation

Fig.1 shows the schematic cross-sectional structure of a typical SiC PiN diode. In this study, our calculation model of current density and carrier density were designed for the drift, buffer and substrate regions as shown in Fig.2. We introduced physical models of the dopant ionization[5], the bandgap narrowing (BGN) effect[6], and the Caughey-Thomas mobility model[7] for 4H-SiC.

The hole density at the bottom of the buffer layer is defined as p_i. The hole current density (J_p) can be determined from the mass action law at the buffer/substrate interface, the diffusion length ($L_{p(\mathrm{sub})}$) and the diffusion constant ($D_{p(\mathrm{sub})}$) in the substrate. J_p is expressed as shown equation (1) using p_i,

$$J_p = \frac{qD_{p(\mathrm{sub})}}{2L_{p(\mathrm{sub})}}\left(-N_{\mathrm{sub}} + \sqrt{N_{\mathrm{sub}}^2 + 4p_i(p_i + N_{\mathrm{buffer}})\exp\left(\frac{\Delta E_{g(\mathrm{sub})} - \Delta E_{g(\mathrm{buffer})}}{kT}\right)}\right), \quad (1)$$

where N_{buffer}, N_{sub}, $\Delta E_{g(\mathrm{buffer})}$ and $\Delta E_{g(\mathrm{sub})}$ are the ionized donor concentration of the buffer layer, the ionized donor concentration of the substrate, BGN in the buffer layer and BGN in the substrate, respectively. $L_{p(\mathrm{sub})}$ is adjusted in the range of 1 ns to 8 ns at 298 K to 498 K. The electron and hole density in the drift layer can be described using J_p and p_i by calculating similarly at the drift/buffer interface, as shown in equation (2) and (3),

$$p_{\mathrm{drift}} = \frac{-N_{\mathrm{drift}} + \sqrt{N_{\mathrm{drift}}^2 + 4\left(p_i + \frac{Jpt_{\mathrm{buffer}}}{qD_{p(\mathrm{buffer})}}\right)\left(p_i + \frac{Jpt_{\mathrm{buffer}}}{qD_{p(\mathrm{buffer})}} + N_{\mathrm{buffer}}\right)\exp\left(\frac{\Delta E_{g(\mathrm{buffer})} - \Delta E_{g(\mathrm{drift})}}{kT}\right)}}{2}, \quad (2)$$

$$n_{\mathrm{drift}} = \frac{N_{\mathrm{drift}} + \sqrt{N_{\mathrm{drift}}^2 + 4\left(p_i + \frac{Jpt_{\mathrm{buffer}}}{qD_{p(\mathrm{buffer})}}\right)\left(p_i + \frac{Jpt_{\mathrm{buffer}}}{qD_{p(\mathrm{buffer})}} + N_{\mathrm{buffer}}\right)\exp\left(\frac{\Delta E_{g(\mathrm{buffer})} - \Delta E_{g(\mathrm{drift})}}{kT}\right)}}{2}, \quad (3)$$

where t_{buffer}, $D_{p(\mathrm{buffer})}$ and $\Delta E_{g(\mathrm{drift})}$ are the thickness of buffer layer, the diffusion constant in the buffer layer and BGN in the drift layer, respectively. The total current density (J) can be estimated by calculating the electron current density (J_n) from J_p and mobility.

$$J_n = \frac{\mu_{n(\mathrm{drift})} n_{\mathrm{drift}}}{\mu_{p(\mathrm{drift})} p_{\mathrm{drift}}} J_p, \quad J = J_p + J_n. \quad (4)$$

Here, the critical hole density (p_{crit}) which occurs SSFs expansion from BPDs at the buffer/substrate interface adopted 1.6×10^{16} cm^{-3} from the experimental value in ref[2]. Calculated J at p_i=p_{crit} is defined as a critical current density, J_{crit}. Temperature dependence is considered for all numerical parameters except for p_{crit}.

3. Results and discussion

Fig.3 shows the calculated current density J corresponding to the hole density at buffer/substrate interface p_i at different temperature. The calculations were performed using PiN diode structure parameters described in ref [2]. Open and close diamond symbols are plots of values estimated from the same reference. It was confirmed that calculated values almost similar to J in ref [2] is obtained.

Fig.4 shows the J_{crit} as a function of the dopant concentration of the buffer layer at different temperature. In this case, the structure of the PiN diode is calculated as the 10μm thick drift layer with donor impurity concentration of 1.0×10^{16} cm^{-3}, the 0.5μm thick buffer layer, and the substrate with donor impurity concentration of 5.0×10^{18} cm^{-3}. It can be seen that J_{crit} strongly depends on the buffer concentration, and greatly increases in the high concentration region.

Fig.5 shows the J_{crit} as a function of the carrier lifetime of the substrate at different temperature used buffer layer with donor impurity concentration of 1.0×10^{18} cm^{-3} in addition to the same structural parameters in Fig.4. It is suggested that lowering the substrate lifetime can increase J_{crit}, that is to say, it is sufficient to lower the lifetime of the substrate without promoting carrier recombination in the buffer layer.

We also estimated J_{crit} for the BPDs converted to TEDs in the substrate. Here, the depth d of 140 nm underneath the buffer/substrate interface (as shown in Fig.6) was used as the BPD-TED conversion effect by Si-VE[8]. Equation (5) shows p_i when p_{crit} reaches the conversion depth d.

$$p_i = \frac{-N_{\mathrm{buffer}}+\sqrt{N_{\mathrm{buffer}}^2+4p_{crit}\left(p_{crit}\exp\left(\frac{d}{L_{p(\mathrm{sub})}}\right)+N_{sub}\right)\exp\left(\frac{d}{L_{p(\mathrm{sub})}}+\frac{\Delta E_{g(\mathrm{buffer})}-\Delta E_{g(\mathrm{sub})}}{kT}\right)}}{2}. \quad (5)$$

J_{crit} is similarly calculated using equations (1)-(4). Fig.7 shows the J_{crit} with dependence of dopant concentration of buffer at different temperature and d. We confirmed that the J_{crit} increased more than twice even under conditions of the low dopant concentration of buffer or high temperature compared to the conversion at the buffer/substrate interface.

4. Conclusions

We proposed the model for the current density using the injected hole density at the buffer/substrate interface in the SiC PiN diode and calculated J_{crit} with various structural parameters including the case of BPD-TED conversion located inside the SiC substrate. The improvement of J_{crit} by the BPD-TED conversion inside the SiC substrate is shown, which is estimated more than twice in the case of Si-VE.

References

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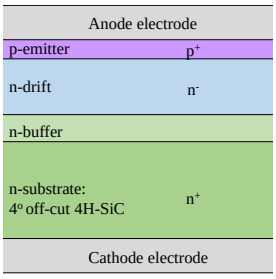

Fig. 1 Schematic cross-sectional structure of SiC PiN diode for this study.

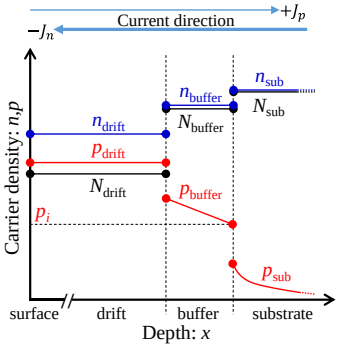

Fig. 2 Carrier density distribution model in the drift, buffer, and substrate.

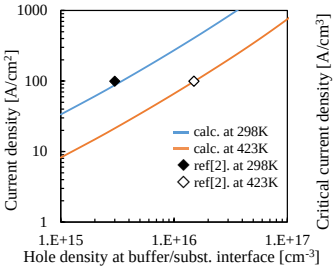

Fig. 3 Calculated current density corresponding to hole density at buffer/subst. interface.

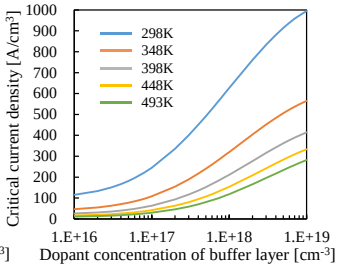

Fig. 4 J_{crit} as a function of dopant concentration of buffer layer at different temperature.

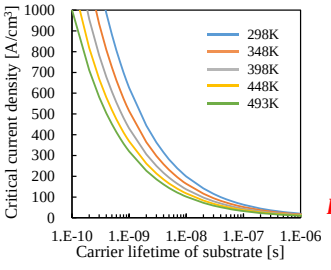

Fig. 5 J_{crit} as a function of carrier lifetime of substrate at different temperature.

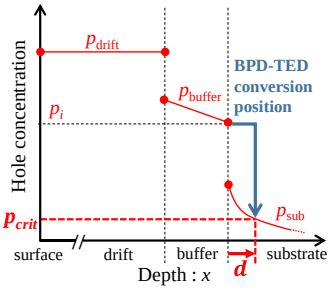

Fig. 6 Case of BPD-TED conversion located inside the substrate and displacement of p_{crit}.

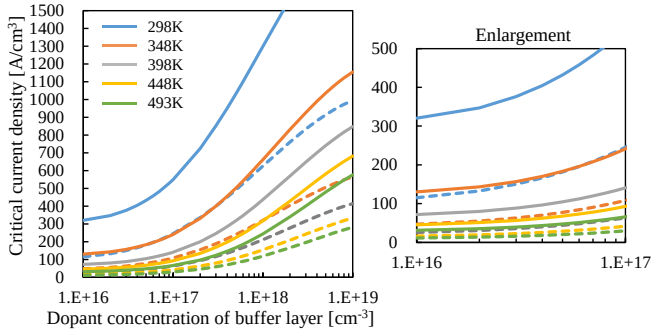

Fig. 7 J_{crit} with dependence of dopant concentration of buffer layer at different temperature and BPD-TED conversion depth. Solid lines: converted inside the substrate at depth of 140nm. Dashed lines: converted at buffer/subst. interface (same as Fig.4).