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Vernier ring based pre-bond through silicon vias test in 3D ICs

Tianming Ni[1], Mu Nie[2], Huaguo Liang[1,2a)], Jingchang Bian[1], Xiumin Xu[1], Xiangsheng Fang[2,3], Zhengfeng Huang[1], and Xiaoqing Wen[4]

[1] *School of Electronic Science & Applied Physics, Hefei University of Technology, Hefei, China*

[2] *School of Computer and Information, Hefei University of Technology, Hefei, China*

[3] *Department of Information Project, Anhui Institute of Economic Management, Hefei, 230051 China*

[4] *Department of Creative Informatics, Kyushu Institute of Technology, Fukuoka 820–8502, Japan*

a) *huagulg@hfut.edu.cn*

Abstract: Defects in TSV will lead to variations in the propagation delay of the net connected to the faulty TSV. A non-invasive Vernier Ring based method for TSV pre-bond testing is proposed to detect resistive open and leakage faults. TSVs are used as capacitive loads of their driving gates, then time interval compared with the fault-free TSVs will be detected. The time interval can be detected with picosecond level resolution, and digitized into a digital code to compare with an expected value of fault-free. Experiments on fault detection are presented through HSPICE simulations using realistic models for a 45 nm CMOS technology. The results show the effectiveness in the detection of time interval 10 ps, resistive open defects 0.2 kΩ above and equivalent leakage resistance less than 18 MΩ. Compared with existing methods, detection precision, area overhead, and test time are effectively improved, furthermore, the fault degree can be digitalized into digital code.

Keywords: 3D IC, TSV, pre-bond, testing, time interval, digital code

Classification: Integrated circuits

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1 Introduction

The advent of three-dimensional integrated circuit (3D IC) technology has opened up the potential of highly improved circuit designs. Through silicon vias (TSVs) enable the vertical integration of separate dies to form a single 3D chip. The TSV-based 3D stacking technology promises better performances, including smaller footprint, higher bandwidth, lower power and higher interconnect density. However, concerns about the 3D IC yield constitute one of the key obstacles for widespread industry adoption of 3D integration technology [1]. Defects in TSVs due to fabrication steps decrease the yield of 3D ICs, hence these defects need to be screened early in the manufacturing flow. Inevitably, TSV testing in pre-bond stage, plays a critical role to guarantee the overall yield, which devoted to detecting TSV defects early.

However, pre-bond TSV testing is very challenging. During TSV formation, new defects would occur, including micro-voids due to insufficient filling and pinholes through the isolation layer surrounding TSVs, as shown in Fig. 1 [2]. Furthermore, before wafer thinning, TSVs are buried in silicon and are only indirectly accessible at their front side through the circuitry connected to the TSVs. A probe based pre-bond TSV testing method is presented in [2], in which multiple TSVs are mechanically contacted by the same probe needle to measure TSV capacitance and resistance, and this approach can detect stuck-at and leakage faults. However, this method has several drawbacks. Firstly, probing techniques require extra logic leading to considerable area overhead. Furthermore, even though the back side of the TSVs is exposed after wafer thinning, contact based probing of TSV arrays without damaging TSVs is still difficult. Mechanical force on TSV tips and micro-bumps can result in damage to TSVs, leading to their degraded performance or even failure. As an alternative to probe testing, built-in self-test (BIST) approaches have been developed [3, 4, 5, 6, 7].

In this work, we propose a novel pre-bond TSV testing method, using a technique named Vernier Ring (VR). We can detect resistive-open and leakage faults with high resolution in picosecond level, and digitize the fault degrees into

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specific digital code. To the best of our knowledge, little research has focused on the TSV testing based on the VR scheme. The technical merits include the following.

1) The proposed VR test method not only supports testing but also digitizes the degree of resistive open and leakage fault into a specific digital code. In addition, this scheme has the characteristic of a relatively high resolution in picosecond level.

2) The proposed VR based pre-bond TSV testing method is contactless, no TSV probing with external equipment is necessary and the test cost is low. In addition, the VR circuit can be shared by multiple TSVs, thus the design for testability (DfT) area overhead is much minimized.

3) Unlike the previous approaches that often utilize some analog or custom circuit, the VR method only uses digital logic gates to allow easy integration with design flow.

The reminder of this paper is organized as follows. Section 2 presents the electrical model of TSVs and related prior works. The detailed VR test scheme is illustrated in Section 3. The corresponding experiments will be elaborated in Section 4. Finally, we conclude this work in Section 5.

2 Related works

This section will illustrate the TSV electrical parameter models first, and related prior works will be described later.

2.1 Electrical models of TSVs

Fig. 1(a) shows a simplified, schematic diagram of a single die with a TSV structure. During manufacturing, new defects will exist in TSVs, especially micro-voids in the TSV filling material and pinholes through the isolation layer surrounding TSVs, as shown in Fig. 1(b) [3]. In this paper, we focus our attention on these two types of TSV defects.

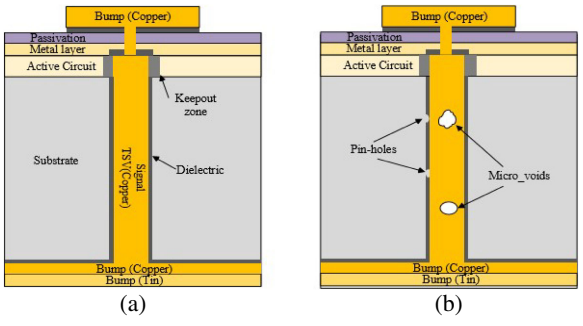

Fig. 1. Schematic of TSV structures: (a) fault-free, (b) faulty.

For simplicity without losing generality, a lumped RC model to represent a TSV has been widely presented in previous works [4], where R is the TSV resistance and C is the parasitic capacitance between the TSV and the substrate. R is generally neglected in the pre-bond phase, and a simplified model is considered (see Fig. 2(a)).

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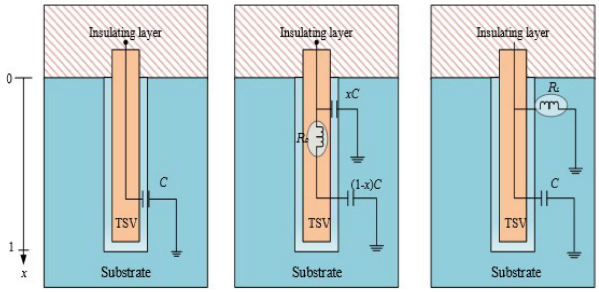

Fig. 2. TSV models: (a) fault-free, (b) micro-void, (c) pinhole.

During TSV fabrication, new manufacturing defects might occur, including micro-voids and pinholes. From a perspective of electrical effect, most TSV defects can be categorized into two main groups: resistive open and leakage faults.

Micro-voids due to insufficient TSV filling increase the TSV resistance at the defect location and thus can be modeled as a resistive open fault as shown in Fig. 2(b). This defect divides the TSV capacitance into two segments: top segment ($[0, x]$) with its capacitance xC; bottom segment ($[x, 1]$) with its capacitance $(1 - x)C$. The location x of the void is possibly ranging from 0 to 1. The worse the resistive open is, the greater R_O would be. An infinity R_O indicates that the TSV becomes full-open.

Pinholes due to silicon side wall imperfection create a conduction path from the TSV to the substrate (often connected to ground), and can be modeled as a leakage fault as shown in Fig. 2(c). The leakage is modeled by the resistor R_L. The worse the leakage fault is, the smaller R_L would be. Since leakage faults tend to deteriorate, which is a serious concern for lifetime chip reliability.

2.2 Related prior works

Minki et al. [5] proposed a voltage dividing (VD) technique to detect TSV resistive open fault. This approach utilizes a TSV-test-inverter (TTI) to connect TSV, which forms a resistor divider cell between the PMOS resistance of the TTI and the TSV resistance. This scheme needs extra analog or custom circuitry and the measurement precision is not high as far as possible. Huang et al. [6] adopted a CAF-WAS (charge-and-float, wait-and-sample) method to detect TSV leakage fault. A leakage test threshold (LTT) was involved, which is defined as the leakage current value beyond which a TSV will be declared as faulty. This technique can be done in only logic gates, making it easy for the common design flow.

In [3, 7], both resistive open and leakage faults can be detected by creating ring oscillator (RO), which contains TSV drivers, receivers and extra inverters in each ring. Deviations in TSV parameters lead to variations in the propagation delay of the net connected to the TSV and thus variations in the oscillation period. By capturing the oscillation in each case, faulty TSVs can be indirectly diagnosed. And the oscillation period is captured thanks to extra binary counters that use the oscillating signal as clock.

The methods above can detect faulty TSVs, but unable to quantify the degree of faults. To overcome this problem, Liang et al. [4] proposed a technique named

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pulse shrinkage (PS), which can generate digital codes to manifest the faulty degrees. In this scheme, a pulse becomes the input signal, and there are several shrinkage cells in the test path. The faults in each TSV will cause the deviation of the rise/fall times of each shrinkage cell. The pulse signal visiting the shrinkage cell will be shrunk by a definite amount of width per cycle until it vanishes completely. As a result, the output counter record the location where the pulse signal vanishes and then encoded into a corresponding digital code. However, this technique requires that the pulse width must be less than loop delay, thus the dynamic range is not large.

Since the propagation delay caused by TSV RC parameter deviations spreads in the picosecond level, if the precision is not high as far as possible, then some subtle variations in TSV may be masked. In addition, the faulty TSVs may have different degrees, thus it is necessary to divide faulty TSVs into several degrees. In the next section, a novel BIST scheme will be presented for pre-bond TSV testing with picosecond-level high resolution, which also supports fault degree digitization.

3 Vernier ring based TSV testing

In this section, Vernier scheme for TSV testing will be presented. Firstly, the principle of the Vernier delay line is illustrated. Then a modified method based on Vernier ring will be applied for pre-bond TSV testing.

3.1 Vernier delay line

As one kind of time-to-digital converter (TDC), the Vernier Delay Lines (VDLs) have been widely used to precisely measure the time interval between two events and quantize it into digital code [8]. Two delay lines, with a pre-defined cell delay difference, are used for interval time measuring as shown in Fig. 3. Suppose that the two input signals are Start and Stop. The Start signal is prior to the Stop signal, and fed into the delay line where the propagation delay of each delay cell is t_s. Once there arrives the Stop signal, it goes to another delay line with a shorter cell delay t_f ($t_f < t_s$). Because the Stop signal lags the Start signal and the Stop signal is used as the sampling clock of the D flip-flops (DFFs), then the DFF will hold a logic-high value. On the other hand, when the Stop signal leads the Start signal, the DFF will hold a logic-low value. Since the Start signal propagates slower than the Stop signal, the Start signal will be caught up sooner or later, and the output of the sampling DFFs will be toggled from 1 to 0, then the VDL will be turned off ever

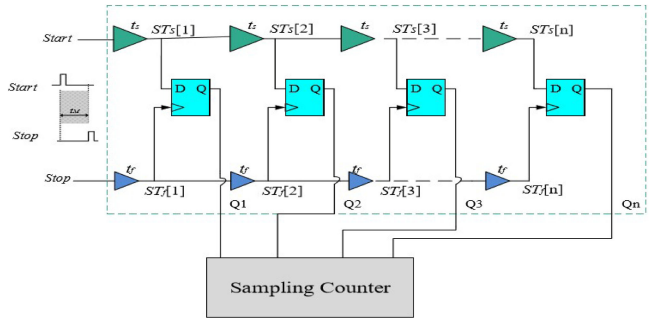

Fig. 3. The Vernier delay line.

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since. After propagating a delay cell, the time interval will be decreased by $(t_s - t_f)$, thus the effective time resolution R equals to the cell delay difference, $R = t_s - t_f$. This method can achieve sub-gate-delay resolution with picosecond level.

3.2 Vernier ring test scheme

As discussed previously, TSV during pre-bond stage, buries one end in the substrate, leaving the other end accessible, which constitutes one major challenge for pre-bond TSV testing. To address the test accessibility issue, a new structure called the I/O TSV cell with a pair of inverters and a TSV is shown in Fig. 4. INV1 and INV2 are used as TSV driver and receiver respectively. When the input signal is rise-edging, the TSV under test will be in a discharging condition.

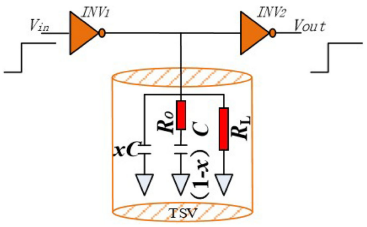

Fig. 4. I/O TSV cell.

Compared with fault-free TSV, open fault will divide the TSV capacitance into two segments, which helps TSV to discharge, thus reduce propagation delay. For leakage fault, the propagation delay will be reduced as well, because it creates a conduction path from the TSV to the substrate, which will accelerate TSV to discharge. Defects in TSV will lead to variations in the propagation delay of the net connected to the faulty TSV, and will generate a time interval with fault-free TSV, as shown in Fig. 5. Bringing the wisdom of time interval measurement, these variations can be measured by the Vernier delay lines as discussed previously. As is shown in Fig. 5, the faulty TSV tends to lead the fault-free one by a interval, thus the faulty TSV should be connected to the slow line of VDL.

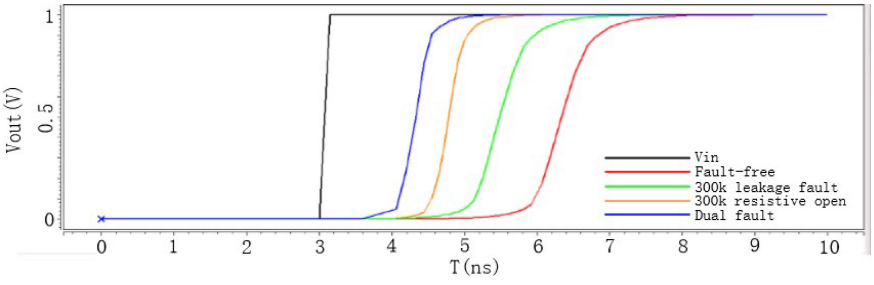

Fig. 5. I/O cell rise time for the fault-free case and faulty cases.

Though the VDL offers good time resolution, and take less time to measurement, however, once the time interval under measurement is large, the area overhead is huge. To solve this problem, a modified VDL is presented, which places the Vernier delay cells in a ring format such that the delay chains can be reused for measuring large time intervals. Unlike the Vernier delay line format described above, the output of the last stage of the VDL is looped back to the first

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stage. Hence, the number of delay stages required in each ring will shut down, as compared to the linear implementation [8].

Buffers were used as the delay cells to construct the VR in a standard digital process. Connecting the outputs of the last delay cells of a VDL to the inputs of the first pair of delay cells constructs a novel VR. Assume Ns (designed manually) delay elements are used to form the rings. Recall that a NAND gate replaces a buffer as the first delay cell and is used to input the signals under test. The rising edge of a signal to be measured can be fed into the delay ring through one of the inputs of the NAND gate. The pair of NAND gates in the two rings are well matched with the same propagation delay.

The VR consists of two chains of D flip-flops (DFFs) with different types, type A and type B, which operate in odd laps and even laps, respectively. In Fig. 6, DFF type A is triggered by a rising edge while DFF type B is triggered by a falling edge. Recall that the VR contains several buffers and a NAND gate, thus a rising edge becomes a falling edge after one lap of propagation along the ring. When input a rise-edge signal, for the first lap, DFF type B will be used; while for the second lap, DFF type A will be effective actually, and so on. DFFs record the arrival sequence of lead and lag signals and detect the location where the lag signal catches up with the lead signal.

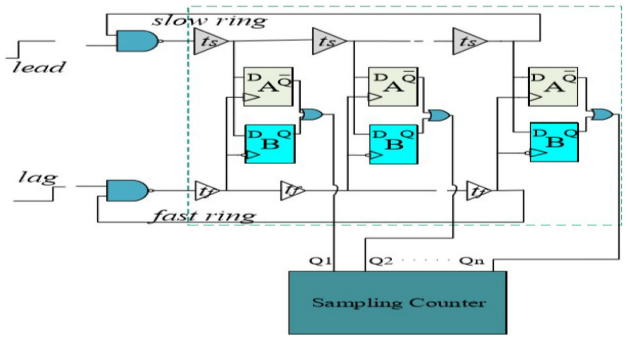

Fig. 6. TSV test architecture based on Vernier ring.

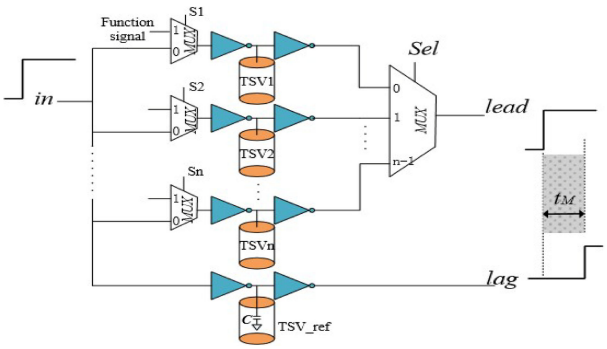

Fig. 7. Pre-logic unit.

The lead signal should be steered to the slow ring, while the lag signal goes to the fast ring. Otherwise, the lag signal will never catch up with the lead signal and the VR will not work. As illustrated in Fig. 5, the signal through defective TSV is prior, thus the defective TSV under test goes to the slow ring, while fault-free TSV is placed in the fast ring. As Fig. 7 shows it, the Vernier ring can be shared by

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multiple TSVs under test via an N-to-1 multiplexer, and one TSV will be measured according to the signal sel. The multiplexers are controlled by the test enable signals $S1 \ldots Sn$ to do selections between the operation signal coming from the internal logic and the rise edge of the test transition signal in. If $S1 = S2 = \ldots = Sn = 1$, all the multiplexers select the functional operation signal, then the circuit is in normal operating mode. If $S1 = 0$, $S2 = \ldots = Sn = 1$, the circuit is configured into TSV1 test mode. The signals Sel can select which TSV is under test, and the receiver of the TSV under test will be connected to the input of the VR test module. Assume 16 TSVs are sharing one test circuit, then signal *Sel* needs 4-bit selection code. The pre-logic unit will output a lead and lag signal with the time interval t_M for measurement via Vernier ring core.

4 Experimentation and results

4.1 Test setup

We verified our approach through HSPICE simulations, for which we used the TSV models described in Section 2 and the 45 nm Predictive Technology Model (PTM) [9]. Each cyclic delay line (either slow ring or fast ring) is composed of 8 delay cells ($Ns = 8$) plus extra 2 balanced inverters used as TSV driver and receiver respectively. All these gates come from the Nangate 45 nm Open Cell Library [10]. To verify the Vernier Ring scheme, we design the delay cell pairs in each ring by setting the resolution $R = 10$ ps.

In our experiments reported below, we consider the following TSV parameters: diameter = 10 µm, height = 75 µm and thickness = 1 µm for an equivalent capacitance of 200 fF, based on the model presented in [7]. This value is considered as the reference value for a fault-free TSV. We set the typical supply voltage $V_{DD} = 1$ V.

4.2 Detection of micro-void

As detailed in Section 2.1, micro-voids are characterized by their location x in the TSV and the resistance of the void, which can vary from few Ω (i.e. micro-void) to infinity (i.e. full-open). These two parameters are used for exploration of the void detection range.

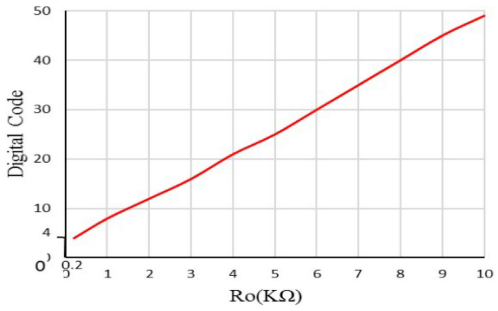

Fig. 8. Digital code versus the resistive open faults (R_O).

From a perspective of electrical effect, TSV defect caused by micro-voids can be considered as resistive open fault. We simulate a resistive open fault at the location x = 0.5 in TSV with its capacitance value of 200 fF as depicted in Fig. 2(b). We sweep R_O from 0 kΩ (no fault) to 10 kΩ (strong resistive open) at

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the typical supply voltage VDD = 1 V. With this model, we perform transient analysis and record the digital code. The worse the resistive open is, the larger R_O will be, and this accelerates TSV to discharge, leading to an increased time interval, and the digital code will be larger at the same time. Fig. 8 shows the obtained digital code in case of a resistive open fault. As expected, an increase in the resistance R_O leads to an increase of digital code. This indicates that we can detect resistive opens of a sufficient size by directly measuring the digital code. Since the resolution of this proposed VR scheme is 10 ps, it determines the minimum resistive open resistance $R_{voidcrit}$ identified. According to our experimental results, open resistances higher than 0.2 kΩ can be detected by means of the proposed approach. Thus $R_{voidcrit}$ identified in our scheme can reach 0.2 kΩ with the digital code staying at 4, and it is assumed to be no open fault if R_O is less than 0.2 kΩ. The fault severity can be illustrated by digital code as well, the higher R_O is, the worse the resistive-open fault is, and the greater the digital code value will be.

4.3 Detection of pinhole

As detailed in Section 2.1, pinholes can be modeled as a leakage fault as shown in Fig. 2(c). Leakage faults exhibit a different behavior from resistive open faults. To show this, we use the same simulation approach as described above. As discussed in Section 3.2, the leakage fault helps the TSV to discharge and cause an increased time interval for measurement, and the corresponding digital code obtained should be greater as well. Fig. 9 shows the relationship between digital code obtained and the leakage resistance R_L. Firstly, we observe that the digital code reduces from 86 to 4 as the leakage resistance increases, which makes them distinguishable from the fault-free case as well as resistive open faults. Normally, it is also difficult to distinguish a TSV with a small leakage fault (large leakage resistance R_L) from a fault-free one. When the leakage resistance R_L increases from 18 MΩ to 20 MΩ, the digital code stayed at 4 unchanged, which indicates that the leakage current is too small to be detected in this case. Hence, in our scheme, the minimum leakage fault resistance $R_{leakcrit}$ identified can reach 18 MΩ. All the pinhole defects with $R_L \leq 18$ MΩ are detected. For larger resistances, the test result does not allow to distinguish fault-free TSV from those TSVs with leakage faults. Different from the resistive-open case described above, the worse the leakage fault is, the lower the R_L is, and the corresponding digital code will be greater, thus the digital code can reflect the leakage fault severity as well.

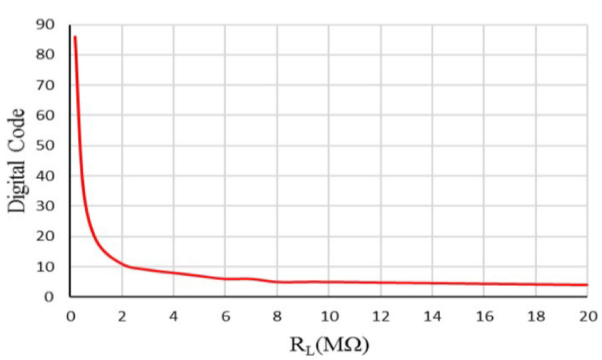

Fig. 9. Digital code versus leakage faults (R_L).

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4.4 Area and test time overhead

Compared with linear delay lines, the looped delay line in ring format can save the area overhead. In the proposed scheme, there does not need any extra analog circuit, and all gates come from the Nangate 45 nm Open Cell Library [9]. The overall overhead is calculated and presented in Table I. In our design, each cyclic delay line (either slow ring or fast ring) is composed of 8 delay cells (Ns = 8) plus extra 2 balanced inverters used as TSV driver and receiver respectively. Note that the DFF B in the proposed scheme was used to detect falling edge, then one additional inverter was added at the input of each DFF B (8 DFF Bs in our scheme, leading to 8 additional inverters). In addition, our scheme needs two NOR gates, each NOR gate consists of an OR gate and one inverter, and the OR gate can be detached from the Nangate library, thus two additional inverters should be added. Assume that 16 TSVs share one test circuit, each TSV needs two inverters to be used as drivers, leading to $2 * 16 = 32$ additional inverters. As a result, the number of additional inverters is $2 * 16 + 2 + 8 = 42$. The DfT circuitry occupies an area of $42 * 0.532 + 2 * 0.798 + 16 * 1.862 + 15 * 1.862 + 8 * 0.798 + 8 * 0.798 + 8 * 1.064 + 16 * 4.788 = 179.55\ \mu m^2$. Generally, taken the TSV pitch and the KOZ into account, one TSV occupies a square area of up to $1600\ \mu m^2$ approximately [4]. Therefore, the DfT area overhead can be negligible compared with one single TSV area overhead. In addition, the proposed TSV test method can be utilized to test multiple TSVs with the individual test module. Assume 16 TSVs share one test circuit, then the average area overhead per TSV is about $11.22\ \mu m^2$.

Table I. Area overhead

Gate	Number	Layout Area (μm^2)
INVERTER	42	0.532
NAND	2	0.798
MUX2_1	16	1.862
MUX16_1	15*	1.862
BUF(ts)	8	0.798
BUF(tf)	8	0.798
OR	8	1.064
DFF(A, B)	16	4.788
Total Area (μm^2)		179.55

The time needed to test a TSV as described in the example above is estimated as follows:

1. Initialization: It takes only one clock cycle to reset all DFFs to '0'.

2. Selection: Since 16 TSVs are bundled as a group for testing, then the signal Sel occupies 4-bit selection code in our scheme. It takes 4 clock cycle to select a TSV for testing through configuring the MUXs.

3. Measurement: Perform the TSV test for all TSVs by giving the signal in a raising edge. It takes one clock cycle to finish fault measurement for the selected TSV and the results are stored in the DFF temporarily.

4. Scan out: In our scheme, the experimental results show that the maximum digital codes are less 90 for both open and leakage fault detection cases. Thus, it

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takes 7 clock cycle at most to read out the test results in the form of digital codes. In summary, each TSV requires at most 13 clock cycles for testing. Therefore, the test time of each TSV is 0.65 µs when 20 MHz test clock is used.

4.5 Comparison of pre-bond TSV BIST methodologies

Finally, the proposed method is more comprehensive compared with the existing techniques in terms of fault type, measurement range, area overhead, test time and fault degree digitization. To ensure the fairness of comparison, the same method is used to calculate the area and time overhead of the methods participating in the comparison in this paper. The results are summarized in Table II. It is obvious that the proposed scheme can achieve relatively higher resolution. The method can detect the resistive open resistance 0.2 kΩ above and equivalent leakage resistance less than 18 MΩ. Furthermore, the presented scheme supports not only testing but also digitizes the fault degree of resistive open and leakage faults into a specific digital code. And the DfT area overhead can be negligible compared with one single TSV area overhead. In addition, the test time is also optimized compared with previous schemes.

Table II. The comparison of pre-bond TSV BIST methodology

Work	Fault type	$R_{voidcrit}$	$R_{leakcrit}$	Area (μm^2)	Test time (µs)	Fault type
[5]	Open	>kΩ	undetected	NULL	NULL	NO
[6]	Leakage	undetected	~4 MΩ	92.7	8	NO
[2]	Open, leakage	~kΩ	~kΩ	20	1.5	NO
[7]	Open, leakage	~kΩ	~kΩ	49	3.2	NO
[4]	Open, leakage	~kΩ	~MΩ	75.54	NULL	Yes
This work	Open, leakage	200 Ω	18 MΩ	11.22	0.65	Yes

5 Conclusion

A versatile pre-bond TSV test method should be able to adapt to different test thresholds, TSV sizes and fault degrees. Existing methods fail to achieve such a one-method-fits-all ideal. A novel BIST solution based on Vernier Ring (VR), achieving picosecond testing resolution, is presented in this paper. With its accurate resolution, the method can detect the resistive open resistance 0.2 kΩ above and equivalent leakage resistance less than 18 MΩ. Furthermore, the presented scheme supports not only test but also digitizes the fault degree of resistive open and leakage faults into a specific digital code. With its high flexibility and no extra analog circuits, it can effectively diagnose resistive open and leakage faults in TSVs early during manufacturing testing, therefore improving the yield of 3D IC, reducing long-life failures.

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