A Universal Test Structure for the Direct Measurement of the Design Margin of Even-Stage Ring Oscillators with CMOS Latch

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Abstract

To validate our optimized design theory for Even Stage Ring Oscillators (ESROs), we have developed a Universal ESRO TEG (U-ESRO TEG) constructed with Equivalent Variable-W Transistors (EVWTs) and Initial-voltage Preset-able Inverters (IPIs). The design parameters can be changed with a single circuit, and it is possible to measure the operation margin and oscillation availability of an ESRO. Experimental results confirm the validity of our ESRO design theory.

1. Intoroduction

Even Stage Ring Oscillators (ESROs) are able to generate four phase clock with a single circuit, and are typically used in communication systems [1-3]. Figures 1(a)-(d) show examples of ESRO circuits. Figure 1(a) shows a circuit including a single CMOS latch inside the delay inverters, Figs.1(b) and (c) show ESROs with two latch, and Fig.1(d) has latches on all the stages. Because these ESROs are constructed with even stage delay inverters, they run the risk that oscillation may be stopped in certain circumstances depending on the design parameters of each transistor. Focusing on the similarity between ESRO and SRAM circuit topologies, we suggest an analytical technique for quantitatively deriving design parameters which enable secure stable oscillation by applying the Static Noise Margin (SNM) analysis used in SRAM circuits [4,5]. By applying this method, the operation margin can be quantitatively evaluated, and ESRO design parameters providing stable oscillation can be determined.

However, this method was formulated based on results from circuit simulations, and the validity of the method has not been tested by measuring an actual circuit. Therefore, we have developed a universal ESRO TEG (U-ESRO-TEG) which can emulate the necessary combinations of design parameters. The U-ESRO TEG enables measurement of the values of the operation margin and oscillation availability and thus validates themethod by actual measurement.

2. Design Margin Diagram (DMD) for ESRO

The evaluation of the conditions for stable oscillation in ESROs is made by using a Design Margin Diagram (DMD) as shown in Fig.2[6]. The procedure to create a DMD is outlined in Fig.3. First, a Static Noise Margin Evaluation Circuit (SNM-EC) is constructed, by extracting one delay inverter and CMOS latch stage that form an ESRO. Second, the SNM-EC is simulated by changing the gate width to plot three SNMs (RSNM (H), RSNM (L) and WSNM) forming the borderlines on the DMD. These borderlines divide the combination of design parameters into five regions shown as A to E in Fig.2. The availability of the oscillation is simulated with the ESRO circuit by changing the gate width, and then superimposing the results as the oscillation available region on the DMD. Kohara et al [6] predict that the design region where oscillation is available is that marked as A for the circuits shown in Figs.1 (a) and (b) and as A+C+D for the circuits shown in Fig.1 (c) and (d).

3. Design of the Universal ESRO TEG (U-ESROTEG)

3.1. Equivalent Variable-W Design

If the design margin diagram is obtained from experimental data with the method as shown in Fig.3, large numbers of SNM measurement circuits and ESROs can be designed. However, the number of circuits on the testing chip would be limited due to the available die area and the number of I/O pins. Therefore, we have replaced a MOSFET with an Equivalent Variable-W Transistor (EVWT) which consists of a current control MOSFET and

an active constant gate width MOSFET as shown in Fig.4. Since the current characteristic of the single MOSFET when changing the value W corresponds to the current characteristic of the EVWT when changing the control voltage, we have effectively emulated a MOSFET with a different W value simply by changing the control voltage instead of having to create several circuits with different W values. The developed circuit diagrams using the EVWT in the SNM measurement circuit and latch (Equivalent Variable-W Latch: EVWL) are shown in Fig.5 (a) and (b). The gate width of the latch inverter of each circuit is set by the control voltages (ncon and pcon).

3.2. Initial-voltage Preset-able Inverter (IPI)

Depending on the initial state, the ESRO may cause an unstable oscillation in spite of the lack of a design margin [6]. In the SPICE simulation, the initial state can be set with simple initial node-set descriptions. However, it is difficult to set the initial state of each node arbitrarily in the actual circuits. Therefore, we have developed an Initial-voltage Preset-able Inverter (IPI) shown in Fig. 6(a). Using the IPI, by setting the nodeset signal to Low, it is possible to output the preset signal directly, and by switching the nodeset signal to High, it starts to operate as inverter, as shown in Fig.6(b).

4. DMD by U-ESRO TEG Measurement

Figures 7 and 8 show the circuit diagram of the Universal ESRO TEG (U-ESRO TEG) and the chip photograph, respectively. Unlike the ESRO, the U-ESRO TEG employs IPIs instead of delay inverters and EVWLs instead of latch circuits. The EVWL can be disabled by setting a control voltage, and thus we are able to change the number of latches inside the U-ESRO TEG and thus fulfill all the circuit configurations described in Figs.1(a)-(d). Moreover, to make it easy to monitor from outside the chip; a signal will be output through the 1/64 frequency divider. Figure 9 summarizes the method of constructing a DMD using measurements from the U-ESRO TEG. First, by using the SNM measurement circuit with varying ncon and pcon, the three SNM borderlines are measured to create a temporary DMD (DMD_EVWL) in which the horizontal axis is the voltage of ncon and the vertical axis is the voltage of pcon. The initial state is set using the IPI and the availability of oscillation is measured using U-ESRO TEG. The region is then superimposed on the DMD_EVWL. Finally, DMD_EVWL is converted into the DMD using the relationship between the control voltage of the EVWT and the gate width value W of the simple MOSFET.

Figures 10(a)-(d) show the experimental results from the circuits shown in Figs.1(a)-(d). We are able to confirm that these measured results agree well with the theoretical predictions of Kohara et al [6]. To confirm the scalability of the EVWT design, we designed 45 simple ESROs with different gate widths for circuits of the type shown in Fig.1(a). The results are shown in Fig.10(a), and indicate that results from ESROs match the results from U-ESRO TEG.

5. Conclusion

We have developed a U-ESRO TEG with EVWT and IPIs to evaluate the design margins of various ESROs with single TEG. The measured DMD of the U-ESRO TEG matches the both theoretical prediction and simple ESRO measurement, so that we successfully proved the validity of our designing method by using the U-ESRO TEG.

Acknowledgments

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References

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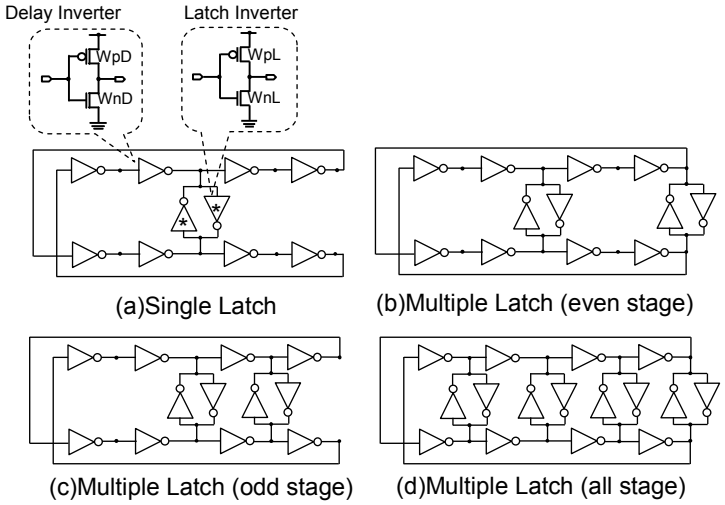


Fig.1: Even Stage Ring Oscillators (ESROs)

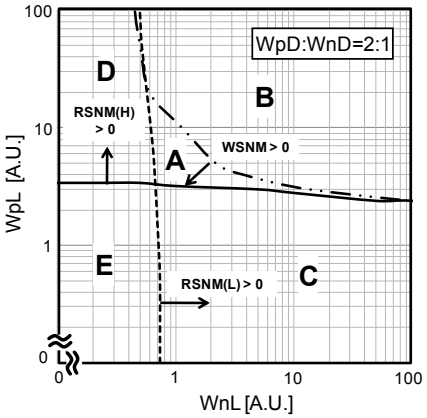


Fig.2: Design Margin Diagram (DMD)

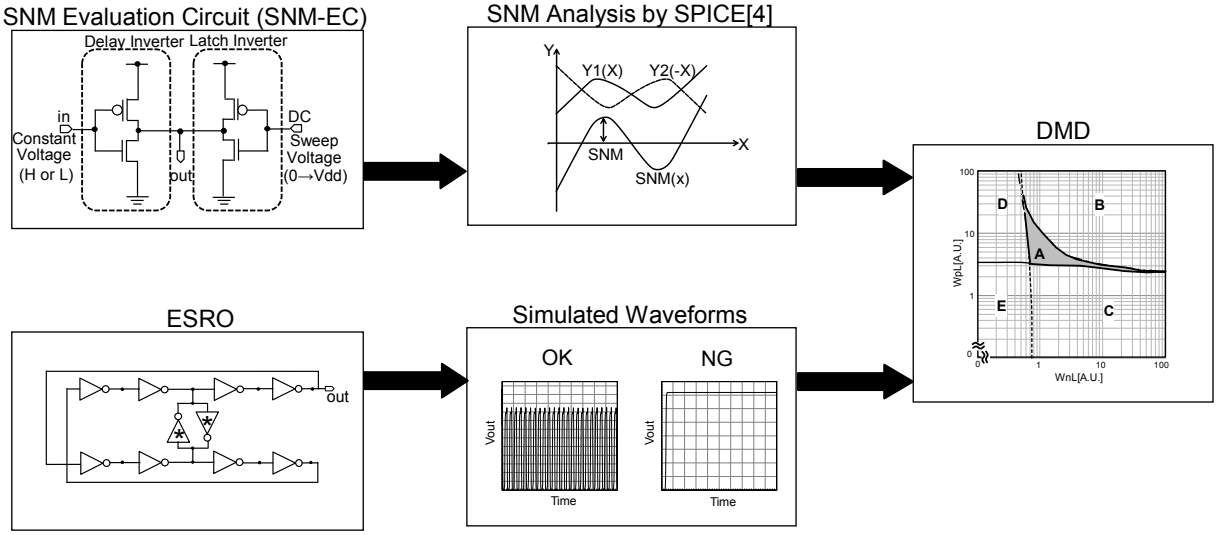
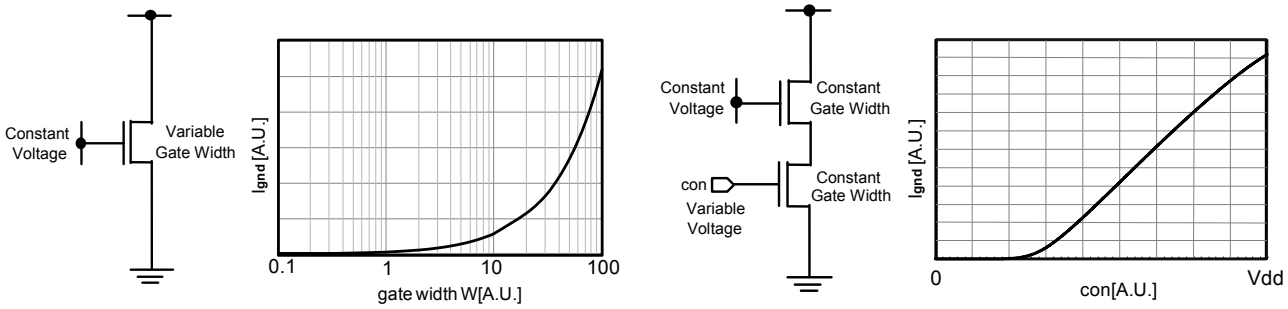


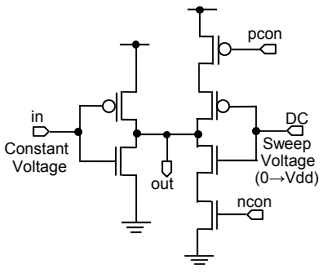
Fig.3: DMD Generation Flow by Simulation

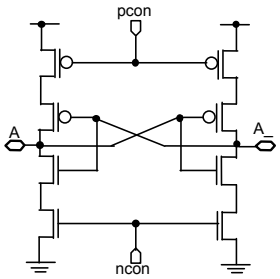


(a)MOSFET

(b)Equivalent Variable W Transistor (EVWT)

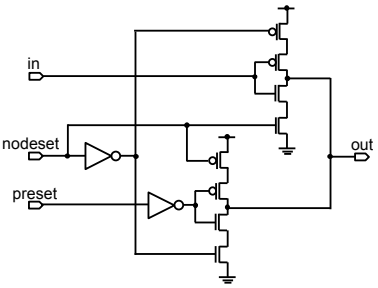
Fig.4 : Current Characteristic

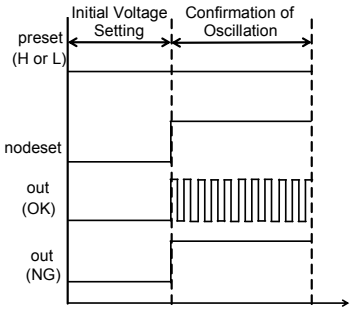




(a)EVW-SNM TEG (b)EVW- Latch (EVWL)

Fig.5: Circuit Design for Measurement





(a)Initial-voltage Preset-able Inverter (IPI) (b)Timing Chart

Fig.6: Developed ESRO for Measurement

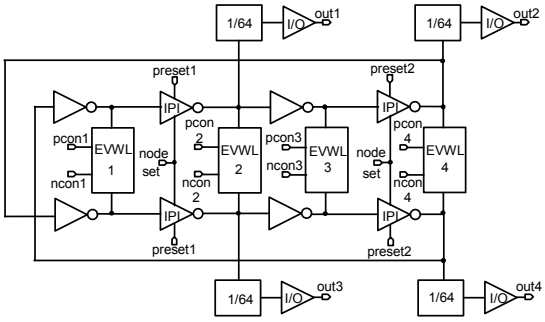


Fig.7: Universal ESRO TEG (U-ESRO TEG)

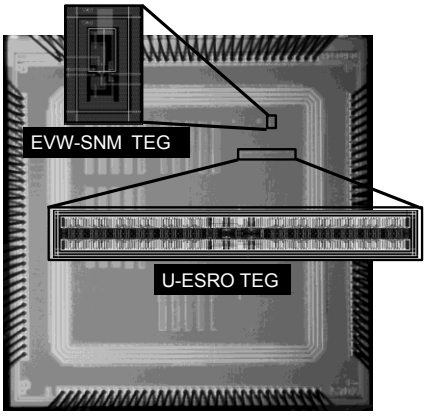


Fig.8: Chip Photograph

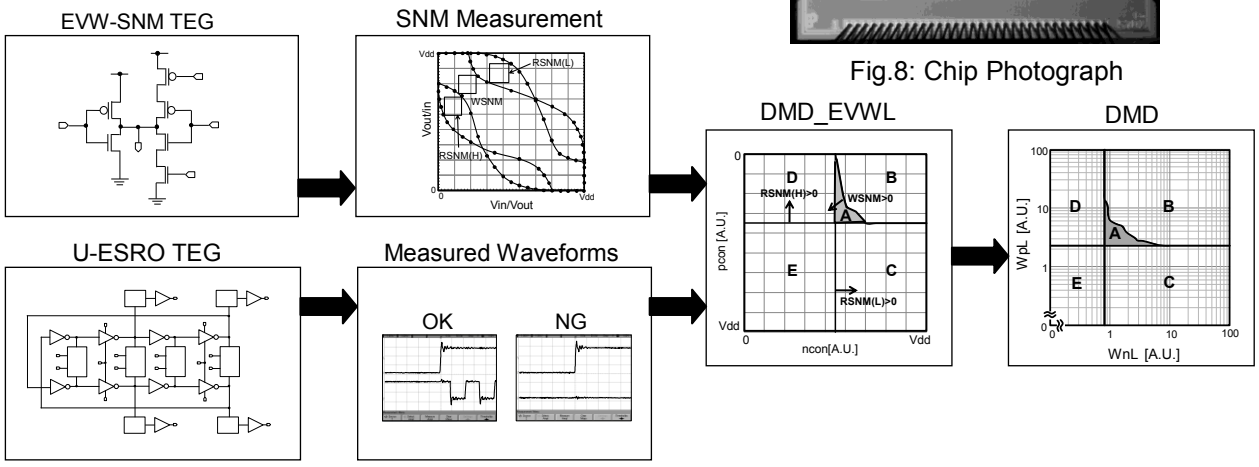
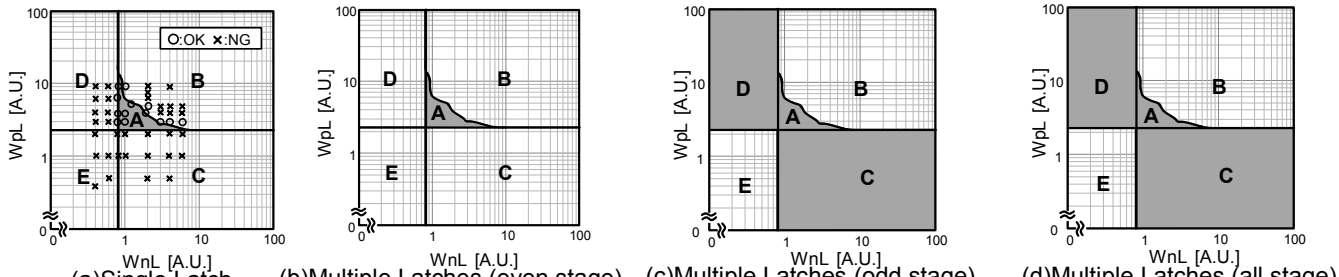


Fig.9: Developed DMD Generation Flow of ESRO by Measurement



(a)Single Latch (b)Multiple Latches (even stage) (c)Multiple Latches (odd stage) (d)Multiple Latches (all stage)

Fig.10: Measured Results of U-ESRO TEG