Mosaic SRAM Cell TEGs with Intentionally-added Device Variability for Confirming the Ratio-less SRAM Operation

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***Abstract*—MOSAIC SRAM Cell TEGs consisting of memory cells having all combinations of gate sizes of transistors differing by two orders of magnitude were developed with 0.18um CMOS process to verify the operation margins for SRAM circuits. The measured results show the operation of the ratio-less SRAM is completely independent of the size of transistors in the memory cell.**

Keywords—*SRAM; Variability; Ratio-less; Static Noise Margin;*

1. Introduction

In the development of SRAMs for the state-of-the-art technology generation, it is difficult to maintain a sufficient operation margin in the SRAM, because of supply voltage scaling and device variability [1]. Figure 1(a) shows a conventional 6-transistor CMOS SRAM cell which has been widely used in the past and up to the present as the basic SRAM memory cell circuit. In this circuit, the write (flip/flop inversion) operation is performed from the outside through the impedance of the transfer transistors (SN1, SN2), while the read operation must be performed by outputting the stored information to the bit-lines through the same transfer transistors without destroying the information in the flip/flop. In the design of the transfer gate transistors, therefore, there exist the upper and lower limit values that are permissible from considerations of impedances, and the ratio design is thus required for stable operation. As a method of quantitatively evaluating this design margin in SRAM cells, there are the Read and Write Static Noise Margin (RSNM and WSNM) indexes as shown in Fig. 1(b) [2]. In recent years, with drastically decreasing the device dimensions, it is becoming difficult to secure these SNMs simultaneously, because they suffer direct effects of the lowering of the power supply voltage and the increase in process variation among devices [3].

To overcome this problem, a circuit named 8T-SRAM has been proposed (Fig. 2(a)) [4]. In this circuit, the RSNM restriction can be avoided since it has a dedicated read buffer, however, the WSNM restriction still exists. In order to avoid both RSNM and WSNM restriction simultaneously, we had proposed the Ratio-less 10T-SRAM [5]. The operation of the Ratio-less SRAM is completely independent of the size for transistors in the memory cell. In order to confirm the Ratio-less operation, we developed the MOSAIC SRAM Cell TEGs.

2. Structure of MOSAIC SRAM Cell TEG

We developed MOSAIC SRAM Cell TEGs using 0.18μm CMOS in which the gate width (W) value of each set of transistors in a memory cell was varied by a range of two orders of magnitude. The device matrix array (DMA) TEGs to evaluate the device variability of MOSFETs or SNMs in SRAM cells were developed in the past [6]. However, a SRAM cell TEG with intentionally-added device variability to confirm the wide operation margin has not been developed. Figure 3 shows the design example of MOSAIC SRAM cell array for conventional 6-transistor SRAM. Our MOSAIC SRAM TEG includes the complete set of size combinations (the number of different designs are two to the sixth power, or 64) for 1-bit memory cells. The cell array consists of 64 memory cells in which the gate widths are designed with the design allocation table in Fig. 3(a). The size of each transistor composing a memory cell is designed to be either 0.3μm or 30μm. The cell design examples are shown in Fig. 3(b)-(d). Cell_0 in Fig. 3(b) is the case in which all transistors have the minimum size of 0.3μm, Cell_63 in Fig. 3(c) is the case in which all transistors have the maximum size of 30μm, and Cell_28 in Fig. 3(d) is an example of a mix of 0.3 and 30μm transistors.

3. Layout Method for MOSAIC SRAM Cell Array

Figure 4 shows the layout method we developed to form the MOSAIC cell array. In order to reduce the layout complexity, a memory cell is divided into the left and right half cells as shown in Fig.4 (a). In the case of 6T SRAM, each half cell consists of 3 transistors. Therefore, we first laid out 16 half cells (L1-8, R1-8) as shown in Fig.4 (b). The area occupied when all transistors have the maximum (30μm) is ensured as the size of footprint for all half cells. Then we develop the array reference of half cells to obtain the MOSAIC array as shown in Fig.4 (c). This method can reduce the layout cost to the order of square root of memory size.

4. Developed MOSAIC SRM Cell TEGs

We developed 3 MOSAIC SRAM TEGs. Figure 5 (a) shows the 64-bit MOSAIC SRAM TEG which includes conventional 6 transistor SRAM cells. Figure 5(b) Shows 256-bit MOSAIC SRAM TEG which includes 8T SRAM cells. Figure 6 (a) shows 1024-bit MOSAIC SRAM TEG which includes 1024 ratio-less 10T cells. The cell layout examples in 1024-bit ratio-less MOSAIC SRAM TEG are shown in Fig. 6(b)-(d). Cell_0 in Fig. 6(b) is the case in which all transistors have the minimum size of 0.3μm, Cell_1023 in Fig. 6(d) is the case in which all transistors have the maximum size of 30μm, and Cell_374 in Fig. 6(c) is an example of a mix of 0.3 and 30μm transistors.

5. Experimental Results

Figure 7(a)-(e) are measured fail bit maps (FBMs) obtained by applying marching pattern tests to our MOSAIC SRAM TEGs. In the MOSAIC SRAM design, the position of memory cell corresponds to the combination of transistor sizes as indicated to the right and bottom of the FBMs. Figures 7(a), and (b) respectively show the results obtained in measurements of the MOSAIC SRAM TEGs with 6T SRAM cells and 8T SRAM cells. The hatched parts in the figures are failed cells. These results show that there are many failed cells in spite of the low-operating frequency of 1MHz. Since these circuits require ratio design, many combinations are inoperative. Figure 7(c) shows the result obtained in measurement with 8T MOSAIC SRAM TEG with the write after read technique [4]. Because this operation can relax the operation margin in write-half-select cells, failed cells are slightly decreased when compared with the result shown in Fig. 7(b). In contrast, only a few cells are failed in our ratio-less SRAM with the high-operating frequency of 15MHz as shown in Fig. 7(d). The operation of whole cells in our ratio-less SRAM is experimentally confirmed at an operating frequency less than 10MHz as shown in Fig. 7(e). The result of MOSAIC SRAM with our ratio-less SRAM cell shows that operation of the SRAM is independent of the size of transistors in the memory cell.

6. Conclusions

This paper proposed a new SRAM TEG to confirm the ratio-less SRAM operation. The MOSAIC SRAM Cell TEGs consisting of memory cells having all combinations of gate sizes of transistors differing by two orders of magnitude were developed with 0.18um CMOS process. The measured result of MOSAIC SRAM Cell TEGs with the ratio-less SRAM cell shows that operation of the SRAM is independent of the size of transistors in the memory cell.

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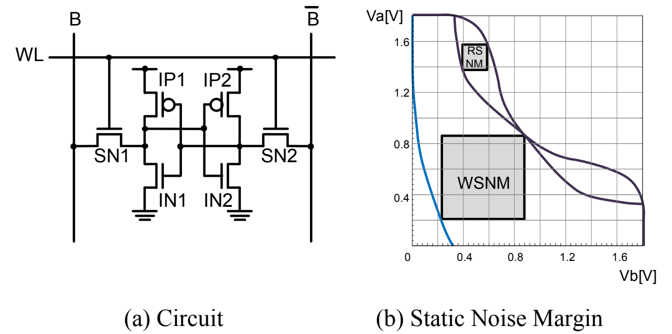
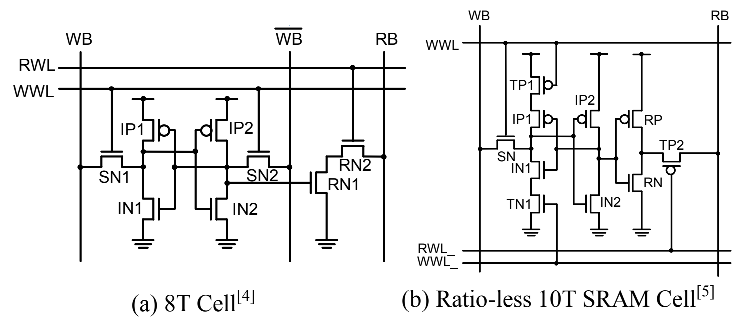


(a) Circuit (b) Static Noise Margin

Fig. 1 Conventional 6 Transistor SRAM Cell

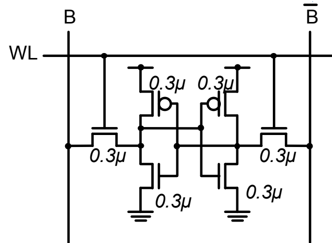


(a) 8T Cell[4] (b) Ratio-less 10T SRAM Cell[5]

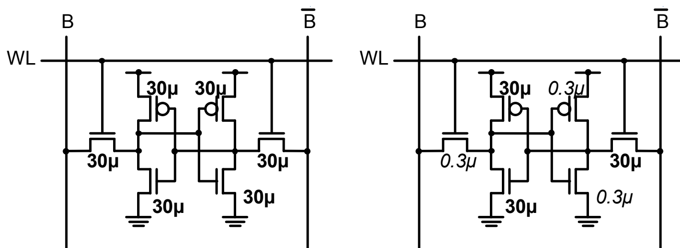
Fig.2 Improved SRAM Cells

WSN1	WIP1	WIN1								
0.3μ	0.3μ	0.3μ	0	1	2	3	4	5	6	7
		30μ	8	9	10	11	12	13	14	15
	30μ	0.3μ	16	17	18	19	20	21	22	23
		30μ	24	25	26	27	28	29	30	31
30μ	0.3μ	0.3μ	32	33	34	35	36	37	38	39
		30μ	40	41	42	43	44	45	46	47
	30μ	0.3μ	48	49	50	51	52	53	54	55
		30μ	56	57	58	59	60	61	62	63
		WIN2	0.3μ	30μ	0.3μ	30μ	0.3μ	30μ	0.3μ	30μ
		WIP2	0.3μ		30μ		0.3μ		30μ	
		WSN2	0.3μ				30μ			

(a) Design Allocation Array

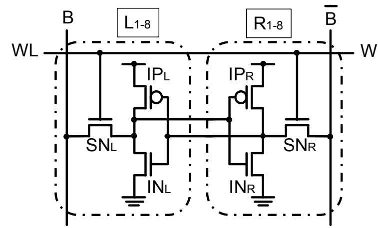


(b) Cell_0



(c) Cell_63 (d) Cell_28

Fig.3 Design of MOSAIC SRAM Cell Array



(a) Left and Right Half Cells

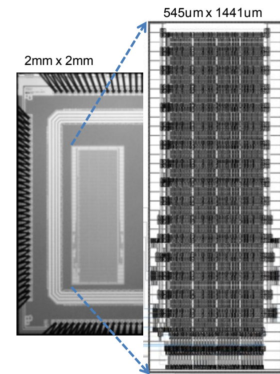
SN(L/R)	IP(L/R)	IN(L/R)	Left-Half	Right-Half
0.3μ	0.3μ	0.3μ	*L1*	*R1*
		30μ	*L2*	*R2*
	30μ	0.3μ	*L3*	*R3*
		30μ	*L4*	*R4*
30μ	0.3μ	0.3μ	*L5*	*R5*
		30μ	*L6*	*R6*
	30μ	0.3μ	*L7*	*R7*
		30μ	*L8*	*R8*

(b) Gate Widths for Half Cells

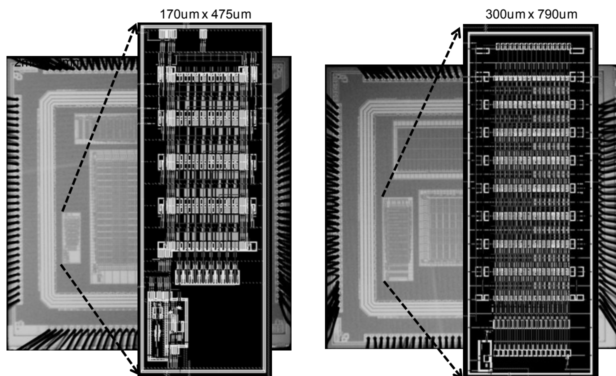
	1		2		3		4		5		6		7		8	
1	*L1*	*R1*	→	*R2*	→	*R3*	→	*R4*	→	*R5*	→	*R6*	→	*R7*	*L1*	*R8*
2	*L2*	↓	→	↓	→	↓	→	↓	→	↓	→	↓	→	↓	*L2*	↓
3	*L3*	↓	→	↓	→	↓	→	↓	→	↓	→	↓	→	↓	*L3*	↓
4	*L4*	↓	→	↓	→	↓	→	↓	→	↓	→	↓	→	↓	*L4*	↓
5	*L5*	↓	→	↓	→	↓	→	↓	→	↓	→	↓	→	↓	*L5*	↓
6	*L6*	↓	→	↓	→	↓	→	↓	→	↓	→	↓	→	↓	*L6*	↓
7	*L7*	↓	→	↓	→	↓	→	↓	→	↓	→	↓	→	↓	*L7*	↓
8	*L8*	*R1*	→	*R2*	→	*R3*	→	*R4*	→	*R5*	→	*R6*	→	*R7*	*L8*	*R8*

(c) Array Layout of Half Cells

Fig.4 Layout Method of MOSAIC Cell Array

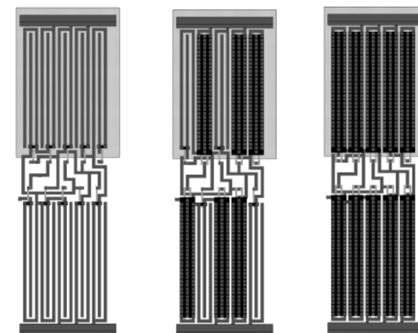


(a) 1024b 10T Ratio-less SRAM



(a) 64b 6T SRAM (b) 256b 8T SRAM

Fig.5 Chip Photograph of MOSAIC 6T/8T SRAMs



(b) Cell_0 (c) Cell_374 (d) Cell_1023

Fig.6 Chip Photograph of 10T Ratio-less MOSAIC SRAM

(a) 6T SRAM (1MHz, 1.8V)

(b) 8T SRAM (1MHz, 1.8V)

(c) 8T SRAM’ (1MHz, 1.8V)

(d) 10T Ratio-less SRAM (15MHz, 1.8V)

(e) 10T Ratio-less SRAM (10MHz, 1.8V)

Fig.7 Measurement Results of MOSAIC TEGs