# $V_{\text {th-shiftable SRAM Cell TEGs for Direct Measurement for the Immunity }}$ of the Threshold Voltage Variability 

Shogo Yamaguchi Hitoshi Imi Shogo Tokumaru Kazuyuki Nakamura

## Kyusyu Institute of Technology

680-4 Kawazu, Iizuka, Fukuoka 820-8502, Japan
Phone: +81-948-29-7584 Fax: +81-948-29-7586 Email: shogo_yamaguchi@cms.kyutech.ac.jp

## 1. Introduction

For SRAM using state-of-the-art processes of deep sub-micron generation, it is becoming difficult to secure operating margins due to the lowering of power supply voltage and the increase in the device characteristic variation [1][2]. To overcome this problem, we proposed the ratio-less SRAM (RL-SRAM) design [3][4]. In order to demonstrate the immunity of the ratio-less SRAM operation for the device characteristic variability by the measurement, we also developed MOSAIC SRAM cell TEGs with intentionally-added device variability within the gate width [5]. However, the immunity for the device variability in the threshold voltage $\left(\mathrm{V}_{\mathrm{th}}\right)$ of MOSFETs has not been evaluated by the measurement. Therefore, we newly developed the $\mathrm{V}_{\mathrm{th}}$-shiftable SRAM cell TEGs (VTSTs).

## 2. Design of $\mathrm{V}_{\text {th }}$ shiftable SRAM Cell TEG

Figure 1 shows a simple model for $\mathrm{V}_{\text {th }}$-shifts in the MOSFETs in a 6 transistor SRAM (6T-SRAM) Cell. Each MOSFET may have the inherent $\mathrm{V}_{\mathrm{th}}$-shift caused by the device characteristic variabilities. Figure 2 shows the developed VTST for 6T-SRAM. In this structure, the all gate terminals of MOSFETs are extracted to the chip boundary and tapped to analog I/O (AIO) buffers. Six external voltage sources (EVSs) are employed to apply the $\mathrm{V}_{\mathrm{th}}$-shift to each MOSFET. The arbitral $\mathrm{V}_{\mathrm{th}}$-shift value and its polarity can be manipulated by the EVS. Figure 3 shows the photo and layout of our developed VTST for 6T-SRAM using the $0.18 \mu \mathrm{~m}$ CMOS process.

## 3. Measured Results and Discussions

In the evaluation of measured results of the VTST, we defined fail condition map (FCM) which summarizes all the combinations of the polarity setting for a $\mathrm{V}_{\text {th }}$-shift. Since the $\mathrm{V}_{\mathrm{th}}$-shift for each MOSFET can be set to $\left(+\Delta \mathrm{V}_{\mathrm{th}}\right.$ or $\left.-\Delta \mathrm{V}_{\mathrm{th}}\right)$, the total number of combinations for the measurement is 64 $\left(=2^{6}\right)$ for the 6T-SRAM cell. Figure 4 shows the FCM for the voltage shift values of $\pm 0.15 \mathrm{~V}$ for 6 T -SRAM. The one cell in FCM indicates one combination of the polarities $\left(+\Delta V_{\text {th }}\right.$ or $\left.-\Delta \mathrm{V}_{\text {th }}\right)$ of six transistors of which an SRAM cell is composed. For example, in the left and the upper corner cell in FCM in Fig.4, the $\mathrm{V}_{\mathrm{th}}$-shifts for all six MOSFETs are set to -0.15 V . In the FCM , white colored cells and gray colored cells mean the combination of $\mathrm{V}_{\text {th }}$-shifts is operable (Pass) as SRAM cell or not operable (Fail), respectively. In the Fig. 4, we can recognize the 6 combinations of the polarities of $\mathrm{V}_{\mathrm{th}}$-shift of $\pm 0.15 \mathrm{~V}$ are not operable. Figures 5 and 6 show the measured FCMs for the $\mathrm{V}_{\mathrm{th}}$-shift values of 0.25 V and 0.3 V , respectively.

Figure 7 summarizes the total counts of the fail conditions of FCMs versus the $\mathrm{V}_{\mathrm{th}}$-shifts $\left(\left|\Delta \mathrm{V}_{\mathrm{th}}\right|\right)$ and the supply
voltages $\left(\mathrm{V}_{\mathrm{dd}}\right)$. This figure means the maximum limit of $\left|\Delta \mathrm{V}_{\text {th }}\right|$ for 6T-SRAM operation is 0.1 V or less. Here we defined the Critical $\mathrm{V}_{\text {th }}\left(\mathrm{C} \Delta \mathrm{V}_{\text {th }}\right)$ as the maximum limit of $\mathrm{V}_{\text {th }}$ - shift for stable SRAM operation. Figure 8 shows the detail of relationship between the $\mathrm{C} \Delta \mathrm{V}_{\text {th }}$ and the supply voltage. From the results of FCMs in Figs. 4-6, the $\mathrm{V}_{\mathrm{th}}$-shifts of N3 and N4 tend to decide the $\mathrm{C} \Delta \mathrm{V}_{\mathrm{th}}$. This is because the higher $\mathrm{V}_{\mathrm{th}}$-shifts of N 3 and N 4 prevents the write operation.

## 4. Conclusion

We developed VTST for 6T-SRAM and evaluated the influences of SRAM operation by threshold voltage fluctuation using measured FCMs and $\mathrm{C} \Delta \mathrm{V}_{\text {th }} \mathrm{s}$. The VTST for the ratio-less 12 transistor SRAM (RL-12T-SRAM) was also developed as shown in Fig.12, however the number of combinations of $4096\left(=2^{12}\right)$ for an FCM is too huge to finish the measurement by manual operation. Therefore now we are trying to construct the automated measurement environment for the RL-12T-SRAM VTST. Figure 10 includes the simulated $\mathrm{C} \Delta \mathrm{V}_{\text {th }}$ for RL-12T-SRAM, however we will obtain the similar measurement results for RL-12T-SRAM soon.

## ACKNOWLEDGMENTS

This work was supported by VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Cadence Design Systems, Inc., Mentor Graphics, Inc., the Rohm Corporation and the Toppan Printing Corporation. This research was also supported by funds from the Japanese Ministry of Education, Culture, Sports, Science and Technology, MEXT.

## REFERENCES

[1] E. Seevinck, F. J. List, J. Lohstroh, "Static-noise margin analysis of MOS SRAMcells", IEEE J. Solid-State Circuits, vol. SC-22, no. 5, October 1987.
[2] L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond"
[3] T. Saito, H. Okamura, H. Yamamoto and K. Nakamura, "Ratio-less 10Transistor Cell and Static Column Retention Loop Structure for Fully Digital SRAM Design", IEEE International Memory Workshop, vol. 2012, May 2012.
[4] T. Kondo, H. Yamamoto, H. Imi, H. Okamura and K. Nakamura, "A Measurement of Ratio-less 12-transistor SRAM cell Operation at Ultralow Supply-voltage", Solid State Devices and Materials, September 2014 [5] H. Okamura, T. Saito, H. Goto, M. Yamamoto and K. Nakamura, "Mosaic SRAM Cell TEGs with Intentionally-addred Device Variability for Confirming the Ratio-less SRAM Operation", IEEE International Conference on Microelectronic Test Structures, March 2013.


Figure 1: Model of $\mathbf{V}_{\mathrm{th}}$-Shifts in 6T-SRAM Cell


Figure 2: Structure of $\mathbf{V}_{\text {th }}$-shiftable SRAM Cell TEG (VTST)


Figure 3: Photo and Layout of VTST for 6T-SRAM


Figure 4: Fail Condition Map (FCM) for $\Delta V_{\mathrm{th}}= \pm 0.15 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{dd}}=1.8 \mathrm{~V}$


Figure 5: FCM for $\Delta V_{\text {th }}= \pm 0.25 \mathrm{~V}$
and $V_{d d}=1.8 \mathrm{~V}$


Figure 6: FCM for $\Delta V_{t h}= \pm 0.3 \mathrm{~V}$ and $V_{d d}=1.8 V$


Figure 7: Number of Fail Conditions versus $\Delta V_{\text {th }}$ and $V_{d d}$


Figure 8: Measured Critical- $\Delta \mathbf{V}_{\text {th }}$ versus $\mathbf{V}_{\text {dd }}$


Figure 9: Model of V $_{\mathrm{th}}$-Shifts RL-12T-SRAM Cell


Figure 10: Comparison of $\mathrm{CV}_{\text {th }}$ for 6T-SRAM and RL-12T-SRAM

