On Pinpoint Capture Power Management in At-Speed Scan Test Generation

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Abstract

*This paper proposes a novel scheme to manage capture power in a pinpoint manner for achieving **guaranteed capture power safety**, **improved small-delay test capability**, and **minimal test cost impact** in at-speed scan test generation. First, switching activity around each long path sensitized by a test vector is checked to characterize it as **hot** (with excessively-high switching activity), **warm** (with normal/functional switching activity), or **cold** (with excessively-low switching activity). Then, X-restoration/X-filling-based **rescue** is conducted on the test vector to reduce switching activity around hot paths. If the rescue is insufficient to turn a hot path into a warm path, **mask** is then conducted on expected test response data to instruct the tester to ignore the potentially-false test response value from the hot path, thus achieving guaranteed capture power safety. Finally, X-restoration/X-filling-based **warm-up** is conducted on the test vector to increase switching activity around cold paths for improving their small-delay test capability. This novel approach of **pinpoint** capture power management has significant advantages over the conventional approach of **global** capture power management, as demonstrated by evaluation results on large ITC'99 benchmark circuits and detailed path delay analysis.*

1. Introduction

Delay testing is indispensable for achieving high product quality for *deep-submicron* (*DSM*) circuits that are susceptible to timing-related physical defects. Delay test vectors can be generated by using the transition delay or path delay fault model or both [1]. There are two issues that are of special importance to delay test vectors.

The first issue with a delay test set is ***test quality***, which is determined by its capability to expose the existence of delay defects of various sizes. It has been shown that small-delay defects are becoming dominant in DSM chips [2]; thus, the capability of detecting small-delay defects should be improved in order to achieve high timing-related test quality. For this purpose, special care can be taken to sensitize long paths for fault detection in transition delay test generation [3], and/or long paths can be explicitly selected and targeted in path delay test generation [1].

The second issue with a delay test set is ***test power***. This is especially true when delay testing is conducted through at-speed scan testing with the ***launch-on-capture*** (***LOC***) clocking scheme as illustrated in Fig. 1. At-speed scan test power includes *shift power* and *capture power* [4].

Shift power is caused by shift switching activity in the whole circuit due to the consecutive application of shift clock pulses. Its impact is therefore accumulative, which

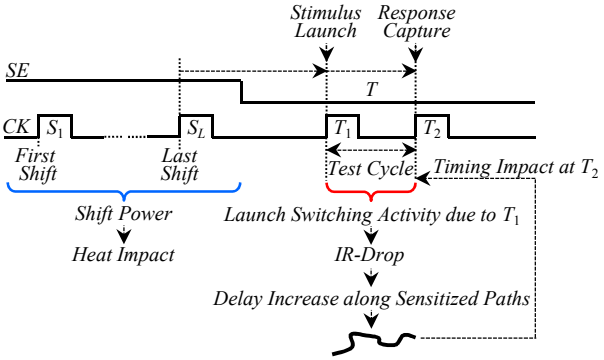


Fig. 1. Test power in LOC-based at-speed scan testing.

mostly manifests itself as excessive heat. Effective techniques [4, 5] are available for effectively reducing shift power through manipulating shift clocking, circuit design, test vector generation, etc.

Capture power is caused by the ***launch switching activity*** (***LSA***) triggered by the stimulus launch clock pulse T_1. This leads to IR-drop in the *power distribution network* (*PDN*), resulting in delay increase on sensitized paths [5]. This IR-drop-induced extra delay can have *negative impact* and *positive impact* on the timing of sensitized paths.

- ***Negative Impact***: When the IR-drop-induced delay increase is larger than the allowable slack of a sensitized path, a false timing failure will occur at T_2 at the endpoint of the sensitized path even when the circuit is fault-free. This results in over-test and thus undue yield loss, which has become a severe challenge in the industry [6-8].
- ***Positive Impact***: When the IR-drop-induced delay increase is less than the allowable slack of a sensitized path, delay defects of smaller sizes on the path will become more likely to be detected because of the extra delay along the path. This results in enhanced test quality in terms of better small-delay test capability [9].

Conventionally, ***global capture power management*** has been widely used in practice, which is for adjusting the whole-circuit capture power that is quantified by a single metric, such as *weighted switching activity* (*WSA*) [10]. Previous techniques based on this approach mitigate the negative impact of capture power by reducing LSA at T_1 (Fig. 1) [4, 5]. However, the reduction effect is often questionable with respect to capture power safety [12], and its impact on test costs is high [13]. Furthermore, the positive impact of capture power has been largely ignored since the global approach is not suitable for adjusting the delay of a particular path. These problems all call for a new approach to capture power management.

1.1 Problems of Global Capture Power Management

The conventional approach of global capture power management tries to control the whole-circuit capture power by adjusting the number of simultaneously-capturing scan *flip-flops* (*FFs*) at T_1 (Fig. 1). This can be achieved by ***circuit / clock modification*** or ***test data manipulation*** [4, 5]. However, circuit / clock modification, when applied in capture mode, tends to entail significant changes to *automatic test pattern generation* (*ATPG*) algorithms, fault coverage loss, as well as test data inflation. Therefore, test data manipulation is generally considered preferable for capture power management [11-17].

The capture power of a test vector can be manipulated during test generation (*in-ATPG*) or after test generation (*post-ATPG*). The former can be realized by disabling clock gators to reduce the number of simultaneously-capturing scan FFs by *low-capture-power ATPG* [18,19]. The latter can be realized by first conducting *test relaxation* [20] to turn fully-specified test vectors into partially-specified test cubes and then applying *low-capture-power X-filling* [11, 12, 14-16] to equalize FF input/output values as much as possible to reduce capture transitions at FFs.

Although many techniques for global capture power management (mostly reduction) have been proposed, they generally suffer from the following serious problems:

- **Problem 1** (***Unfocused Capture Power Reduction***): Most of the previous techniques only reduce capture power in a global or unfocused manner. This is a severe problem since capture power is not evenly distributed across the whole chip. Global or unfocused reduction may end up with reducing the capture power in an area already with low capture power but leaving the capture power in an area with excessively-high capture power intact. As a result, the negative impact of capture power cannot be effectively mitigated by global capture power reduction.
- **Problem 2** (***No Guarantee of Capture Power Safety***): Although previous techniques can reduce capture power to some extent, most of them cannot guarantee that they can always sufficiently reduce capture power below a safe limit [8, 12]. This is a major problem since ***capture power safety***, rather than ***capture power reduction***, is the ultimate goal in mitigating the negative impact of capture power.
- **Problem 3** (***Test Vector Count Inflation***): The global/ unfocused approach often results in unnecessary reduction for test vectors or chip regions that need no capture power reduction. This is the cause of severe low-power-test-generation-induced inflation in test vector count [12,13].
- **Problem 4** (***Compromised Test Quality***): Most of the previous techniques only try to mitigate the negative impact of capture power by unconditionally reducing capture power. They ignore the positive impact of capture power, thus missing the chances of improving small-delay test capability. In addition, global capture power reduction also tends to over-reduce the capture power in some regions, which also leads to compromised test quality.

All the aforementioned problems are essentially caused by the obvious fact that, conducting capture power management in a ***global manner*** is fundamentally against the ***local nature*** of capture power.

1.2 Needs for Pinpoint Capture Power Management

Fig. 2 illustrates why the impact of capture power is ***local*** in nature and largely depends on the sensitization status and lengths of paths, as the motivation of this work.

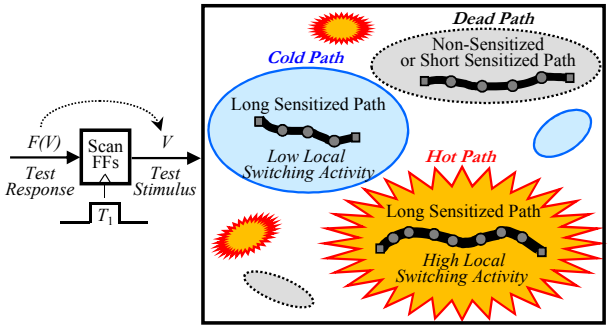


Fig. 2. Motivation for pinpoint capture power management.

Fig. 2 shows three possible scenarios when the test stimulus is launched at T_1 (Fig. 1), based on whether and what type of capture power impact will occur to a path due to IR-drop-induced delay increase. First, if a path is not sensitized or sensitized but very short, then no matter how much switching activity occurs around it, neither the negative impact nor a significant level of the positive impact of capture power will occur to the path. Such a path is a ***dead path***, and there is no need to manage (reduce or increase) its neighboring switching activity. Second, if a long path is sensitized and its neighboring switching activity is excessively high, there is a risk that IR-drop-induced delay increase along the path may cause a false timing failure at the endpoint of the path. Such a path is a ***hot path***, and clearly it is imperative to eliminate all hot paths for a test vector so as to guarantee capture power safety [12]. Third, if a long path is sensitized but its neighboring switching activity is considerably low (i.e., significantly below the functional level), there is a possibility to benefit from the positive impact of capture power. Such a path is a ***cold path***, which can be warmed-up by properly increasing its neighboring switching activity so as to improve its small-delay test capability [9].

Fig. 2 clearly demonstrates the needs for ***pinpoint capture power management***, whose ***focused nature*** completely matches the ***local nature*** of capture power. Based on this new approach, the goal of this work is to establish a novel and practical at-speed scan test generation scheme with the following unique advantages:

(1) *Guaranteed Capture Power Safety*
(2) *Improved Small-Delay Test Capability*
(3) *Minimal Test Cost Impact*

1.3 Paper Organization

The rest of the paper is organized as follows: Sect. 2 describes the background, followed by Sect. 3 that presents the basic idea of this work. Sect. 4 first shows the proposed test generation scheme based on pinpoint capture power management and then provides the details of major techniques developed for the scheme. Sect. 5 describes evaluation results, and Sect. 6 concludes the paper.

2. Background

This section first reviews sensitized-path-based capture power analysis, which is indispensable for pinpoint capture power management. A brief review then follows about previous work related to guaranteeing capture power safety and improving small-delay test capability, which helps highlight the novelty of this work.

2.1 Sensitized-Path-Based Capture Power Analysis

The impact of capture power for a test vector mostly manifests itself as delay increase along paths sensitized by the test vector [5, 9, 12]. However, it is prohibitively costly to obtain the accurate IR-drop-induced delay increase of a sensitized path in test generation since it requires timing-accurate logic simulation, IR-drop analysis, and delay calculation. A realistic alternative for test generation is to measure logical switching activity in the neighbourhood of a path by normal logic simulation [4, 5]. The neighbourhood, also referred to as *impact area*, is defined below [12]:

Definition 1: The ***aggressor region*** of a gate G, denoted by $AR(G)$, is composed of aggressor nodes (gates and FFs) whose transitions strongly impact the supply voltage of G.

Definition 2: The ***impact area*** of a path P, denoted by $IA(P)$, consists of the aggressor regions of all of its on-path gates (G_1, G_2, ..., G_n). That is, $IA(P) = \sum_{i=1}^{n} AR(G_i)$.

Fig. 3 illustrates the impact area of a path P. Note that the aggressor region of a gate G can be readily obtained by finding nodes that share the power vias from which G draws most of its current [5, 9]. Such power vias and their related or influenced nodes can be directly identified by using circuit/PDN layout data.

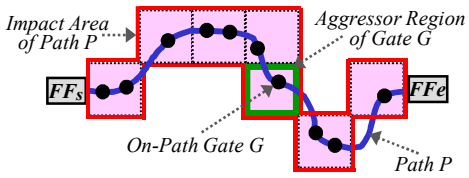


Fig. 3. Impact area of a path.

Once the impact area of a long sensitized path is obtained, the switching activity level in this area can be estimated with a metric based on the results of logic simulation. For example, the WSA metric [10], calculated as a weighted toggle count for all nodes in the impact area, can be used for this purpose. One can also use more sophisticated metrics [4, 5], which can provide a more accurate estimation of IR-drop-induced delay increase but usually at a higher computational cost.

This work uses sensitized-path-based capture power analysis in pinpoint capture power management for guiding its decisions and assessing its effect. The details will be presented in Subsection 3.1.

2.2 Related Work

Some representative previous techniques related to pinpoint capture power management are reviewed below.

2.2.1 Guaranteeing Capture Power Safety

There is no doubt that capture power safety is more important than capture power reduction. Capture power reduction techniques with capture safety checking [8,15] or based on pseudo-functional testing [21] are helpful for this purpose. Recently, we proposed a ***rescue-and-mask*** based test generation scheme [11, 12] for explicitly guaranteeing capture power safety with minimal test data inflation, through the following four steps:

- **Step-1** (***Initial Test Vector Generation***): Conventional test generation is conducted to deterministically generate a test cube C_1 for detecting targeted faults and randomly-fill C_1 into a test vector V_1 for fortuitous detection. Randomly-filled bits in V_1 are called ***X-filled logic bits***. No capture power reduction is considered in this step.
- **Step-2** (***Capture Safety Checking***): Sensitized-path-based capture power analysis is conducted on V_1. If there is at least one ***risky path*** (i.e., a long sensitized path with excessively-high switching activity in its impact area), go to Step-3; otherwise, V_1 is capture-power-safe and final.
- **Step-3** (***Rescue***): The ***rescue*** operation is conducted by first restoring into X-bits those X-filled logic bits in V_1 that can reach the impact areas of risky paths, resulting in a new test cube C_2. Then, low-capture-power X-filling [4, 11] is conducted on C_2 to reduce switching activity in the impact areas of the risky paths, resulting in a modified test vector V_2. If all risky paths become safe, V_2 is capture-power-safe and final; otherwise, go to Step-4.
- **Step-4** (***Mask***): The ***mask*** operation is conducted on V_2 by assigning a special symbol (X for most testers) to the expected test response bit corresponding to the output of each remaining risky path. X instructs the tester not to compare test responses at this output bit so as to avoid the impact of the risky path, thus guaranteeing capture power safety. Note that the masking is only effective for the current test vector. That is, the masked output bit is available for fault detection for other test vectors. In addition, fault coverage loss due to the masking of the current test vector can be fully recovered by other test vectors generated in subsequent ATPG runs.

Although the above rescue-and-mask scheme [12] can achieve guaranteed capture power safety with minimal test vector count inflation (less than 0.1% for large ITC'99 benchmark circuits as reported in [12]), it only tries to mitigate the negative impact of capture power by reducing switching activity and ignores the positive impact of capture power. In addition, it runs the risk of over-reducing the switching activity in the impact area of a risky path, resulting in compromised small-delay test capability. These problems will be addressed in this paper.

2.2.2 Improving Small-Delay Test Capability

Previous techniques exist for maximizing IR-drop on critical paths by increasing switching activity around on-path nodes [9]. Although being intended for estimating worst-case delay for critical paths, they demonstrate the possibility of making use of the positive impact of capture power for improving small-delay test capability in at-speed scan testing. This possibility will be fully exploited by the new test generation scheme in this work.

3. Basic Idea

This section presents the basic idea of this work. First, it shows how to classify paths sensitized by a test vector. Then, based on the results of path classification, a strategy for pinpoint capture power management is established.

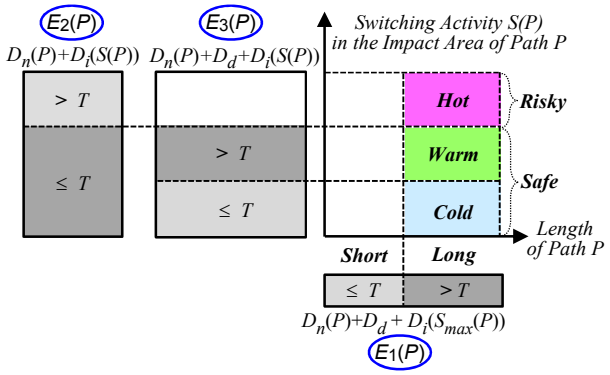
3.1 Path Classification

Because the impact of capture power manifests itself as timing failures due to IR-drop-induced delay increase, it can only show up at the endpoints of sensitized paths. Especially, the length of a sensitized path and the switching activity in its impact area determine the characteristic of the path with respect to the impact of capture power. Such characteristics can be revealed through ***path classification***. Table 1 lists the definitions of variables needed for this purpose.

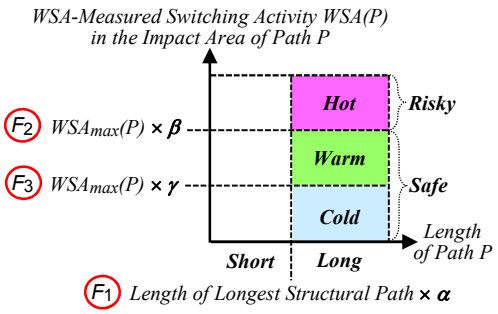
Table 1. Variable Definitions

$E_k(P)$	Total delay of path P for criterion k (k = 1, 2, 3)
$D_n(P)$	Nominal delay of path P
$S(P)$	Switching activity in the impact area of path P
$S_{max}(P)$	Maximum amount of $S(P)$
$D_i(S(P))$	Delay increase on path P due to $S(P)$
D_d	Typical defect delay
T	Test cycle (as shown in Fig. 1)

The theoretical criteria for path classification are shown in Fig. 4(a). First, $E_1(P)$ is used to determine if a sensitized path P is ***long*** or ***short***. For a long path P, $E_2(P)$ and $E_3(P)$ are further used to determine if P is ***hot***, ***warm***, or ***cold***.



(*a*) *Theoretical criteria*



(*b*) *Practical criteria*

Fig. 4. Path classification.

• **Criterion 1**: $E_1(P) = D_n(P) + D_d + D_i(S_{max}(P))$

$E_1(P)$ indicates whether the switching activity in the impact area of a sensitized path P can possibly affect the delay fault detection capability of P. $E_1(P) > T$ means that increasing switching activity in the impact area of P may help in detecting delay faults by P. Such a path is a ***long path***. On the other hand, $E_1(P) \le T$ means that increasing switching activity in the impact area of P cannot help in detecting delay faults by P. Such a path is a ***short path***. It is clear that pinpoint capture power management only needs to be conducted for long sensitized paths.

Definition 3: A sensitized path P for a test vector V is ***long*** (***short***) if $E_1(P) = D_n(P) + D_d + D_i(S_{max}(P)) > T$ ($\le T$).

• **Criterion 2**: $E_2(P) = D_n(P) + D_i(S(P))$

$E_2(P)$ indicates whether the current switching activity under the test vector V in the impact area of a long, sensitized, but defect-free path P, namely $S(P)$, causes an excessively-large delay increase on P. $E_2(P) > T$ means that a false timing failure may occur at the endpoint of P, causing a good chip to fail only in test mode. Such a path is a ***risky*** (***hot***) ***path***. $E_2(P) \le T$ means that the impact of the current switching activity is insufficient to invalidate the test response at the endpoint of P. Such a path is a ***safe path***.

Definition 4: A long sensitized path P for a test vector V is ***risky*** (***safe***) if $E_2(P) = D_n(P) + D_i(S(P)) > T$ ($\le T$). A risky path is also referred to as a ***hot path***.

• **Criterion 3**: $E_3(P) = D_n(P) + D_d + D_i(S(P))$

$E_3(P)$ shows whether the current switching activity under the test vector V in the impact area of a safe path P, namely $S(P)$, causes sufficient delay increase to help in detecting a delay defect of the typical size on P. $E_3(P) > T$ means that the current switching activity induces sufficient delay increase to detect a typical delay defect on P. Such a safe path is a ***warm path***. $E_3(P) \le T$ means that the delay increase caused by the current switching activity is insufficient to help in detecting a typical delay defect on P. Such a safe path is a ***cold path***.

Definition 5: A safe path P for a test vector V is ***warm*** (***cold***) if $E_3(P) = D_n(P) + D_d + D_i(S(P)) > T$ ($\le T$).

It is clear that the theoretical criteria of Fig 4(a) classify paths sensitized by a test vector from three perspectives: (1) path length, (2) switching activity in the impact area of a path in a defect-free case, and (3) switching activity in the impact area of a path in a defective case. ***Theoretical path classification*** can be conducted as follows:

• **Step-1** (***Long / Short***): Long paths are identified by E_1 as those sensitized paths on which capture power may help improve their capability for detecting delay defects.

• **Step-2** (***Risky / Safe***): Long sensitized paths are further classified into risky (hot) paths and safe paths by E_2, based on whether the current switching activity in the impact area of a long sensitized path may cause a false timing failure at its endpoint even when the path is defect-free.

• **Step-3** (***Cold / Warm***): Safe paths are further classified into warm paths and cold paths by E_3, based on whether the current switching activity in the impact area of a safe path may cause sufficient IR-drop-induced delay increase to help in detecting delay defects along the path.

The theoretical criteria shown in Fig. 4(a) for path classification are accurate but time-consuming for large circuits. In order to classify paths efficiently in an actual ATPG flow, ***practical criteria*** shown in Fig. 4(b) can be applied by using easy-to-compute parameters. ***Practical path classification*** can thus be conducted as follows:

- **Step-1** (***Long / Short***): Each sensitized path P is checked by the criterion $\boldsymbol{F_1}$ to see whether P is longer than a preset percentage (α) of the longest structural path. If so, P is a long path; otherwise, P is a short path.
- **Step-2** (***Risky / Safe***): Each long sensitized path P is further checked by the criterion $\boldsymbol{F_2}$ to see whether $WSA(P)$ (the current WSA-measured switching activity in the impact area of P) is higher than a preset percentage (β) of $WSA_{max}(P)$ (the maximum WSA in the impact area of P). If so, P is a risky (hot) path; otherwise, P is a safe path.
- **Step-3** ((***Cold / Warm***): Each safe path P is further checked by the criterion $\boldsymbol{F_3}$ to see whether $WSA(P)$ (the current WSA-measured switching activity in the impact area of P) is lower than a preset percentage (γ) of $WSA_{max}(P)$ (the maximum WSA in the impact area of P). If so, P is a cold path; otherwise, P is a warm path.

Practical criteria $\boldsymbol{F_1} \sim \boldsymbol{F_3}$ are easy to implement in any ATPG system and less costly to apply. More details about choosing α, β, and γ will be provided in Section 5.

3.2 Strategy for Pinpoint Capture Power Management

Based on the result of path classification for a test vector V, a strategy for applying pinpoint capture power management on V can be established as follows:

- ***Eliminating Hot Paths***: The impact of any hot path P should be avoided. This is achieved with a similar approach used in [12] by first reducing the switching activity in the impact area of P. If the reduction effect is insufficient to turn P into a safe (preferably warm) path, the expected test response bit for V at the endpoint of P is masked to instruct the tester to ignore the actual test response for V from P so as to avoid the possible negative impact of P.
- ***Warming-Up Cold Paths***: The switching activity in the impact area of a cold path P can be increased in an attempt to turn P into a warm path in order to improve its small-delay test capability. Even if P eventually remains as a cold path, increased switching activity in its impact area still helps improve its general delay test capability.
- ***Maintaining Warm Paths***: A warm path P has a right level of switching activity in its impact area. That switching activity will not cause any false timing failure when P is defect-free but will help fault detection when P has a delay defect of a typical size. Therefore, when dealing with hot or cold paths by pinpoint capture power management, special care should be taken so as not to change the status of any warm path in order to avoid compromising its small-delay test capability.

4. Proposed Test Generation Scheme

This section presents the proposed test generation scheme based on pinpoint capture power management. First, the general test generation scheme is outlined. After that, individual techniques are described in detail.

4.1 General Scheme

Fig. 5 shows the outline of the proposed test generation scheme. It consists of conventional test generation steps (**A**~**E**) and new steps (①~⑥) for pinpoint capture power management based on the strategy outlined in 3.2. New steps ②~④ form Phase-I (*Hot Path Elimination*) while new steps ⑤ and ⑥ form Phase-II (*Cold Path Warm-Up*).

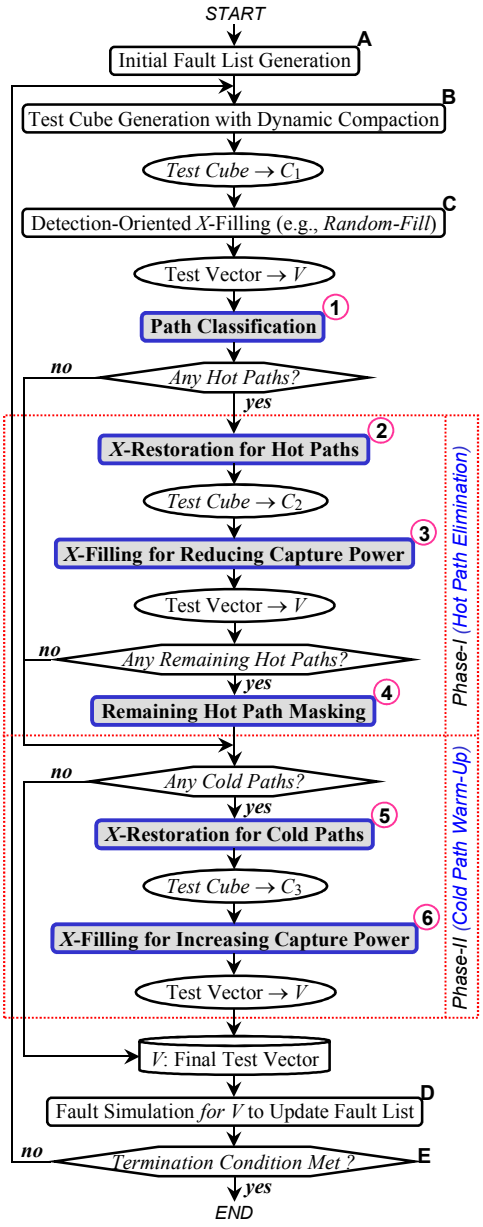


Fig. 5. Proposed test generation scheme.

In Fig. 5, conventional test generation (**A**~**E**) starts from initial fault list generation (**A**). Each test generation run begins with an all-X input vector, and logic values are gradually assigned to them. First, a partially-specified test cube C_1 is deterministically generated to detect a *primary fault* and dynamic compaction is optionally conducted to

detect ***secondary faults*** (**B**). Note that these primary and secondary faults are explicitly targeted faults in test generation. Since C_1 usually still contains *X*-bits even after aggressive dynamic test compaction, detection-oriented *X*-filling needs to be conducted to turn C_1 into a fully-specified test vector V (**C**). *Random-fill* is widely used for this purpose since its high fortuitous detection capability improves unmodeled-defect detection (thus *higher test quality*) and reduces test data volume (thus *lower test cost*). After that, fault simulation is conducted for V to update the fault list (**D**), and the termination condition is checked to decide whether to continue test generation (**E**).

It is clear that the initial test vector V, obtained by conventional test generation (**A**~**E**), consists of two types of logic bits, as defined below:

Definition 6: A logic bit in a test vector is a ***deterministic logic bit*** if it is deterministically generated for detecting explicitly targeted faults (i.e., primary and secondary faults) in conventional test generation.

Definition 7: A logic bit in a test vector is an ***X-filled logic bit*** if it is obtained by *X*-filling an *X*-bit in a partially-specified test cube without explicitly targeting any fault.

Fig. 6 illustrates the two types of logic bits in a test vector. It is clear that *deterministic logic bits* are responsible for intentionally detecting explicitly targeted faults, while *X-filled logic bits* are responsible for unintentionally-achieved fortuitous detection. This classification of paths is important for *X*-restoration to be described in Subsections 4.2.1 and 4.3.1.

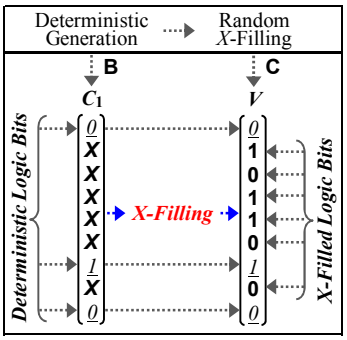


Fig. 6. Two types of logic bits.

The new test generation scheme is obtained by enhancing the conventional test generation scheme (**A**~**E**) with pinpoint capture power management. The enhancement consists of *path classification* (①), Phase-I (*Hot Path Elimination*) (②~④), and Phase-II (*Cold Path Warm-Up*) (⑤ and ⑥). The details of path classification have been provided in Subsection 3.1. Phase-I and Phase-II will be described in Subsections 4.2 and 4.3, respectively.

4.2 Phase-I: *Hot Path Elimination*

A test vector with even one hot path is risky for at-speed scan testing. To eliminate all hot paths in Phase-I, we have significantly improved a technique based on rescue-and-mask [12] so that it can not only achieve capture power safety by *eliminating all hot paths* but also avoid test quality degradation by *maintaining warm paths*. Phase-I consists of three steps (②~④ in Fig. 5) as follows:

- **Step-②** (***X-Restoration for Hot Paths***) to obtain *X*-bits that can only affect the impact areas of hot paths.
- **Step-③** (***X-Filling for Reducing Capture Power***) to determine proper logic values for the *X*-bits obtained by Step-② so as to reduce capture power around hot paths.
- **Step-④** (***Remaining Hot Path Masking***) to instruct the tester not to use the possibly-false test response bit that corresponds to the endpoint of any remaining hot path.

Step-② and Step-③ are for rescuing hot paths by trying to turn them into warm paths. On the other hand, Step-④ is for avoiding the impact of any remaining hot path if the rescue effort fails. By first rescuing and then masking, Phase-I can effectively guarantee capture power safety without causing severe test data inflation. This is because the more test response bits are masked, the more new test vectors usually need to be generated. Therefore, it is preferable to apply masking after rescuing is tried.

The details of the three steps in Phase-I are as follows.

4.2.1 X-Restoration for Hot Paths

X-restoration is a fast and efficient technique [12] for obtaining a partially-specified test cube with *X*-bits directly from a fully-specified test vector. Its basic idea is to keep all deterministic logic bits in a fully-specified test vector intact and only change some *X*-filled logic bits back into *X*-bits for a specific purpose, e.g., hot path elimination in this work. Note that, different from *X*-relaxation / *X*-identification [20], *X*-restoration adds no additional computational costs since it only utilizes the results of logic bit classification, which are naturally available in any conventional test generation flow.

In *X-restoration for hot paths* (② in Fig. 5), bits that are changed to *X*-bits are *X*-filled logic bits that can only affect hot paths by reaching the impact areas of hot paths but not warm paths. This guarantees that *X*-filling for the resulting test cubes only reduces the switching activity around hot paths (for contributing to capture power safety) while maintaining all warm paths (for keeping test quality).

X-restoration for hot paths is conducted as follows:

(**1**) The set of *X*-bit positions for all hot paths of a test vector V, denoted by $S_{X\text{-}bit\text{-}for\text{-}hot\text{-}paths}(V)$, is obtained by

$$S_{X\text{-}bit\text{-}for\text{-}hot\text{-}paths}(V) = S_{X\text{-}filled\text{-}logic\text{-}bits}(V) \cap \frac{S_{reach\text{-}hot\text{-}paths}(V) \cap}{S_{reach\,-\,warm\,-\,paths}(V)}$$

where $S_{X\text{-}filled\text{-}logic\text{-}bits}(V)$ is the set of all *X*-filled logic bit positions in V, $S_{reach\text{-}hot\text{-}paths}(V)$ is the set of all bit positions in V that can reach nodes (including both FFs and gates) in the impact areas of hot paths of V, and $S_{reach\text{-}warm\text{-}paths}(V)$ is the set of all bit positions in V that can reach nodes in the impact areas of warm paths of V.

(**2**) Turning the bits in $S_{X\text{-}bit\text{-}for\text{-}hot\text{-}paths}(V)$ into *X*-bits results in a partially-specified test cube C_2 at ② in Fig. 5.

An example of *X*-restoration for hot paths is shown in Fig. 7, where V = <0101101000111> and $S_{X\text{-}filled\text{-}logic\text{-}bits}(V)$ = <*b*, *c*, *d*, *e*, *f*, *h*, *j*, *k*, *m*>. If V has two hot paths P_1 and P_3 and one warm path P_2, $S_{reach\text{-}hot\text{-}paths}(V)$ = <*a*, *b*, *c*, *d*, *e*, *j*, *k*, *l*, *m*> and $S_{reach\text{-}warm\text{-}paths}(V)$ = <*e*, *f*, *g*, *h*, *i*, *j*>. As a result, $S_{X\text{-}bit\text{-}for\text{-}hot\text{-}paths}(V)$ = <*b*, *c*, *d*, *k*, *m*>. The resulting partially-specified test cube C_2 is thus <0*XXX*101000*X*1*X*>.

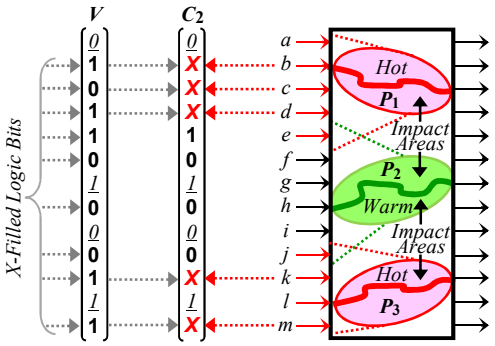


Fig. 7. Example of *X*-restoration for hot paths.

Different from the previous *X*-restoration technique [12], the improved technique for *X*-restoration for hot paths is more sophisticated in that it avoids any impact on warm paths, thus maintaining warm-path-related test quality.

Note that *X*-restoration (for hot paths as described in this subsection and for cold paths to be described in Subsection 4.3.1) does not affect the basic fault detection capability of a test vector achieved by its *deterministic logic bits*. *X*-restoration may only affect the fortuitous detection achieved by *X-filled logic bits* since it only changes some *X*-filled logic bits back into *X*-bits. As illustrated in Fig. 5, fault coverage loss due to *X*-restoration, if any, will be fully recovered by new test vectors generated in subsequent ATPG runs.

4.2.2 X-Filling for Reducing Capture Power

As shown in Fig. 5, after a test cube C_2 is obtained from a test vector V by *X*-restoration for hot paths (②), *X*-filling for reducing capture power (③) is conducted on C_2. Since the *X*-bits in C_2 only affect the impact areas of hot paths without affecting warm paths, the *X*-filling is ***pinpoint*** in that it only reduces switching activity around hot paths in an attempt to turn them into warm paths, without the risk of increasing switching activity around warm paths that may turn some of them into hot paths. Note that this pinpoint nature exists even when hot paths and warm paths or their impact areas overlap, as illustrated in Fig. 7.

There are two basic approaches to reducing capture power by *X*-filling: ***FF clock disabling*** and ***FF input-output equalizing***, as illustrated in Fig. 8. Here, the clock gator signal *CG* controls two FFs (FF_c and FF_d), and disabling the clock gator *CG* by *X*-filling will reduce two possible capture transitions from FF_c and FF_d. On the other hand, although the capture clock pulse cannot be stopped for FF_b, no capture transition will occur at FF_b if *X*-filling makes the same logic value to appear on its input and output.

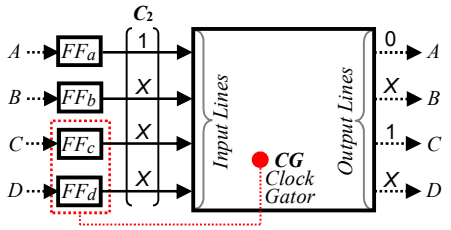


Fig. 8. Basic approaches to reducing capture power.

A hybrid procedure is used for *X*-filling for reducing capture power at ③ in Fig. 5 to turn a test cube C_2 to a test vector V. First, *FF clock disabling* is applied since it is effective even in test compression [4, 5, 18, 19]. After that, *FF input-output equalizing* is applied by using a fast and highly scalable *X*-filling technique based on *Preferred-fill* [14]. The details of the procedure are as follows:

```
Procedure-A X-Filling for Reducing Capture Power;
Input: C2 (a partially-specified test cube);
Output: V (a fully-specified test vector);
{
 // FF Clock Disabling
    A1: Conduct 3-valued logic simulation for C2.
    A2: For each clock gator with X, disable the
        clock gator signal by justifying 0 onto
        it through assigning proper logic values
        to some X-bits in C2.
 // FF Input-Output Equalizing
    A3: For all remaining X-bits (input lines)
        in C2, calculate the logic probabilities
        of their corresponding output lines in
        the circuit by assuming 50% 0-probability
        / 1-probablity for each X-bit in C2.
    A4: Assign 0 (1) to an X-bit in C2 if the 0-
        probability of its corresponding output
        line is greater (less) than its 1-
        probability.
}
```

Note that a clock gator having *X* after logic simulation (A1) means that all of its controlled FFs do not contribute to the basic fault detection capability of the initial test vector achieved by its *deterministic logic bits*; thus the FFs can be stopped by disabling the clock gator (A2).

Also note that in the above procedure, the switching activity in the impact area of each hot path can be monitored. If the switching activity is reduced to the level of a warm path, the corresponding hot path is said to be rescued. In this case, further *X*-filling for its impact area is stopped. This is to avoid turning the path into a cold path due to over-reducing capture power in its impact area.

4.2.3 Remaining Hot Path Masking

Even after *X*-filling for reducing capture power (③ in Fig. 5), some hot paths may remain due to insufficient switching activity reduction in their impact areas. In this case, ***masking*** [12] is applied (④ in Fig. 5) by putting a special symbol (*X* for most testers) at the expected test response bit for the endpoint of each remaining hot path. This symbol instructs the tester to ignore the test response bit from the path for the test vector since it may be faulted not by a delay defect but by excessive capture power. This guarantees capture power safety for the test vector.

Fig. 9 shows an example. *X*-filling for reducing capture power turns a test cube C_2 into a test vector V. As a result, the original hot path P_1 (shown in Fig. 7) becomes a warm (thus safe) path but the other original hot path P_3 remains. Although the expected test response bit from P_3 is 1, it is masked with *X* (meaning "*ignore*" on a tester) to avoid the possible negative impact of the remaining hot path P_3.

Note that masking-induced fault coverage loss, if any, will be recovered in subsequent ATPG runs as shown in Fig. 5. Also note that masking an output bit is only for the current test vector. For other test vectors, the output bit is not masked and available for fault detection.

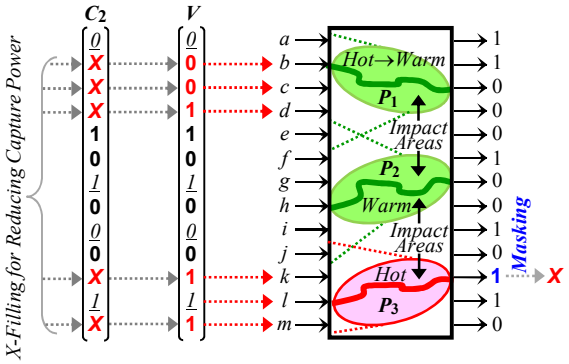


Fig. 9. Example of remaining hot path masking.

4.3 Phase-II: *Cold Path Warm-Up*

In the test generation scheme shown in Fig. 5, after Phase-I (*Hot Path Elimination*) is completed to achieve capture power safety, Phase-II (*Cold Path Warm-Up*) is conducted to increase switching activity around cold paths in order to improve their small-delay test capability. Phase-II consists of two steps (⑤ and ⑥ in Fig. 5) as follows:

- **Step-⑤** (***X-Restoration for Cold Paths***) to obtain *X*-bits that can only affect the impact areas of cold paths.
- **Step-⑥** (***X-Filling for Increasing Capture Power***) to determine proper logic values for the *X*-bits obtained by Step-⑤ so as to increase capture power around cold paths.

4.3.1 X-Restoration for Cold Paths

Similar to *X*-restoration for hot paths described in 4.2.1, *X*-restoration for cold paths can be conducted as follows:

(**1**) The set of *X*-bit positions for cold paths of a test vector *V*, denoted by $S_{X\text{-}bit\text{-}for\text{-}cold\text{-}paths}(V)$, is obtained by

$$S_{X\text{-}bit\text{-}for\text{-}cold\text{-}paths}(V) = S_{X\text{-}filled\text{-}logic\text{-}bits}(V) \cap \frac{S_{reach\text{-}cold\text{-}paths}(V) \cap}{S_{reach\,-\,warm\,-\,paths}(V)}$$

where $S_{X\text{-}filled\text{-}logic\text{-}bits}(V)$ is the set of all *X*-filled logic bit positions in *V*, $S_{reach\text{-}cold\text{-}paths}(V)$ is the set of all bit positions in *V* that can reach the impact areas of cold paths of *V*, and $S_{reach\text{-}warm\text{-}paths}(V)$ is the set of all bit positions in *V* that can reach nodes in the impact areas of warm paths of *V*.

(**2**) Turning the bits in $S_{X\text{-}bit\text{-}for\text{-}cold\text{-}paths}(V)$ into *X*-bits results in a partially-specified test cube C_3 at ⑤ in Fig. 5.

X-restoration for cold paths is illustrated by an example shown in Fig. 10. Here it is assumed that there are a cold path P_5 and a warm path P_6. In this case, $S_{X\text{-}filled\text{-}logic\text{-}bits}(V)$ = <*b*, *c*, *d*, *e*, *f*, *h*> h, $S_{reach\text{-}cold\text{-}paths}(V)$ = <*a*, *b*, *c*, *d*, *e*> and $S_{reach\text{-}warm\text{-}paths}(V)$ = <*e*, *f*, *g*, *h*, *i*>. The resulting partially-specified test cube C_3 is thus <0*XXX*10100>.

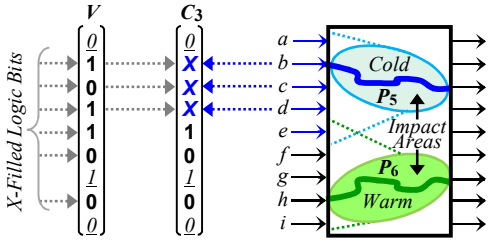


Fig. 10. Example of *X*-restoration for cold paths.

Similar to *X*-restoration for hot paths, the *X*-bits obtained by *X*-restoration for cold paths only affect the impact areas of cold paths but not warm paths. Note that some warm paths in Phase-II may be originally hot paths but later rescued in Phase-I. Thus, avoiding impact on warm paths helps in maintaining not only test quality but also capture power safety achieved in Phase-I.

4.3.2 X-Filling for Increasing Capture Power

In the test generation scheme of Fig. 5, after a test cube C_3 is obtained from a test vector *V* by *X*-restoration for cold paths (⑤), *X*-filling is conducted on C_3 for increasing capture power (⑥). Since the *X*-bits in C_3 only affect the impact areas of cold paths, the *X*-filling is ***pinpoint*** in that it only increases switching activity in the impact areas of cold paths, without running the risk of accidentally increasing switching activity around warm paths that may turn some of them into hot paths. Note that this pinpoint nature exits even when cold paths and warm paths or their impact areas overlap, as illustrated in Fig. 10.

Generally, *X*-filling for increasing capture power can be conducted by ***reversing*** the operations used for *X*-filling for reducing capture power (described in 4.2.2). In this work, we use the following procedure for this purpose:

```
Procedure-B X-Filling for Increasing Capture Power;
Input: C3 (a partially-specified test cube);
Output: V (a fully-specified test vector);
{
 // FF Clock Enabling
    B1: Conduct 3-valued logic simulation for C3.
    B2: For each clock gator with X, enable the
        clock gator signal by justifying 1 onto
        it through assigning proper logic values
        to some X-bits in C3.
 // FF Input-Output Non-Equalizing
    B3: For all remaining X-bits (input lines) in
        C3, calculate the logic probabilities of
        their corresponding output lines in the
        circuit by assuming 50% 0-probability /
        1-probablity for each X-bit in C3.
    B4: Assign 1 (0) to an X-bit in C3 if the 0-
        probability of its corresponding output
        line is greater (less) than its 1-
        probability.
}
```

Procedure-B is the reversion of *Procedure-A* used for *X*-filling for reducing capture power (described in 4.2.2). As in *Procedure-A*, the switching activity in the impact area of each cold path can be monitored. If the switching activity is increased to the level of a warm path, the corresponding cold path is said to be successfully warmed-up. In this case, further *X*-filling for its impact area is stopped. This is to avoid turning the path into a hot path due to over-increasing capture power in its impact area.

4.4 Extension to Test Compression

The descriptions so far in this paper are focused on the non-test-compression environment. Nonetheless, the proposed ATPG scheme can be readily applied to broadcast-scan-based test compression through simple circuit model extension [4,22]. For linear-decompression-based test compression, the basic idea of this paper still applies. Especially, masking will remain effective for achieving capture power safety, while clock-gator-based direct ATPG [18, 19] will be needed for the part of *X*-restoration/*X*-filling-based capture power management.

5. Experiment Results

The proposed test generation scheme was implemented in *C* based on a broadcast-scan-based-test-compression tool (*VirtualScan*™), and evaluated on large ITC'99 benchmark circuits. Circuit statistics, including information on longest structural path lengths (`Max. Path Length`), are shown in Table 2. Evaluation experiments were conducted on a workstation with an Intel Xeon® 3.33 GHz CPU.

Table 2. Circuit Statistics

Cir.	# of Gates	# of FFs	Max. Path Length
b17	40,918	1,415	44
b18	99,467	3,320	62
b19	196,305	6,642	66
b20	16,013	490	61
b21	16,579	490	61
b22	23,349	735	59

5.1 Results

Table 3 shows the results of conventional ATPG as the baseline for evaluation. A split ratio of 1:8 was used for test compression. Test vector count (`# of Vectors`) is for evaluating test costs, while transition fault coverage (`FC`), *bridging coverage estimate* (`BCE`) [23], and *statistical delay quality level* (`SDQL`) [2] are for evaluating test quality. *BCE* and *SDQL* are effective in assessing the detection capability of unmodeled structural defects (e.g., bridging defects) and small-delay defects, respectively.

Table 3. Results of Conventional ATPG

Cir.	Conventional ATPG					CPU (Sec.)
	# of Vectors	%Risky Vectors	FC (%)	BCE (%)	SDQL	
b17	1,568	3.8	82.8	39.3	1358.4	491
b18	2,592	1.9	78.0	46.6	1292.8	1,869
b19	3,776	0.2	76.0	45.6	3329.1	2,196
b20	1,280	2.2	80.9	43.1	282.3	264
b21	1,330	3.9	83.1	42.9	187.8	224
b22	1,444	13.0	81.4	44.2	255.7	533

Path classification was also conducted for test vectors generated by conventional ATPG. First, *long sensitized paths* (*LSPs*) were identified by using a fast sensitization checking algorithm [24] and the practical criterion $\boldsymbol{F_1}$ (Fig. 4(b)) with $\alpha = 70\%$. That is, a sensitized path whose length was longer than 70% of the longest structural path in a circuit was considered an LSP. After that, a hot path was identified by using the practical criterion $\boldsymbol{F_2}$ (Fig. 4(b)) with $\beta = 30\%$. That is, an LSP was considered a hot path if the WSA in its impact area was higher than 30% of the maximum WSA in its impact area. Furthermore, a cold path was identified by using the practical criterion $\boldsymbol{F_3}$ (Fig. 4(b)) with $\gamma = 10\%$. That is, an LSP was considered a cold path if the WSA in its impact area was lower than 10% of the maximum WSA in its impact area. These parameters were set by assuming a 20% functional toggle rate. It can be seen that all circuits had some risky test vectors as shown under `% of Risky Vectors` in Table 3. This result also clearly demonstrates the needs for guaranteeing capture power safety in at-speed scan testing.

Table 4 shows the results of applying the proposed ATPG, whose biggest advantage is *guaranteed capture power safety* achieved by hot path elimination. Another advantage is that the impact of the proposed ATPG on test costs and test quality is minimal as evidenced by the percentage changes in test vector count and three test quality metrics (*FC*, *BCE*, *SDQL*) as shown under `Δ# of vectors`, `ΔFC`, `ΔBCE`, and `ΔSDQL`, respectively.

Table 4. Results of Proposed ATPG

Cir.	Proposed ATPG					CPU (Sec.)
	Δ# of Vectors (%)	%Risky Vectors	ΔFC (%)	ΔBCE (%)	ΔSDQL (%)	
b17	0.20	0	0.14	-0.45	-2.02	683
b18	1.45	0	0.06	-0.41	-0.17	2,931
b19	0.15	0	0.03	-0.07	-0.65	3,229
b20	0.21	0	0.08	+1.86	+0.63	532
b21	0.17	0	0.05	-1.10	-0.98	394
b22	0.30	0	0.11	-0.68	-2.03	1,150

Table 5 shows the details of Phase-I (*Hot Path Elimination*) in the proposed ATPG (Fig. 5) for guaranteeing capture power safety. The number of long sensitized paths and the percentage of hot paths are shown under `# of LSPs` and `% of Hot Paths`, respectively. The percentage of *X*-bits obtained by *X*-restoration (② in Fig. 5) is shown under `% of Restored X-Bits`, and the rescue rate (i.e., the percentage of hot paths becoming warm paths) achieved by *X*-filling for reducing capture power (③ in Fig. 5) is shown under `Rescue Rate (%)`; maximum and average WSA reduction rates for impact areas of hot paths are shown under `Max. WSA Reduction Rate (%)` and `Ave. WSA Reduction Rate (%)`, respectively; the number of test response bits masked for remaining hot paths (④ in Fig. 5) is shown under `# of Masked Test Res. Bits`. It can be seen that the powerful masking operation for guaranteeing capture power safety only masks a relatively small number of test response bits with respect to the number of remaining hot paths. This is because many hot paths share the same endpoint.

Table 5. Details of Phase-I (*Hot Path Elimination*)

Cir.	Path Info.		X-Restoration/Filling-Based Resuce				Masking
	# of LSPs	% of Hot Paths	% of Restored X-Bits	Rescue Rate (%)	Max. WSA Reduction Rate (%)	Ave. WSA Reduction Rate (%)	# of Masked Test Res. Bits
b17	1337	11.1	13.7	4.0	10.5	0.7	85
b18	1124	18.7	11.3	4.8	10.8	1.4	24
b19	1641	0.3	25.0	40.0	17.6	14.2	1
b20	1161	3.2	0.6	0.0	0.1	0.1	4
b21	1371	50.3	3.6	0.0	1.6	0.1	25
b22	2748	36.9	4.9	1.6	3.3	0.2	73

Table 6 shows the details of Phase-II (*Cold Path Warm-Up*) in the proposed ATPG (Fig. 5) for improving small-delay test capability. The percentage of cold paths for each circuit is shown under `% of Cold Paths`. The percentage of *X*-bits obtained by *X*-restoration (⑤ in Fig. 5) is shown under `% of Restored X-Bits`; maximum and average WSA increase rates for impact areas of cold paths achieved by *X*-filling for increasing capture power (⑥ in Fig. 5) are shown under `Max. WSA Increase Rate (%)` and `Ave. WSA Increase Rate (%)`, respectively. `% of Cold→Warm` shows the percentage of cold paths becoming warm paths (i.e., the best result of cold path warm-up).

Table 6. Details of Phase-II (*Cold Path Warm-Up*)

Cir.	Path Info.		X-Restoration/Filling-Based Warm-Up			
	# of LSPs	% of Cold Paths	% of Restored X-Bits	Max. WSA Increase Rate (%)	Ave. WSA Increase Rate (%)	% of Cold→Warm
b17	1337	7.3	24.9	18.7	2.6	4.1
b18	1124	3.2	31.0	12.7	6.5	27.8
b19	1641	47.0	26.9	16.6	3.1	5.6
b20	1161	1.5	3.1	9.0	2.1	11.8
b21	1371	3.1	6.3	7.7	0.4	2.4
b22	2748	1.8	5.7	3.2	0.1	3.8

Note that even if the switching activity around a cold path is not sufficiently increased to turn it into a warm path, its delay test capability may still improve. This has been confirmed by delay analysis on ITC'99 benchmark circuit *b19* with *VCS*©, *PrimeRail*, and *PrimeTime*®. Synopsys 90nm Generic Library was used and a test cycle time of 9ns was assumed. Fig. 11 shows the results of 50 cold paths for two test vectors, in terms of the slack change (`% Path-Slack-Change`) of each path and the WSA change in its impact area (`% Impact-Area-WSA-Change`).

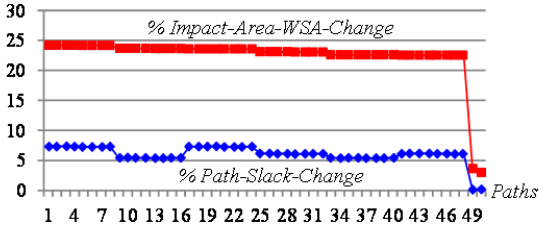


Fig. 11. Detailed delay analysis for cold paths.

Note that *SDQL* values shown in Tables 3 and 4 do not reflect power supply noise caused by switching activity of individual test vectors. In this sense, detailed delay analysis provides a better assessment of delay test capability.

5.2 Discussions

- Table 3 shows that risky vectors are sparse in most cases. In addition, hot paths often cluster together for a risky test vector. This indicates that the conventional approach of reducing capture power unconditionally for all test vectors and globally across the whole chip may be both *wasteful* (i.e., causing test data inflation) and *harmful* (i.e., compromising test quality). This fact further highlights the need for a paradigm shift from *global* capture power management to *pinpoint* capture power management.
- The proposed ATPG scheme is easy to integrate into any ATPG flow. All added processes, including *X*-restoration, *X*-filling, and masking, are highly scalable since they only need one pass of structural cone analysis, 3-valued logic simulation, and probability estimation for each risky test vector. In addition, there is no risk of fault coverage loss since masking is only for the current test vector, and faults becoming undetected due to the current masking can be detected by subsequently generated test vectors.

6. Conclusions

This paper is the first that has proposed ***pinpoint capture power management*** and has established a novel at-speed scan test generation scheme based on it. Compared with the conventional (global / unfocused) capture power reduction, the proposed scheme has three significant advantages: *guaranteed capture power safety*, *improved small-delay test capability*, and *minimal test cost impact*. Applicable both in-ATPG and post-ATPG, pinpoint capture power management has the potential of leading to the next-generation capture-power-aware ATPG to meet the industry's growing needs for capture-power-safe, low-cost, and high-quality at-speed scan test vectors.

Acknowledgements

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