STAHL: A Novel Scan-Test-Aware Hardened Latch Design

Ruijun Ma[1], Stefan Holst[1], Xiaoqing Wen[1], Aibin Yan[2], and Hui Xu[3]

[1]Kyushu Institute of Technology, Iizuka 820-8502, Japan

[2]Anhui University, Hefei 230601, P. R. China

[3]Anhui University of Science & Technology, Huainan 232000, P. R. China

***Abstract*—As modern technology nodes become more susceptible to soft errors, many radiation hardened latch designs have been proposed. However, redundant circuitry used to tolerate soft errors in such hardened latches also reduces the test coverage of cell-internal manufacturing defects. To avoid potential test escapes that lead to soft error vulner-ability and reliability issues, this paper proposes a novel Scan-Test-Aware Hardened Latch (STAHL). Simulation results show that STAHL has superior defect coverage compared to previous hardened latches while maintaining full radiation hardening in function mode.**

Keywords—soft error, hardened latch, defect, scan test

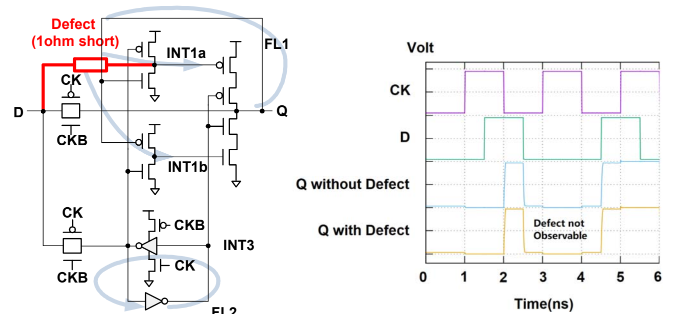
I. INTRODUCTION

The continuing trend towards low power and higher integration lead to smaller feature sizes and lower supply voltages for Integrated Circuits (ICs). As a result, the amount of charge that defines the state of storage cells, such as latches, gets smaller, making them more vulnerable to *Single-Event-Upsets* (SEUs) caused by radiation [1-3]. Modern ICs are becoming increasingly suspectible to soft errors [4-6], not only in high-radiation environments, such as aerospace [7], but also at the sea-level [8-9].

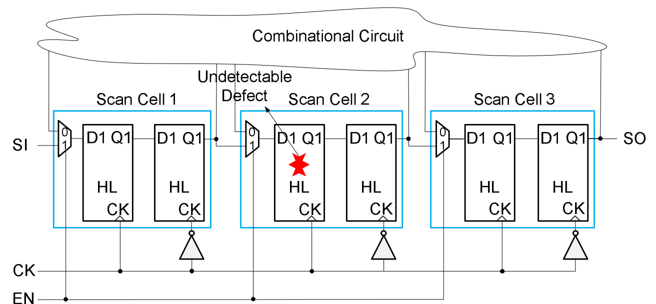
An SEU occurs when a particle strikes a sensitive node within a latch and changes its stored value. To mitigate SEUs, many radiation hardened latch designs have been proposed [10-16]. A hardened latch usually stores its state in multiple redundant feedback loops. When one of the feedback loops is hit by a particle, the changed state is corrected by the information stored in other loops. In addition, a simple voter (e.g., a C-element) prevents transi-ent errors from appearing at the output of the hardened latch.

However, the existence of redundant feedback loops and voters in hardened latches may prevent the detection of production defects as their effects may be masked by the same circuitry designed to mask transient errors. Fig. 1 (a) shows an example of a typical latch [16] with a short defect between D and INT1a. The SPICE simulation result in Fig.1 (b) reveals that this defect is not observable at Q and therefore is not testable. In addition, we have shown in our previous work [17] that defects like these compromise the hardness of a latch and make it vulnerable to certain particle hits.

Scan design is the most commonly used design-for-test methodology for effectively testing sequential logic circuits [18]. In full scan design, all storage cells in a circuit are replaced with scan cells, which are then connected into scan chains for loading test vectors as well as observing test responses. If such a scan cell is based on a hardened latch, defects in the scan cells may not be detected as shown in Fig.1 (c), thus causing the risk of passing defective chips in scan test. In general, many previous hardened latches [10-16] have high performance but are unsuitable for scan test as their redundancy may mask the detection of cell-internal defects. A few hardened latches [19-20] have been proposed to enhanced delay fault testing. However, defects within hardened latch structures themselves are not targeted. Therefore, there is a strong need to test for cell-internal manufacturing defects in hardened latches since they may lead to compromised soft error tolerance [17] or early-life failures.



(a) HiPeR [16] with a short defect (b) SPICE simulation



(c) Scan chain structure with hardened latch (HL)

Fig. 1 The Impact of Production Defects

This paper proposes a novel Scan-Test-Aware Hardened Latch design (STAHL). It can tolerate soft errors in function mode and is easily tested in scan mode. STAHL can be readily inserted into existing scan-designs without additional control signals or scan chains. To the best of our knowledge, this work is the first to address the testability of production defects within hardened latches.

This paper is organized as follows: The structure of STAHL is described in Section II. Section III shows the usage of STAHL in scan chains and a novel test procedure. Section

IV shows evaluation results and Section V concludes the paper.

II. SCAN-TEST-AWARE HARDENED LATCH (STAHL)

Fig. 2 shows the structure of the proposed STAHL latch. Instead of using just one input D and one input Q as in a common latch, STAHL has two inputs (D0 and D1) as well as two corresponding outputs (Q0 and Q1). In addition to the normal clock signals CK and CKB, STAHL has an additional control input EN that switches between shift mode (EN = 1) and function mode (EN = 0). ENB is the inverse signal of EN. STAHL contains two independent feedback loops (FL0 and FL1) formed by 4 transmission gates (TG1 to TG4) and 6 inverters (I1 to I6). Two C-elements (CE0 and CE1) are used to prevent soft errors from appearing at the outputs.

The inputs of the C-elements are driven by two multiplexers (MUX0 and MUX1) that switch to different feedback loops depending on the two modes. The detailed operations in these two modes are discussed below.

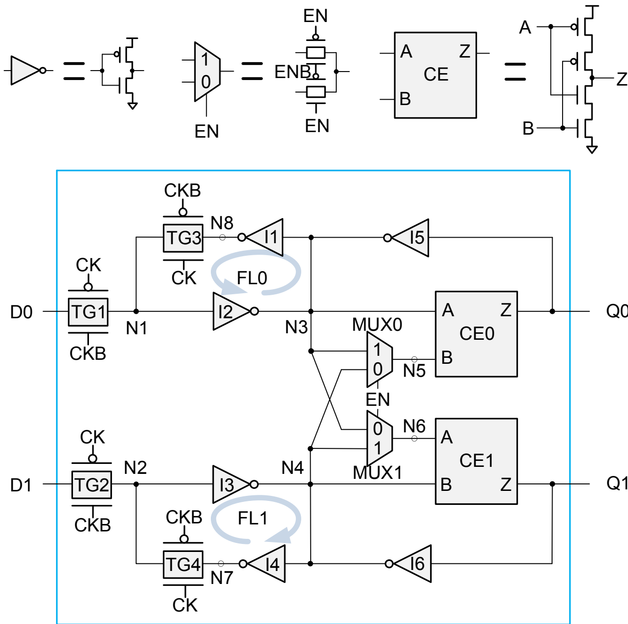


Fig. 2 Structure of the Proposed STAHL Latch

A. Function (Hardened) Mode

The STAHL latch is in function mode when EN = 0. Fig. 3 shows the equivalent circuit for this mode. In function mode, the value to be stored in the latch needs to be applied to both inputs D0 and D1.

In the transparent phase (CK = 0), the transmission gates TG1 and TG2 are ON. The input value at D0 (D1) propagates through N1 (N2), inverter I2 (I3), node N3 (N4), C-elements CE0 and CE1 to both outputs Q0 and Q1.

In the latching phase (CK = 1), the transmission gates TG1 and TG2 are OFF, while TG3 and TG4 are ON. There are two feedback loops, FL0 and FL1. FL0 consists of inverters I1, I2, and the transmission gate TG3. FL1 consists of inverters I4, I3, and the transmission gate TG4. Particle strikes can be tolerated by STAHL as follows. Both feedback loops FL0 and FL1 will store the same value and each of the C-elements is connected to both loops. If any of the feedback loops gets affected by a particle strike, both C-elements will stop driving the outputs Q0 and Q1 and therefore mask the soft error.

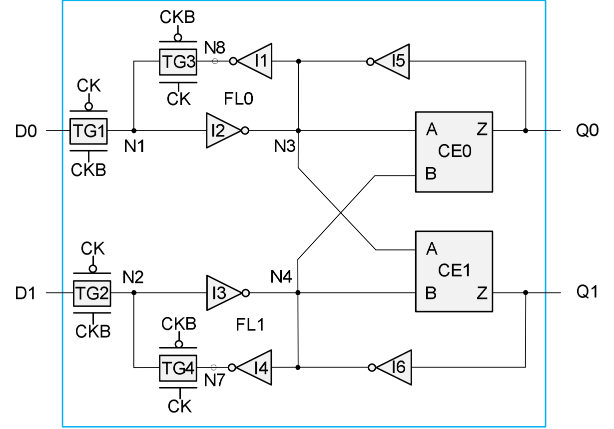


Fig. 3 EN = 0: Function Mode (Hardened)

Suppose that node N1 is affected by an SEU and that the logic value of N1 is temporally changed. Node N3 is influenced by this SEU through inverter I2. Since nodes N1 and N8 are equivalent, they are influenced too. However, nodes N4 is not influenced by this transient, leaving the outputs Q0 and Q1 in a high-impedance state. The correct output logic value at Q0 will propagate back through inverter I5 to restore the changed node N1. Similar analysis can be made for SEUs occuring on nodes N3 and N8.

Due to the symmetric nature of STAHL, the same discussion holds for an SEU at node N2 and similar analysis can be made for SEUs on nodes N4 and N7.

B. Shift Mode

The STAHL latch is in shift mode when EN = 1. Fig. 4 shows the equivalent circuit for this mode. In shift mode, both feedback loops operate completely independent of each other, effectively forming two independent latches D0 – Q0 and D1 – Q1. Both inputs of CE0 are connected to FL0 while both inputs of CE1 are connected to FL1; thus, they act as simple inverters.

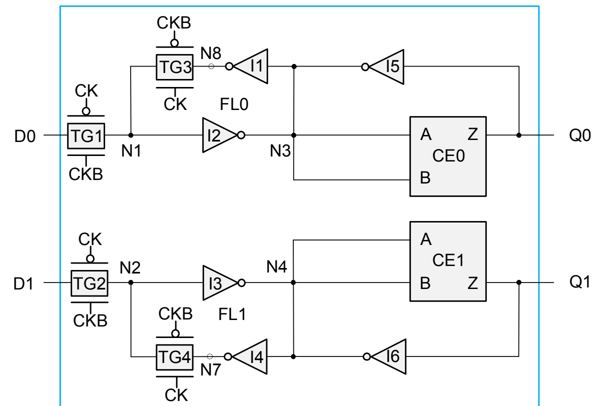


Fig. 4 EN = 1: Shift Mode (Two Independent Latches)

Both feedback loops can be tested in the same way as standard non-hardened latches. The only structures that

cannot be completely tested in scan mode are the cross-connections from the FL0 to CE1 and FL1 to CE0. It is because that the two cross-connections are turned OFF during the shift mode.

III. Scan Chain Based on STAHL

A. Scan Chain Structure

Fig. 5 shows a STAHL-based scan cell. Two STAHL latches are used to form a flip-flop, and two additional multiplexers are used to complete the scan cell. The input D and output Q connect with the combinational portion.

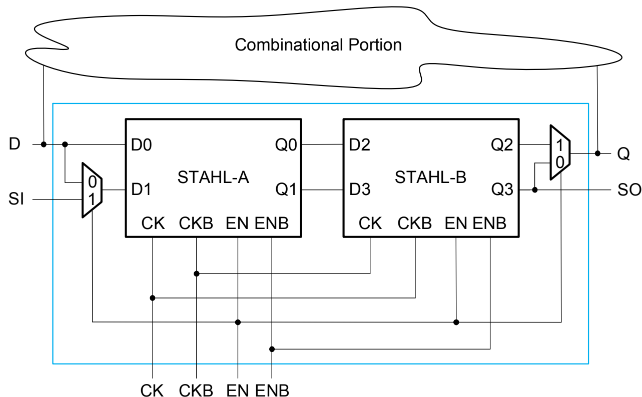


Fig. 5 STAHL-based Scan Cell

When EN = 0, the scan cell operates in function mode. In function mode, both STAHL latches are hardened against soft errors. The input D is applied to both inputs D0 and D1 of the STAHL-A latch. The output Q of the scan cell is connected to the output Q3 of the STAHL-B latch.

When EN = 1, the scan cell operates in scan mode. In scan mode, both STAHL-A and STAHL-B operate as two independent flip-flops and can store two values simultaneously. The flip-flop D0 – Q2 is connected D and Q of the scan-cell. The flip-flop D1 – Q3 is connected to the SI (scan-in) and SO (scan-out) of the scan-cell. Since both flip-flops operate independently, the combinational portion of the design continues to operate just as in function mode while test data is shifted from SI to SO.

Fig. 6 shows an example of a STAHL-based scan chain with three scan-cells. All connections between the scan-cells are identical to traditional scan design. The behavior of the STAHL-based scan chain, however, is more similar to an enhanced scan approach [19] than a standard scan design.

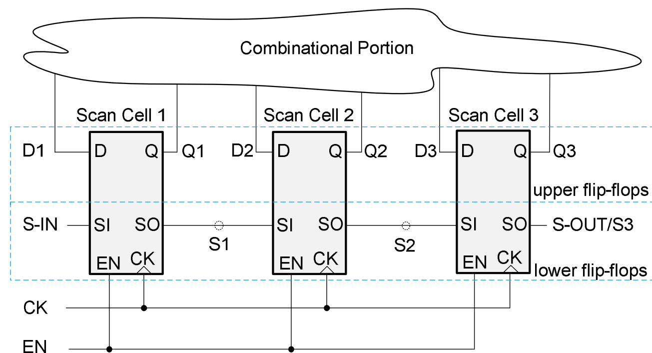


Fig. 6 STAHL-based Scan Chain

B. Test Procedure

In shift mode (EN = 1) test data can be shifted from S-IN to S-OUT via the lower flip-flops in each scan cell. In Fig. 6, the design-under-test (DUT) consists of three scan cells and the combinational portion. With each clock cycle, the DUT executes function clock cycles via the upper flip-flops in each scan cell. This is different from enhanced scan, where the inputs to the combinational parts of the design are held stable during shifting. The reason of having the DUT execute functional clock cycles during shifting is that this allows to load every value combination into the two halves of the STAHL latches without additional hardware or test data overhead. For example, while a standard scan flush test is performed on the lower flip-flops, the combinational portion of the DUT will load various different values into the upper flip-flops, thus increasing the coverage of short defects within the scan cells.

When a test pattern is completely shifted in, EN is set to 0 in preparation for conducting the capture operation. With the falling edge of EN, the output Q of each scan cell switches to the values of the shifted-in test pattern. The pattern starts to propagate through the combinational portion of the DUT and the next rising clock edge will capture the result. The time between the falling edge of EN and the rising edge of CK defines the capture time. By changing this capture time, it is possible to observe not only the response to the current test pattern but also the response to the last functional state of the DUT. This is important in order to test both halves of the STAHL-based scan cells.

Taking the scan cell in Fig. 5 as an example, when a test vector is completely shifted into the scan cell, EN is set to 0 and node Q3 connects with output Q. The test vector is propagating through the output Q to the combinational portion and after the next clock cycle, the scan cell will capture the response of the test vector.

A *standard capture cycle* allows enough time for the combinational portion to propagate the test pattern. It allows the detection of all testable defects in the combinational logic as well as the lower flip-flops in the scan cells including the output multiplexer at Q.

The values in the upper flip-flops, however, are not observable. To observe these, we introduce a *fast capture cycle*. For the fast capture cycle, the falling edge of EN is placed right before the next rising edge of the clock. Before the fast capture cycle, the combinational logic has calculated the response to the state currently stored in the upper flip-flops of the scan cells. The fast capture cycle will capture exactly this response, because the test pattern that has been applied to the circuit with the falling edge of EN does not have enough time to propagate. Assuming that the combinational portion provides enough hold-time at each scan cell, the fast capture cycle will provide observability for the upper flip-flops and allows testing for defects in these parts.

The *fast capture cycle* requires strict constraints on the timing between the clock (CK, CKB) and the scan enable signals (EN, ENB). These may be difficult to meet especially with rising process variations and if the hold-time of the combinational portion is insufficient. The reason of

using *fast capture cycle* is to avoid the need of additional control signals to be routed to each scan cell. If the timing demands for the *fast capture cycle* turn out to be too expensive to ensure, one can easily achieve the same effect by controlling the output multiplexer of the scan cells with a separate control signal instead of scan enable. This would allow leaving Q connected to Q2 from STAHL-B (see Fig. 5) while performing a capture with normal timing and thus observing Q2 through the combinational portion.

Fig. 7 shows an example of a test procedure that uses both capture types to completely test the scan chain. The test starts with applying two bits Fa and Fb that are shifted through the scan chain in a scan flush test. This allows testing for defects in the lower flip-flops of the scan chain. Next, a test pattern (S1 S2 S3 = 111) is loaded into the chain and the standard capture cycle is executed. The combinational portion, which in this example just inverts its input, calculates the response (000) which is then captured, shifted out and checked. With each consecutive clock cycle after capture, the combinational portion will continue to execute functional clock cycles based on the last test pattern. This can be seen in the waveform for d2, which continues to oscillate between 0 and 1 regardless of the test data loaded in the scan chain. The following fast capture cycle at 5.25ns loads the current output of the combinational portion into the scan chain (R'1 R'2 R'3 = 111) for observation.

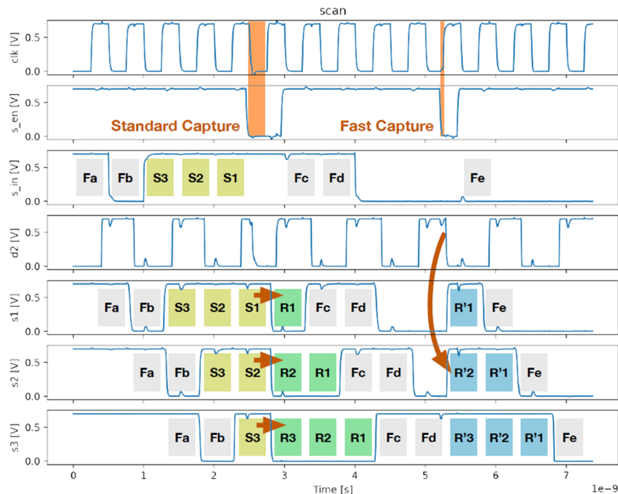


Fig. 7 Test Procedure of the Scan Chain

IV. Experimental Results

The proposed latch was simulated using the 16nm predictive technology model [22] with a 0.7 V supply voltage and a clock frequency of 2 GHz at the room temperature. Transistors aspect ratios were set as follows: W/L = 1 for both PMOS and NMOS transistors in inverters I1, I2, I3, I4, I5, I6 as well as transmission gates TG3, TG4, and two multiplexers (MUX0 and MUX1). W/L = 8 for the PMOS transistors and W/L = 4 for the NMOS transistors of the transmission gates TG1 and TG2. W/L = 4 for the PMOS transistors and W/L = 2 for the NMOS transistors of CE1, CE2 to increase the driving strength of the C-elements. For fair comparison the minimum possible transistor sizes for making the latches work properly were applied [14].

Table 1 shows the statistics of the latches targeted in our experiments. The columns show the latch names, defect counts, transistor counts, power consumption, propagation delay, power-delay product, SEU Immunity, CG (Clock Gate) Suitability, respectively. Standard is an unhardened latch design used as the base line, TMR is a standard triple modular redundancy implementation consisting of three standard latches and a voter. The remaining 7 latches are hardened latches and the last one is STAHL.

Table 1. Basic Statistics of All Considered Latches

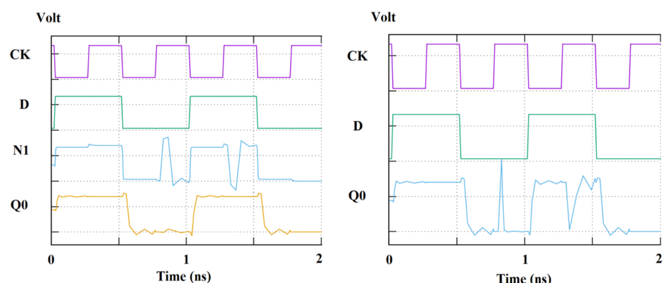
Latch	#Defect	#Trans.	Power (*uW*)	Delay (*ps*)	PDP (*E-18J*)	SEU Immunity	CG Suitability
Standard	47	12	0.13	10.56	1.37	NO	YES
TMR	216	48	0.15	13.64	2.05	YES	YES
FERST [13]	189	28	0.18	24.57	4.42	YES	NO
HLR [14]	167	24	0.41	5.84	2.39	YES	NO
HiPeR [16]	99	18	0.41	7.08	2.90	YES	NO
ISEHL [15]	204	24	0.25	5.51	1.38	YES	YES
HLR-CG1 [14]	74	18	0.49	5.87	2.88	YES	YES
HLR-CG2 [14]	224	24	0.05	4.67	0.23	YES	YES
[21]	306	36	0.07	19.24	1.35	YES	YES
STAHL	240	36	0.77	27.11	20.87	YES	YES

A. *Hardness against Soft Errors*

SEUs were injected into the proposed STAHL latch and the simulation waveforms are shown in Fig. 8. A double exponential sharp pulse current was applied to simulate SEUs occurring in the latch phase.

$$I(t) = I_0(e^{-t/\tau_1} - e^{-t/\tau_2})$$

As shown in Fig. 8 (a), SEU was injected into node N1. The logic value of N1 was temporally changed. The correct output logic value at Q0 propagated through inverter I5 to restore the changed node. As shown in Fig. 8 (b), SEU was injected into the node Q0. The logic value of Q0 temporally changed. The correct logic value was recovered within a time interval depending directly on the amount of charge injected by the hitting particle, and inversely on the conductance of transistors driving the output node.



(a) SEU at N1 (b) SEU at Q0

Fig. 8 Impact of SEU on Internal Nodes

In order to analyze the robustness of the latches, the critical charges of internal nodes for all considered latches were evaluated by simulation. There are three types of nodes [16].

Type-1: An SEU only generates a voltage pulse on the same node without propagating to the output node, regardless of the energy of the striking particle. The critical charge of such a node is commonly set to infinity: $Q_{crit} \rightarrow \infty$.

Type-2: An SEU generates a voltage pulse that may propagate to the output, whose correct value is restored within a time interval related to the particle energy and to the strength of the C-elements driving node. As introduced before, even though the correct value of the output of a latch is recovered, the glitch generated at the output may propagate through the downstream logic and lead to a soft error. For such nodes, the critical charge Q_{crit} is defined as the amount of charge required to generate an output glitch with the voltage amplitude equal to half the supply voltage.

Type-3: An SEU generates an upset at the output of the latch. This type of node is the most critical one since a continuing wrong output is generated.

For the proposed STAHL latch, there are thirteen Type-1 internal nodes. The critical charge was assumed to be infinity. There is one Type-2 internal node (Q0). For this node, a critical charge of $Q_{crit} = 0.3\, fC$ was estimated by simulation for the proposed latch. The greater of the amount of critical charge, the more robust the sensitive node is. Note that the proposed STAHL latch has no Type-3 nodes.

Table 2 shows the results of soft error rate (SER) of all considered latches, susceptible node counts, and the critical charge Q_{crit}, respectively. All hardened latches, including STAHL, can tolerate transient faults (thus SER = 0) if they are defect-free. The number of susceptible nodes and their Types are summarized in Table 2.

Table 2. Soft Error Hardness

Latch	SER(%)	Type-1	Type-2	Type-3	Qcrit (fC)
Standard	80.0	0	0	3	0.6
TMR	0.0	14	1	0	0.6
FERST [13]	0.0	12	2	0	1.8
HLR [14]	0.0	12	1	0	0.8
HiPeR [16]	0.0	8	1	0	0.3
ISEHL [15]	0.0	14	1	0	0.5
HLR-CG1 [14]	0.0	6	1	0	0.6
HLR-CG2 [14]	0.0	15	1	0	0.6
[21]	0.0	16	3	0	0.2
STAHL	0.0	13	1	0	0.3

The critical charge Q_{crit} denotes the amount of collected charges that generate an output glitch and the glitch has a voltage amplitude equal to half of the supply voltage. This means that if the collected charge is less than the Q_{crit}, the SEU on the nodes of Type-2 can not lead to a soft error in the downstream circuit. For the Standard latch, the number of Q_{crit} in Table 2 represents the critical charge of nodes of Type-3.

B. Defect Coverage

This section compares the STAHL latch with state-of-the-art hardened latches in terms of defect coverage (DC) and the *Post-Test Vulnerability Factor* (PTVF) [17]. Between power supply and a latch cell, a resistor of 10Ω was inserted to allow for supply voltage drop in case of excessive power consumption of a defective cell. Most published hardened latch designs do not provide actual cell layouts. For fair comparisons, we used the worst case defect model (every possible defect based on the latch structure) instead of layout-based defect models.

The set of targeted manufacturing defects include transistor open defects and short defects between internal nets in a latch. For a transistor open defect, a resistor of 10MΩ was inserted at the source of the transistor. Since there are 36 transistors in STAHL, 36 transistor open defects were considered. As for short defects, the set of nets were classified into external and internal ones. External nets are GND, VDD, CK, CKB, EN, and ENB, while internal nets are the remaining nets as shown in Fig.5. Since a short defect between two external nets (e.g., VDD and GND) can always be detected, such shorts are excluded from consideration. A short defect was injected into the SPICE netlist of the proposed latch with a resistor of 1Ω between the two nets.

We used the worst case for analysis with a total of 240 assumed defects, including 36 transistor open defects and 204 net short defects. The other latches are simulated in the same way.

Table 3 shows the results of defect coverage (DC) and PTVF, respectively. DC is measured by the defect detection ratio. Higher DC means higher test quality. The Post-Test Vulnerability Factor (PTVF) [17] is used to evaluate the soft error vulnerability of test-escaped defective cells. A lower PTVF means that the undetected defective cell can still functionally operate and can tolerate some soft errors.

The standard latch has the highest defect coverage; however it cannot tolerate any soft error and contains 3 susceptible nodes of Type-3, which is the worst case. STAHL has the highest defect coverage and the lowest PTVF among all hardened latches. This means that the proposed latch has high defect coverage in scan mode and has high soft error tolerance capability in function mode.

Table 3. Defect Coverage (DC) and PTVF

Latch	DC(%)	PTVF (%)
Standard	89.4	100.0
TMR	21.3	81.8
FERST [13]	63.5	79.7
HLR [14]	49.1	70.5
HiPeR [16]	50.5	71.5
ISEHL [15]	52.5	76.4
HLR-CG1 [14]	43.2	54.8
HLR-CG2 [14]	32.1	71.7
[21]	68.3	48.5
STAHL	83.3	5.7

C. Defect Coverage in Scan-Test

This experiment was conducted to demonstrate the testability of a STAHL-based scan cell in the context of a scan chain.

Here, a scan chain with three STAHL-based scan cells (see Fig. 6) was simulated in SPICE. Defects were injected one by one into the second scan cell (Scan Cell 2) of the scan chain. Similar to previous experiments, all possible open defects and short defects between internal nodes were injected. Here, however, all internal defects within the complete scan cell were considered and not just the defects within a single latch.

For each defect, the test procedure in Fig. 7 was simulated and the scan-out signal was observed. The test was considered to pass, if all response bits from Fa to Fe were correctly observed. For the scan chains based on the HiPeR latch and the Standard latch, only the bits from Fa to Fd were checked. This is because these chains did not support the fast capture feature.

Table 4 shows the test results for a scan chain based on the Standard latches, a scan chain based on the HiPeR latches and our STAHL-based scan chain. The Standard latch based scan cell shows a satisfactory defect coverage of 83%. The majority of undetected defects were opens and shorts that might degrade the performance or power consumption of the scan cell but were not detected during scan test.

Table 4. Defect Coverage in Scan-Test

Latch	#Defect	#Det.	#Undet.	DC (%)
Standard	244	202	42	83
HiPeR [16]	452	215	237	48
STAHL	950	747	203	79

As expected, the defect coverage of the HiPeR latch based scan cell is 48% lower. The STAHL-based scan cell achieves a defect coverage of 79%, which is similar to the non-hardened scan cell. We can therefore conclude that the STAHL-based scan infrastructure maintains its testability and at the same time provides soft error hardness during the functional operation of the design.

V. CONCLUSIONS

This paper has proposed a novel Scan-Test-Aware Hardened Latch design (STAHL). The proposed latch has two modes. In function mode, it can tolerate soft errors. In scan mode, most cell-internal manufacturing defects remain detectable. Simulation results have shown that its defect coverage is 83.3%, which is much higher than any existing state-of-the-art hardened latches and its PTVF is 5.7%, which means that undetected defects in STAHL have less influence on its soft error vulnerability.

ACKNOWLEDGMENT

This research was supported in part by JSPS Grant-in-Aid for Young Scientists 18K18026 and JSPS Grant-in-Aid for Scientific Research (B) 17H01716. Aibin Yan (abyan@mail.ustc.edu.cn) was supported by the National Natural Science Foundation of China (No.61604001), and Hui Xu was supported by the National Natural Science Foundation of China (No.61404001, No.61306046, No.61371025).

REFERENCES

[1] P. E. Dodd, et al, "Single-Event Upsets and Distributions in Radiation Hardened CMOS Flip-Flop Logic Chains," *IEEE Trans. on Nuclear Science*, vol. 58, no. 6, pp. 2695-2701, Dec. 2011.

[2] E. Ibeet, et al, "Impact of Scaling on Neutron-Induced Soft Error in SRAMs from a 250nm to a 22nm Design Rule," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1527-1538, Jul. 2010.

[3] R. Baumann, "Soft Errors in Advanced Computer Systems," *IEEE* Design & Test of Computers, vol. 22, no. 3, pp. 258-266, May-Jun. 2005.

[4] H. Zhang, et al, "Angular Effects of Heavy-Ion Strikes on Single-Event Upset Response of Flip-Flop Designs in 16nm Bulk FinFet Technology," *IEEE Trans. on Nuclear Science*, vol. 64, no. 1, pp. 491-496, Jan. 2017.

[5] H. Zhang, et al, "Effects of Threshold Voltage Variations on Single-Event Upset Response of Sequential Circuits at Advanced Technology Nodes," *IEEE Trans. on Nuclear Science*, vol. 64, no. 1, pp. 457-463, Jan. 2017.

[6] B. Gill, et al, "Comparison of Alpha-Particle and Neutron-Induced Combinational and Sequential Logic Error Rates at the 32 nm Technology Node," *Proc. IEEE Int'l Reliability Physics Symp.*, pp. 199-205, Jul. 2009.

[7] H. Cha, et al, "A Logic-Level Model for α-Particle Hits in CMOS Circuits," *Proc. IEEE Int'l Conf. Computer Design*, pp. 538-542, Oct. 1993.

[8] R. Baumann, "Radiation-Induced Soft Errors in Advanced Semiconductor Technologies," *IEEE Trans. on Device and Materials Reliability*, vol. 5, no. 3, pp. 305-316, Dec. 2005.

[9] T. Karnik, et al, "Characterization of Soft Errors Caused by Single Event Upsets in CMOS Processes," *IEEE Trans. on Dependable and Secure Computing*, vol. 1, no. 2, pp. 128-143, Apr. 2004.

[10] M. Nicolaidis, et al, "Low-Cost Highly-Robust Hardened Cells Using Blocking Feedback Transistors," Proc. *IEEE VLSI Test Sympo.*, pp. 371-376, May. 2008.

[11] Calin. T, et al, "Upset Tolerant Latch Based on Error Detection", *IEEE Trans. on Nuclear Science*, vol. 43, no. 6, pp. 2874-2878, Dec. 1996.

[12] M. Omana, et al, "Latch Susceptibility to Transient Faults and New Hardening Approach" *IEEE Trans. on Computers*, vol. 56, no. 9, pp. 1255-1268, Aug. 2007.

[13] M. Fazeli, et al, "Low Energy Single Event Upset/Single Event Transient-Tolerant Latch for Deep Submicron Technologies," *IET Computers Digital Techniques*, vol. 3, no. 3, pp. 289-303, May. 2009.

[14] H. Nan, et al, "High Performance, Low Cost, and Robust Soft Error Tolerant Latch Designs for Nanoscale CMOS Technology," *IEEE Trans. on Circuits and Systems I: Regular Papers,* vol. 59, no. 7, pp. 1445-1457, Jul. 2012.

[15] H. Liang, et al, "Design of a Radiation Hardened Latch for Low-Power Circuits",*Proc. IEEE Asian Test Sympo.,* pp. 19-24, Dec. 2014.

[16] M. Omana, et al, "High-performance robust latches," *IEEE Trans. on Computers*, vol. 59, no. 11, pp. 1455–1465, Nov. 2010.

[17] S. Holst, et al, "The Impact of Production Defects on the Soft-Error Tolerance of Hardened Latches," *IEEE 23rd European Test Sympo.,* May. 2018.

[18] L. Wang, et al, VLSI Test Principles and Architectures: Design for Testability, Morgan Kaufmann Publishers Inc., San Francisco, CA, USA, Jun. 2006.

[19] A. Goel, et al, "Low-Overhead Design of Soft-Error-Tolerant Scan Flip-Flops with Enhanced-Scan Capability," *IEEE Asia and South Pacific Conference on Design Automation*, Jan. 2006.

[20] Y. Lu, et al, "Design and Analysis of Single-Event Tolerant Slave Latches for Enhanced Scan Delay Testing," *IEEE Trans. On Device and Materials Reliability,* vol. 14, no. 1, pp. 333–343, Mar. 2014.

[21] C. Qi, et al, "Low Cost and Highly Reliable Radiation Hardened Latch Design in 65-nm CMOS Technology," Microelectron. Reliab., vol. 55, no. 6, pp. 863–872, May. 2015.

[22] Predictive Technology Model for Spice, http://ptm.asu.edu/