Si (100)-GaN/Si (111) low temperature wafer bonding process for 3D power supply on chip

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***Abstract*—In this paper, we describe the wafer bonding technology Si (100) substrate and GaN/Si (111) substrate using surface activated bonding at room temperature and the removal technique for Si (111) substrate underneath the GaN and buffer layers for 3D power-supply on chip.**

Keywords—Power-SoC; 3D IC; Wafer bonding technology

I. INTRODUCTION

The mainstream of the power supply is miniaturization [1]. The passive components such as inductor and capacitor occupy a larger part of the volume of the power supplies. The most promising approach to shrink the size of the passive components is increasing the switching frequency and this induces increase in loss caused by switching devices. The GaN power device is one of the promising candidates for high frequency switching applications [2]. However, the conventional PCB-based assembly technology increases the loss caused by the parasitic inductance resulting from the wiring at high frequency switching [3] (Fig. 1). As a result, the performance of the GaN power devices for high-frequency switching applications cannot be fully exploited. In such a situation, we previously proposed 3D power-SoC (Supply on Chip) [4] (Fig. 2). In the proposed 3D power-SoC, the GaN power devices are stacked with Si-LSI and passive devices. Thus, it can minimize the parasitic inductance by the wiring because the wiring length can be minimized. This enables high efficiency at high frequency [3]. Because bonding of

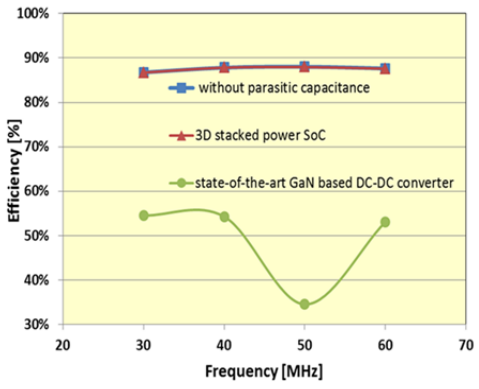


Fig. 1 Efficiency vs. switching frequency.

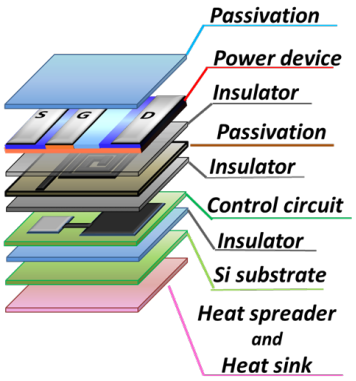


Fig. 2 3D power SoC [4].

The devices should be handled at a maximum temperature of 400 ° C or lower after the process is complete. Also, when the temperature is high, the difference in coefficient of thermal expansion between devices is a problem. Therefore, low temperature bonding technology is a key technology. The wafer bonding technology at low temperature has been reported [5]. However, the technology for stacking the GaN power devices and the Si devices at low temperature and subsequent processes have not been studied.

In this paper describes surface activated bonding technology for stacking GaN power devices and Si devices at low temperature in 3D Power-SoC.

II. FABRICATION PROCESS

The main steps of the fabrication process for bonding the Si (100) substrate and the GaN/Si (111) substrate are shown in Fig. 3. All processes are performed less than 300 °C. First, a SiO_2 film is deposited on a Si (100) wafer by using P-CVD (Plasma- Enhanced Chemical Vapor Deposition) (Fig. 3 (a)). Si-LSI was fabricated on this substrate. After the SiO_2 film was deposited, the SiO_2 layer is penalized by a CMP (Chemical Mechanical Polishing) process in order to obtain smaller surface roughness which is sufficient for wafer bonding process. Colloidal silica is used as the slurry. Deposition of SiO_2 and CMP process supposed planarization of wafer surface after metallization process. The surface roughness (Rq) of after the CMP process is less than 0.5 nm, which is sufficient for surface activated bonding technology.

Next, Al_2O_3 is deposited on both the SiO_2 film on Si (100) and GaN/Si (111) by ALD (Atomic Layer Deposition) (Fig. 3 (b)). The deposition temperature of ALD-Al_2O_3 is 300 °C. ALD-Al_2O_3 is suitable for passivation film of GaN devices and surface roughness of this film is less than 0.5 nm. The two wafers are bonded by surface activated bonding technology at room temperature [6]. Bonding interface is ALD-Al_2O_3 and ALD-Al_2O_3. Si-LSI and GaN power device are bonded face to face. The Si (111) wafer was removed by grinding, polishing, CMP and dry etching. Finally, the buffer layer under the GaN power device is removed by dry etching.

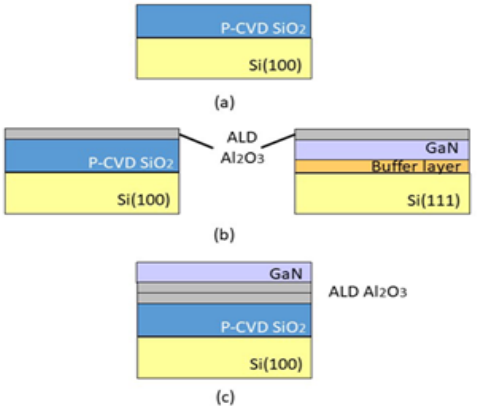


Fig. 3 Main steps of the fabrication process for bonding process

III. Results and Discussion

The AFM (Atomic Force Microscope) image on the surface after the ALD-Al_2O_3 deposition is shown in Fig. 4. The Rq was 0.19 nm, and this Rq is sufficient for the surface activated bonding technology.

A photograph after bonding is shown in Fig. 5. Cross sectional SEM photographs after wafer bonding and after removing Si (111) are shown in Figs. 6 (a) and (b). The bonding strength is sufficient for backend process, for example, polishing, grinding, and dicing process.

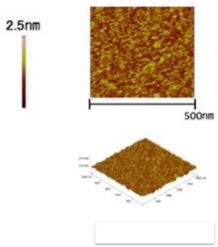


Fig. 4 AFM image after ALD-Al_2O_3 deposition.

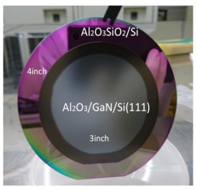
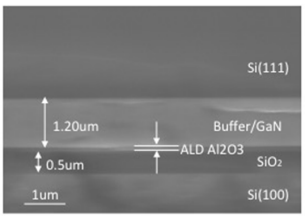
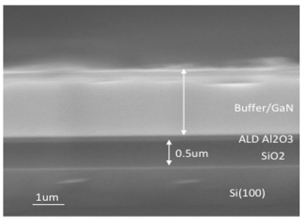


Fig. 5 Photograph after bonding wafer.



(a) After bonding



(b) After Si (111) removal

Figs. 6 Cross sectional SEM images.

IV. Conclusion

We have developed wafer bonding technology for Si (100) substrate and GaN/Si (111) substrate at room temperature using surface activated bonding. We also developed the removal technique for Si (111) substrate underneath the GaN and buffer layers.

Acknowledgment

I would like to thank Professor S. Shinkai at CMS (Center for Microelectronic System) of Kyushu Institute Technology for SEM observation.

Part of this research was supported by Grants-in-Aid for Scientific Research (18H04130).

Part of this research was conducted with the support of the Research Center for Biomedical Engineering.

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