

Novel Software Defined Power Supply Utilizing Power Supply on Chip

-Power supply which outputs the regulated output voltage by only connecting the load-

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«Power supply », «DC power supply», «Digital control», «High frequency power converter», «Software»

Abstract

In this paper, we propose a novel software defined power supply using the general purpose DSP (Digital Signal Processor) and its control algorithm based on power supply on chip. The proposed power supply can regulate the output voltage only loading a program into the DSP without adjusting the parameters and changing the external parts. Also, it can change the output voltage according to the state of the load by executive instruction from the load. The simulation results show that the transient response depends on the inductance, the capacitance and the internal resistance, and expects sub- μ s. at switching frequency of 30 MHz.

Introduction

Point of load converters(POLs) become one of the key parts in ICT (information and communication technology) systems and they are required high efficiency, high power density (smaller size), high speed response, and low cost. Recently, LSIs, which are key components of ICT systems, spend greater part of the power consumed in the ICT systems. Therefore, the supply voltage reduces to suppress the power consumption of the ICT systems, however consumption current increases. As a results, it is important to put POL as closest to LSIs(load) to avoid voltage drop, voltage fluctuation, and loss caused by wiring impedance [1]. Shrinking the size of the POLs is one of the effective ways to implement those near the LSIs.

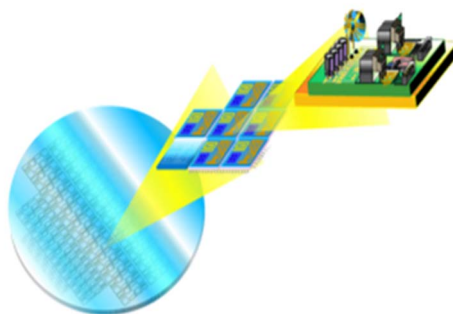


Fig.1 Power-SoC.

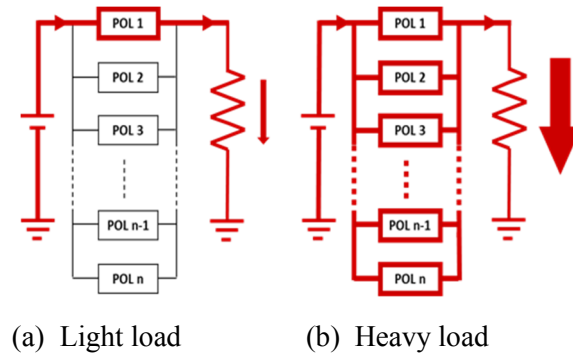


Fig. 2. Parallel-connected POL system [8-11].

A power SoC (power Supply on chip), which integrates Si-LSI (as a load), power devices, control circuits and passive devices such as capacitors and inductors is shown in Fig. 1, has been attracted attentions because it can ultimately miniaturize the POL [2-7]. The switching frequency of the power - SoC is required several tens of MHz to reduce the size of passive components and the traditional analog based PWM (pulse width modulation) control will face the problems. In such a situation, we previously propose a control technique, which is suitable for the power-SoC. The proposed control technique is utilizing parallel connected POLs shown in Fig. 2 [8-11]. This control technique only switches the number of working POLs according to the output voltage and does not change the duty ratio. This technique can realize high frequency switching and high efficiency operation over the wide load range.

Power SoC is fabricated using LSI and MEMS (Micro Electro Mechanical System) process and mass-produced. Thus, versatility becomes important. The analog based control technology does not have versatility because they require modification of external parts. Digital control technology is favorable because it is not necessary to change any external part. However, the PID (Proportional-Integral-Differential) control technology, which is widely used as the digital control, does not have versatility because it adjusts the parameters according to the load and/or applications. In addition, the power-SoC has been one of the promising candidate as power supplies for MCU (Micro Controller Unit) and RF power amplifier because it can be integrated with the load [3]. Power supply for such applications are required high versatility, various functions such as DVFS (Dynamic Voltage and Frequency Scaling) and envelope tracking.

In this paper, we propose a novel software defined power supply and its control algorithm without adjustment parameters. The proposed power supply can regulate the output voltage only load a program into the DSP without adjusting the parameters and changing external parts.

A SOFTWARE DEFINED POWER SUPPLY

The proposed software defined power supply consists of the general purpose DSP, AD (Analog Digital) converter and ROM (Read Only Memory) (Fig. 3). The proposed software defined power

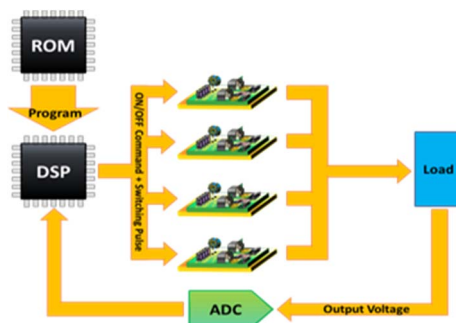


Fig. 3 The proposed software defined POL.

supply has two advantages. First, it can work only connecting “load” and DC-DC converters. Its control program is written in the ROM which is implemented in “load (ex. MCU)”. When it works, it loads a program into the DSP from the ROM which is originally implemented in the load. Therefore, it can work immediately when it is required to use. Second, its specification can be changed easily by rewriting three program codes such as “input voltage”, “output voltage”, and” switching frequency”. The software defined power supply with these two advantages enables high versatility. In addition, the proposed software defined POL reduces power consumption of the system because the changing the operating conditions such as the output voltage and the switching frequency according to the operating conditions of the load.

CONTROL ALGORITHM OF SOFTWARE DEFINED POWER SUPPLY

We propose the control algorithm of the software defined power supply based on the previously reported paper [8]. In this section, we explain the buck converter. Expression (1) shows output voltage conversion equation of the power-SoC used in buck converter mode.

$$V_{out} = DV_{in} - \frac{r}{N}I \quad (1)$$

D is the duty ratio, V_{in} is the input voltage, r is the internal resistance, N is the number of operating power-SoCs connected in parallel, and I is the output current. The load characteristics of our previously proposed control technique is shown in Fig. 3[8-11]. The output voltage is regulated by adjusting the number of operating power-SoCs(N) according to the load current without changing D.

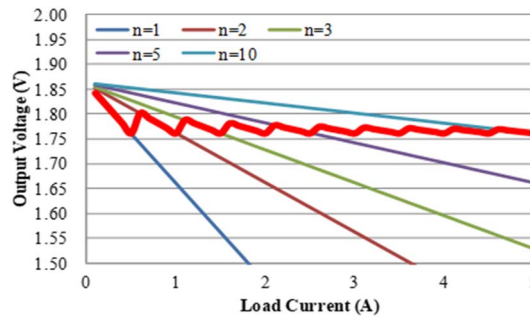


Fig. 3 Load characteristics[8-11].

Figure 4 illustrates dependence of the output voltage on the output current at each number of working power-SoCs. V_{set} is the target voltage, $V_{out(0)}$ is the output voltage when the output current is 0 A, and V_N is the hysteresis voltage. The slope and the voltage drop between the target voltage and the present output voltage are decided by number of working power-SoCs. From results of Fig. 3, we show flowchart of the proposed control algorithm based on the previously reported paper is shown in Fig. 5. [11]. First, the DSP reads the output voltage (V_{out}) from the AD converter. Secondly, the V_{out} is

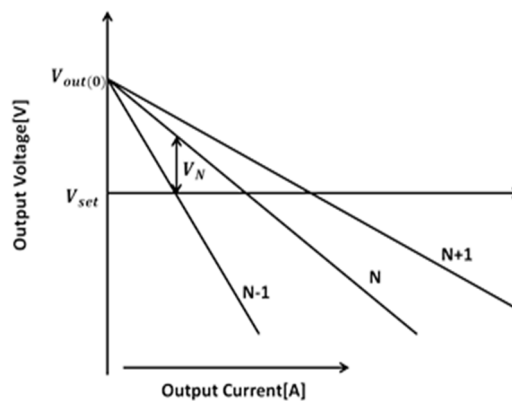


Fig. 4 Voltage-Current characteristics[11].

compared with V_{set} . The next step is considered the following two cases.

$$V_{out} < V_{set} \quad (2)$$

$$V_{set} + V_N < V_{out} \quad (3)$$

In the case of (2), the number of operating Power-SoCs increases according equation (4).

$$N_J = \frac{\Delta I}{I} = \frac{N(V_{set} - X)}{DV_{in} - V_{set}} \quad (4)$$

Finally, number of working POLs (N_{AJ}) is defined by the equation (5).

$$N_{AJ} = N + N_J \quad (5)$$

If V_{out} is represented by equation (3) or X equal to V_{set} , number of working POLs reduces as shown in Fig.5. Similarly, number of working POL switched according to the sudden change in load (-jump).

The proposed algorithm provides hysteresis (V_N) to avoid oscillation when it reduces the number of working POL. "One" POL is stopped according to equation (6).

$$V_{set} + V_N \cdot 2 > X \geq V_{set} + V_N \cdot 1 \quad (6)$$

Using equation (8), N_J is shown in equation (7).

$$N_J = \frac{X - V_{set}}{V_N} \quad (7)$$

Finally, the number of working POLs is represented by the equation (8).

$$N_{AJ} = N - N_J \quad (8)$$

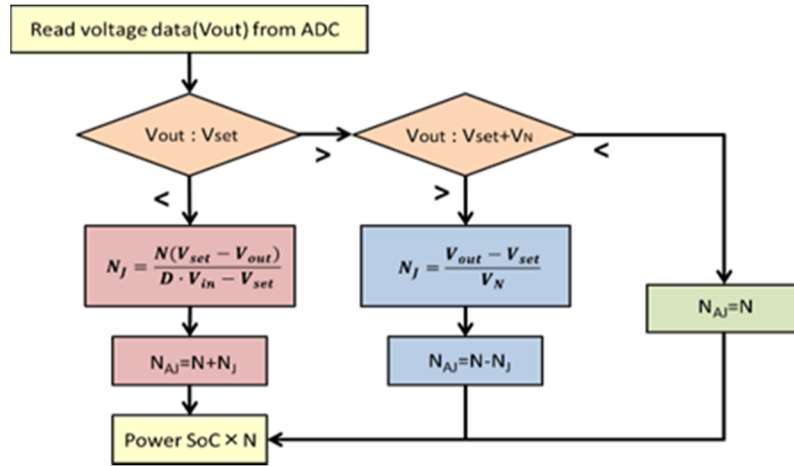
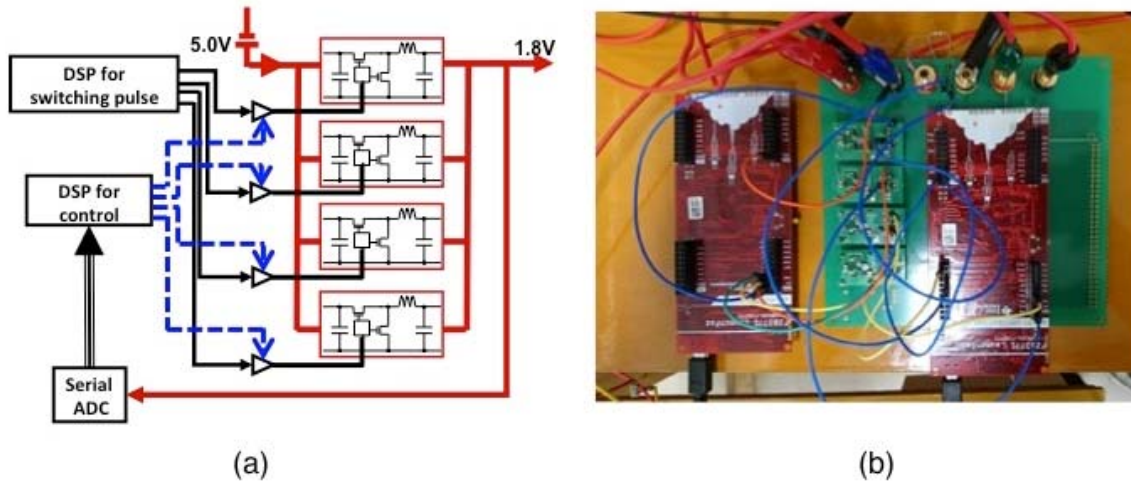


Fig. 5 Flowchart of the proposed algorithm[11].

EXPERIMENTAL SET UP

The block diagram of prototype software defined power supply and photograph of evaluation board are shown in Figs. 6 (a) and (b). Four parallel-connected buck converters with synchronous rectification is used.



Figs. 6 (a) block diagram (b) photograph of evaluation board

The main specifications and circuit parameters are listed in Table 1.

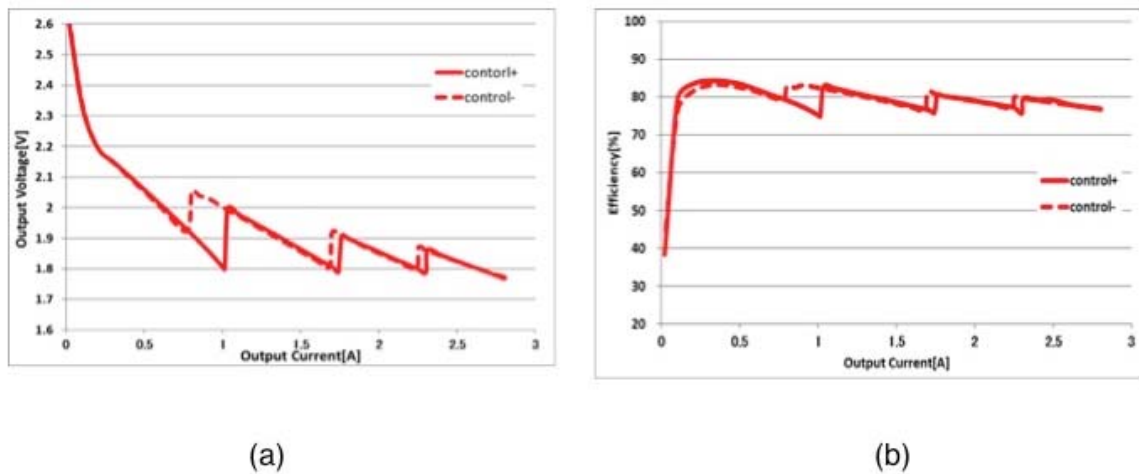
Table I: The main specifications and circuit parameters

V_{in}	Input voltage [V]	5
V_{out}	Output voltage [V]	1.8
f_s	Switching frequency [MHz]	1
C_{in}	Input capacitance [μF]	4.7
C_{out}	Output capacitance [μF]	4.7
L	Smoothing inductor [μH]	4.7
R	Internal resistance [Ω]	0.7

RESULTS AND DISCUSSION

Experimental results

Experimental results of the load and efficiency characteristics are shown in Figs. 7 (a) and (b), respectively. The proposed software defined power supply and control algorithm can easily output the target voltage by rewriting the values of the input voltage and output voltage in the program codes as shown in Figs. 7 (a). It can keep high efficiency over the wide load range as shown in Figs.7 (b) .



Figs. 7 (a) Load characteristics (b) Efficiency characteristic

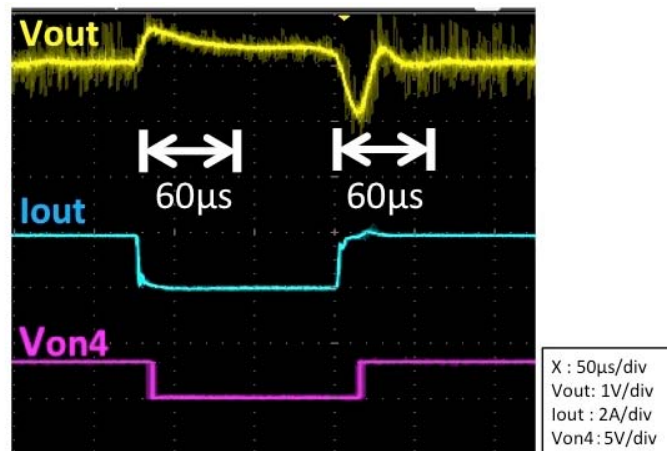


Fig. 8 Tangent response of the proposed software defined power supply.

Transient response of the proposed software defined power supply is shown in Fig. 8. V_{out} and I_{out} indicate the output voltage and the input voltage, respectively. The load current changes from 2.5 A to 0.5 A and from 0.5 A to 2.5 A. In these cases, number of working POLs is from 4 to 1 and from 1 to 4. V_{on4} indicates the control signal of a 4th POL. The signal is output quickly. The settling time is both 60 µs.

The transient response is represented by transfer function as shown in equation (11). We can obtain the settling time (T_s) through the step response of equation (11). Thus, the settling time is expressed by equation (13). v_o is the output voltage, i_o is the output current, v_i is the input voltage, D is the duty

ratio, L is the inductance, r_L is the equivalent series DC resistance of the inductor, C is the capacitance, and r_C is the equivalent series resistance of capacitor.

$$\left. \begin{array}{l} \Delta v_o(t) \\ \Delta i_o(t) \end{array} \right|_{\substack{\Delta V_i = 0 \\ \Delta D = 0}}$$

$$= r_L - \sqrt{(r_L - r_C)^2 + \left\{ \frac{C(r_L^2 + r_C^2) - 2L}{\alpha} \right\}^2} e^{-\frac{r_L + r_C}{2L}t} \sin \left\{ \frac{\alpha}{2LC}t + \tan^{-1} \frac{\alpha(r_L - r_C)}{C(r_L^2 + r_C^2) - 2L} \right\} \quad (11)$$

$$\alpha = \sqrt{4LC - C^2(r_L + r_C)^2} \quad (12)$$

$$T_s = -\frac{2L}{r_L + r_C} \ln \left(\frac{0.01r_L}{\sqrt{(r_L - r_C)^2 + \left\{ \frac{C(r_L^2 + r_C^2) - 2L}{\alpha} \right\}^2}} \right) \quad (13)$$

The settling time of $60 \mu s$ is obtained by equation (13) and this result is in good agreement with experimental results. The settling time depends on circuit parameters and characteristics of the passive components.

Figure 9 shows the transient response of the output voltage at the sudden duty change for the proposed power supply. This assumes DVS (Dynamic Voltage Scaling). The control algorithm of DVS is shown in Fig. 10. The number of connecting POLs is 4 and duty ratio changes from 50% to 33%. The output voltage stabilized in $55 \mu s$ after sudden the duty change.

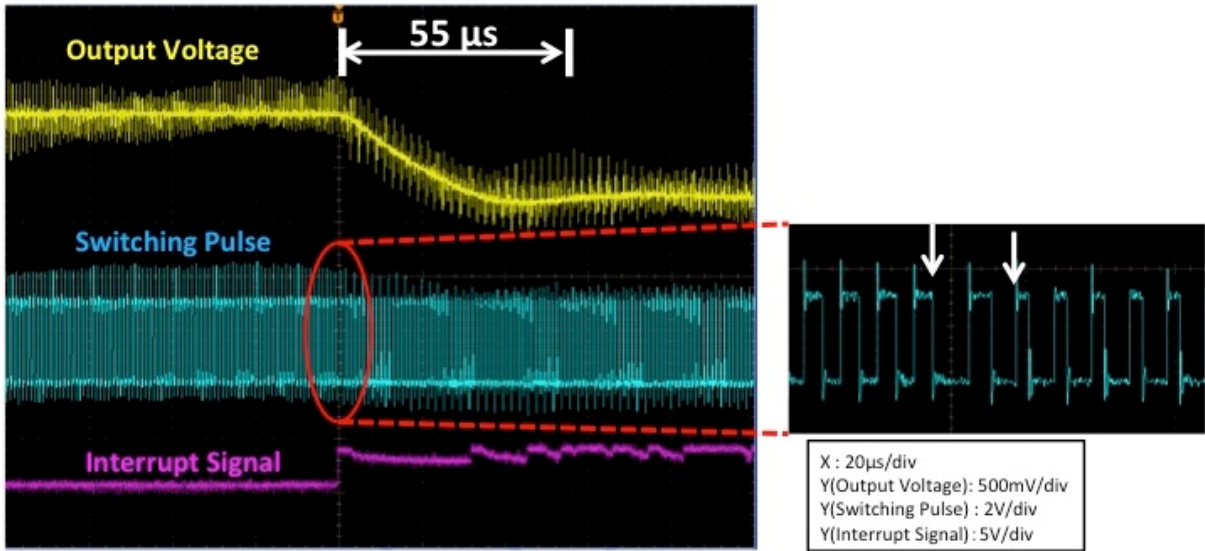


Fig. 9 Output voltage waveform of output voltage sudden change.

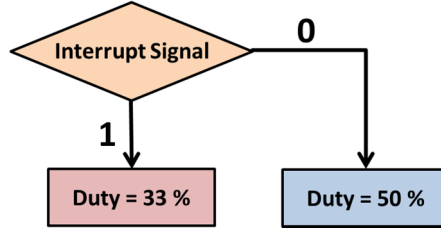


Fig. 10 Flow chart of DVS.

The transient response at DVS is represented by transfer function as shown in equation (14). We can obtain the settling time (T_s) through step response of equation (14). Thus, response time at DVS is expressed by equation (15).

$$\frac{\Delta v_o(t)}{\Delta D(t)} \Big|_{\substack{\Delta V_i = 0 \\ \Delta i_o = 0}} = V_i - V_i \sqrt{1 + \frac{C^2(r_L - r_C)^2}{\alpha^2}} e^{-\frac{r_L + r_C}{2L}t} \sin \left\{ \frac{\alpha}{2LC}t + \tan^{-1} \frac{\alpha}{C(r_L - r_C)} \right\} \quad (14)$$

$$T_s = -\frac{2L}{r_L + r_C} \ln \left(\frac{0.01}{\sqrt{1 + \frac{C^2(r_L - r_C)^2}{\alpha^2}}} \right) \quad (15)$$

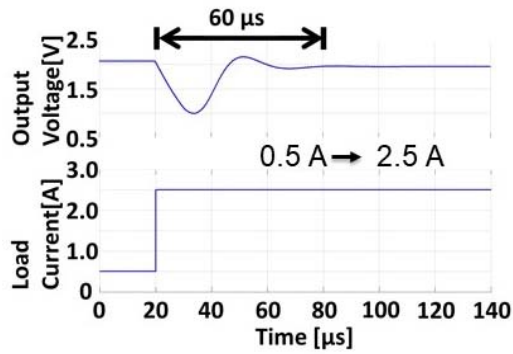
Settling time of 60 μ s is obtained by equation (15). The settling time depends on circuit parameters and characteristics of the passive components

Simulation results

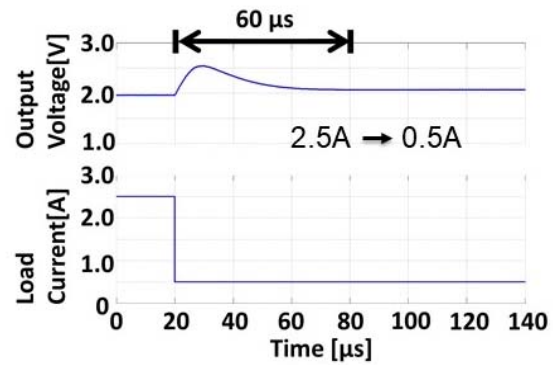
Table II shows the circuit parameters and system specifications for simulations. The circuit parameters used in 30 MHz are assuming 3D power SoC[12].

Table II: Circuits parameters and system specifications

		Switching Frequency	
		1 MHz	30 MHz
Inductor	Inductance [μ H]	4.7	0.038
	DCR [Ω]	0.24	0.38
Capacitor	Capacitance [μ F]	4.7	0.098
	ESR [Ω]	0.01	9.08×10^{-7}
On resistance [Ω]		0.07	0.07



(a)

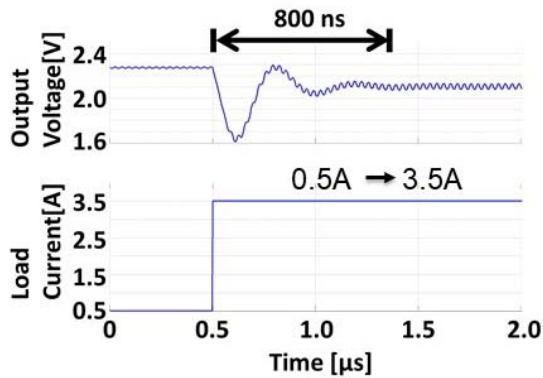


(b)

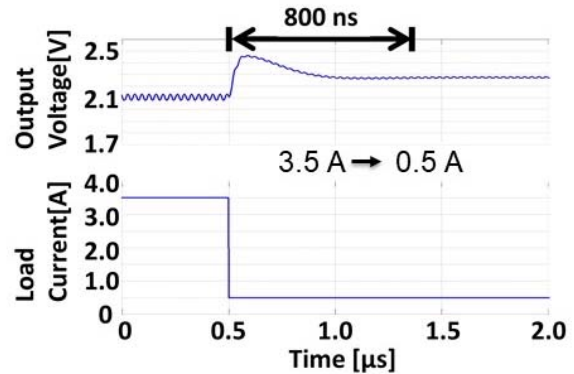
Figs.11 Simulated transient response of the proposed software defined power supply at 1 MHz.

(a) Load current changes from 0.5 A to 2.5 A.

(b) Load current changes from 2.5 A to 0.5 A



(a)



(b)

Figs.12 Simulated transient response of the proposed software defined power supply at 30 MHz.

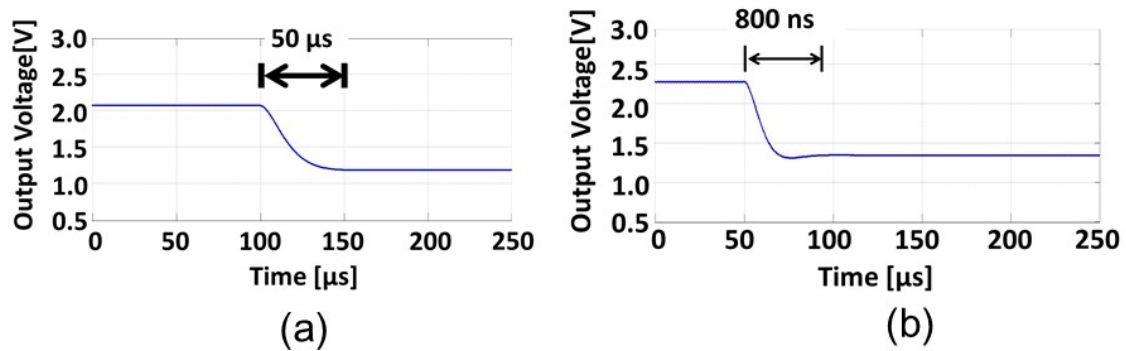
(a) Load current changes from 0.5 A to 3.5 A.

(b) Load current changes from 3.5 A to 0.5 A

Figures 11 (a) and (b) shows the simulation results of the transient response at 1 MHz. The simulation results are in good agreement with experimental results.

Figures 12 (a) and (b) shows the simulation results of the transient response at 30 MHz. The transient response is improved and that of sub μ s is achieved by increasing the switching frequency.

The simulated transient response of output voltage at the sudden duty change for the proposed power supply at (a) 1 MHz and (b) 30 MHz are shown in Figs 13 (a) and (b), respectively. The simulated transient response of the output voltage at the sudden duty change at 1 MHz is in good agreement with experimental results shown in Fig. 13. This is improved by increasing the switching frequency.



Figs. 13 Simulated transient response of output voltage at sudden duty change.
 (a) 1 MHz (b) 30 MHz

Conclusion

We proposed a new software defined power supply using the MUC or general purpose DSP and its control algorithm. The proposed power supply can regulate the output voltage only load a program into the DSP or MCU without adjusting the parameters and the external parts. Also, it can change the output voltage according to the state of the load by execution instruction from the load. In addition, the transient response is expected 900ns at 30MHz when duty sudden changes.

References

- [1] <http://tij/analog/jp/docs/analogsplash.tsp?contentID=46073>
- [2] S. Matsumoto, M. Mino, and T. Yachi.: Integration of a power supply part for a system on silicon, IEICE Trans. Communication and Computer Science, vol.80-A, No.2, pp.276-282.
- [3] K. Bharath, S. Venkatraman.: Power Delivery Design and Analysis of 14 nm Multicore Server CPUs with Integrated Voltage Regulators, 2016 IEEE 66th Electronic Components and Technology Conference (ECTC2016), pp.368-373.
- [4] I. Ranmuthu.: Challenged of integration of power supply on chip, International Workshop on Power Supply On Chip 2016(PwrSoc'16), Session 1-3.
- [5] R. Zou.: A 100 MHz IVR PMIC with On-silicon Magnetic Thin Film Inductors, International Workshop on Power Supply On Chip 2018(PwrSoc'18), Plenary session 4.
- [6] T. Phillips.: Delivering the Inner Power of SoCs: The Value of Fully Integrated Voltage Regulator, International Workshop on Power Supply On Chip 2018(PwrSoc'18), session 6-2.
- [7] P. Bezerra.: Towards the Integration of Voltage Regulators in Server Applications, International Workshop on Power Supply On Chip 2018(PwrSoc'18), session 7-1.
- [8] T. Yamamoto, J. Rikitake, S. Matsumoto, S. Abe, and T. Ninomiya.: A New Control Strategy for Power Supply on Chip Using Parallel Connected DC-DC Converters, Proc. The 10th IEEE International Conference on Power Electronics and Drive Systems (PEDS2012), pp.109-112,.
- [9] T. Yamamoto, S. Matsumoto, S. Abe.: A novel concept of digitally controlled multiple output POL for power supply on chip, The 36th International communication Energy Conference(INTELEC2014), PO-33.
- [10] S. Abe, S. Matsumoto, and T. Ninomiya.: A novel load regulation technique for power-SoC with parallel connected POLs, IEEJ Journal of Industry Application vol.4 No.6, pp.732- 737.
- [11] M. Higashida, S. Abe, and S. Matsumoto.: A concept of field programmable power supply array utilizing power supply on chip -- Fully digital controlled multiple input and output voltages POL--, 17th European Conference on Power Electronics and Applications (EPE 2015, ECCE Europe), LS1e.4.
- [12] K. Ono, K. Hiura, and S. Matsumoto,.: Design consideration of a 3D stacked power supply on chip, 2018 IEEE Electronic Components and Technology Conference, Session 27.7.