IEEJ Journal of Industry Applications
Vol.8 No.3 pp.480–487 DOI: 10.1541/ieejjia.8.480

Paper

A Condition-Monitoring Method of DC-Link Capacitors Used in a High-Power Three-Phase PWM Inverter with an Evaluation Circuit

Kazunori Hasegawa[*a)] Member, Shin-ichi Nishizawa[**] Non-member
Ichiro Omura[*] Member

(Manuscript received July 24, 2018, revised Oct. 15, 2018)

This paper presents a condition-monitoring method of dc-link capacitors used in a high-power three-phase PWM inverter with an evaluation circuit intended for ageing tests. Although its power rating is 1/25 of the inverter, the evaluation circuit provides the equivalent ripple current waveform and dc-bias voltage to the high-power inverter. The monitoring method independently extracts the capacitance and ESR of the dc-link capacitor, where the fast Fourier transform is introduced to the ripple current waveform and the dc-link voltage of the evaluation circuit. Experimental results verify that the monitoring method obtains both the ESR and capacitance changes of a capacitor under test.

Keywords: DC-link capacitors, three-phase inverters, condition monitoring, equivalent series resistance, capacitance

1. Introduction

DC-link capacitors including electrolytic capacitors, film capacitors, and ceramic capacitors in power electronic converters are a major constraint on the improvement of power density as well as of reliability [(1)–(3)]. They usually have a shorter lifetime than the other components in power electronic converters. Reference (4) describes that capacitors were chosen by 18% of fragile components responsible for converter failure by a survey of reliability in power electronic converters. Many researchers and engineers have been working on reliability-related issues including condition monitoring [(5)–(9)], failure analysis, and ageing test [(10)–(12)].

Degradation of capacitors usually progresses with an increase in equivalent-series resistance (ESR) and a decrease in capacitance. Hence, monitoring these parameters plays an important role in estimating health condition of capacitors [(5)–(9)].

Accelerated ageing tests are effective in estimating lifetimes and in analyzing failure mechanisms of capacitors [(10)–(12)]. For example, reference (11) carried out an accelerated ageing test of metalized film capacitors under high ripple currents provided by a resonant inverter, which presents an ageing law that indicates ESR and capacitance evolution of the capacitors. The authors of this paper investigated the relation between the dc-bias voltage and degradation of aluminum electrolytic capacitors by an accelerated ageing test, which has revealed that either ESR or capacitance is not always a unique indicator of the degradation of the capacitors [(12)].

On the other hand, the so-called "ripple current tester" is developed, which supplies a sinusoidal ripple current and a dc-bias voltage into a capacitor under test [(13)]. The ripple current tester is designed for ageing tests, applications of which includes capacitor quality evaluation and quality assurance [(13)].

In general, however, characteristics of the capacitors are evaluated by a single sinusoidal current [(7)(11)(13)]. Actual ripple current generated by the converter contains multiple frequency components [(14)], so that characteristics of the capacitor cannot be exactly evaluated. For example, the authors have revealed that the power loss with the square-wave current injection cannot be estimated only by the root-mean-square (RMS) value of the capacitor current [(15)].

The authors have proposed an evaluation circuit for testing dc-link capacitors used in a full-scale high-power three-phase inverter [(16)(17)]. Although the power rating of the evaluation circuit is smaller than that of the full-scale inverter by a factor of ten, the circuit produces the actual ripple current waveform and dc bias voltage that are equivalent to the full-scale inverter.

This paper presents a condition-monitoring method of dc-link capacitors used in a high-power three-phase pulse-width modulated (PWM) inverter intended for ageing tests, where the evaluation circuit consisting of a low-voltage inverter is used. The monitoring method is characterized by extracting both the ESR and capacitance of the dc-link capacitor. In addition, this paper discusses the possible power rating of the low-voltage inverter by analyzing the relation between the dc-link voltage of the low-voltage inverter and the ripple current waveform.

2. Evaluation Circuit for DC-Link Capacitors

2.1 Basic Circuit Configuration The most effective and simplest method to test dc-link capacitors is measuring

a) Correspondence to: Kazunori Hasegawa. E-mail: hasegawa@life.kyutech.ac.jp
* Kyushu Institute of Technology
2-4, Hibikino, Wakamatsu-ku, Kitakyushu, Fukuoka 808-0196, Japan
** Kyushu University
6-1, Kasuga-koen, Kasuga, Fukuoka 816-8580, Japan

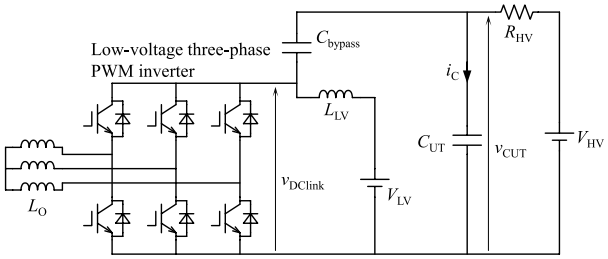
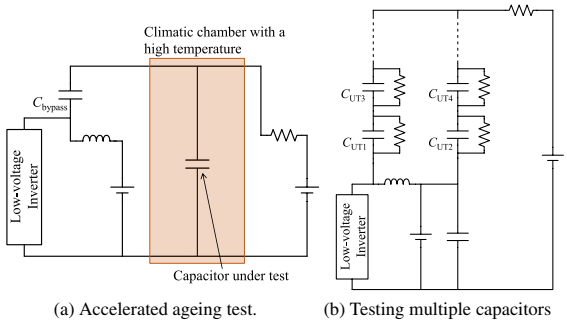


Fig. 1. Evaluation circuit for dc-link capacitors



(a) Accelerated ageing test. (b) Testing multiple capacitors

Fig. 2. Applications of the evaluation circuit

their characteristics with an existing converter in operation. This method, however, brings a high cost.

Figure 1 shows an evaluation circuit that employs a small-power-rating low-voltage three-phase inverter [16][17]. The low-voltage inverter is used for producing the ripple current, while the high-voltage dc supply provides a dc-bias voltage into a capacitor under test, C_{UT}. The bypassing capacitor C_{bypass} compensates the voltage deference between the dc-link voltage of the inverter and the voltage across the capacitor under test, where the ripple current flows. The choke inductor L_{LV} and resistor R_{HV} block the ripple current, through which only dc current flows. Hence, their impedances should be much larger than those of capacitors C_{UT} and C_{bypass} [14]. Note that the inductor and the two capacitors do not result in oscillation in practice [17].

The current rating of the low-voltage inverter is full-scale, while voltage rating is downscale. Therefore, the circuit operates as a full-scale voltage-rating and full-scale current-rating inverter from the viewpoint of the dc bias voltage and ripple current although the power rating of the low-voltage inverter is greatly smaller than that of the full-scale inverter. This concept is similar to the circuits proposed in (7) and (11) in terms of the combination of a ripple current generator and a dc voltage source, whereas it produces the same current waveform as that generated by the inverter.

2.2 Examples of Applications Figure 2 illustrate examples of applications of the evaluation circuit. Figure 2(a) aims for an accelerated ageing test of a capacitor that is placed on a climatic chamber with a high temperature. The evaluation circuit is also applicable to testing multiple capacitors as shown in Fig. 2(b), in which the bypass capacitor is replaced by capacitors under test. In other words, the circuit can be used with confirming variation between capacitors under test. The capacitors under test on the right side in Fig. 2(b) is connected to the positive terminal of V_{LV} so as to make all the capacitor voltage uniform.

2.3 Basic Implementation of Ageing Tests Figure 3 shows a basic implementation of the ageing test for which this paper aims. Since the degradation of the capacitor is accompanied by an increase in ESR and a decrease in capacitance, it is desirable for the evaluation circuit to have a monitoring function of these two parameters. The following section provides a monitoring method of both the ESR and capacitance with the evaluation circuit in operation.

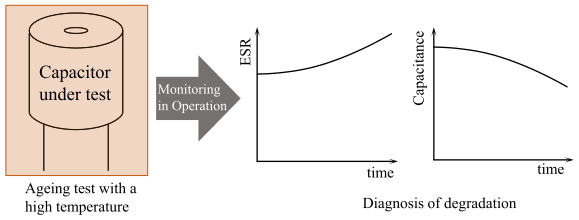


Fig. 3. Basic implementation of ageing test

3. Condition Monitoring Method

3.1 How to Extract ESR and Capacitance Since the ripple current i_{CUT} consists of multiple frequency components, it is given by

$$i_{CUT} = \sum_{k=1}^{n} I_{CUT}(\omega_k) \sin(\omega_k t + \varphi_k) \cdots\cdots\cdots\cdots\cdots (1)$$

where $I_{CUT}(\omega_k)$ and ϕ_k are the amplitude and initial phase angle for each frequency, respectively. Figure 4 shows an equivalent circuit of the capacitor under test for this analysis, where R_S is the ESR of the capacitor. The voltage across the capacitor under test is given by

$$\begin{aligned} v_{CUT} &= \frac{1}{C}\int i_{CUT}dt + R_S i_{CUT} \\ &= \sum_{k=1}^{n} I_{CUT}(\omega_k)\left\{-\frac{1}{\omega_k C}\cos(\omega_k t + \varphi_k)\right. \\ &\quad \left. + R_S \sin(\omega_k t + \varphi_k)\right\} \cdots\cdots\cdots\cdots\cdots\cdots (2) \end{aligned}$$

From Eq. (2), the amplitude of v_{CUT} at each frequency is given by

$$V_{CUT}(\omega_k) = I_{CUT}(\omega_k)\sqrt{\left(\frac{1}{\omega_k C}\right)^2 + R_S^2} \cdots\cdots\cdots\cdots (3)$$

Dividing (3) by $I_{CUT}(\omega_k)$ gives the impedance of the capacitor at each frequency as follows:

$$Z_{CUT}(\omega_k) = \frac{V_{CUT}(\omega_k)}{I_{CUT}(\omega_k)} = \sqrt{\left(\frac{1}{\omega_k C}\right)^2 + R_S^2} \cdots\cdots\cdots (4)$$

Equations (4) suggest that the capacitance and ESR are independently calculated if impedances at different frequencies are obtained. Multiple frequency components of the ripple current help calculate the capacitance and ESR.

Figure 5 shows a block diagram of ESR and capacitance

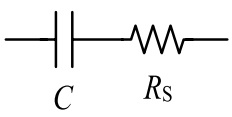


Fig. 4. Equivalent circuit of the capacitor for analysis

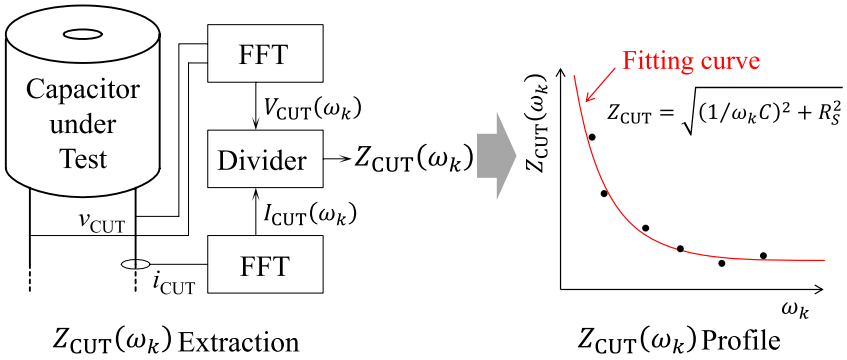
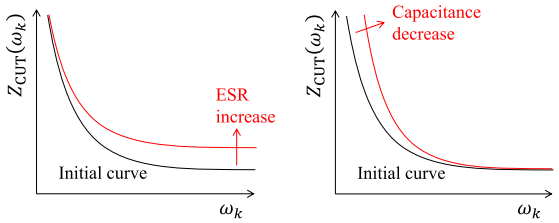
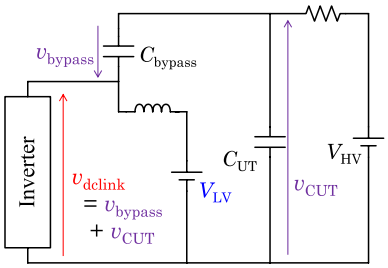


Fig. 5. How to extract ESR and capacitance from the actual ripple current and voltage

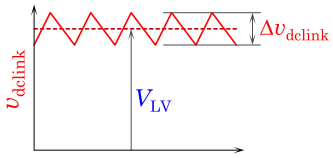


(a) ESR increase. (b) Capacitance decrease

Fig. 6. How to monitor ESR and capacitance from the variation of the fitting curve



(a) Positive direction of the voltages.



(b) Ripple component appearing on the dc link.

Fig. 7. Relation between dc-link voltage and capacitor voltages

extraction, which introduces the fast Fourier transform (FFT) that obtains $V_{CUT}(\omega_k)$ and $I_{CUT}(\omega_k)$. Dividing $V_{CUT}(\omega_k)$ by $I_{CUT}(\omega_k)$ yields the impedance at each frequency, $Z_{CUT}(\omega_k)$. One can plot an impedance profile of $Z_{CUT}(\omega_k)$ and draw a fitting curve by the least squares method, which indicates both the ESR and capacitance.

Figure 6 illustrates how to monitor the ESR and capacitance from the variation of the fitting curve, in which the increase in the ESR results in a rise in the fitting curve in a high-frequency region, whereas the decrease in the capacitance raises the curve in a low-frequency region. This variation can be utilized for the implementation of the ageing test shown in Fig. 2.

3.2 Capacitor Voltage Monitoring from DC-Link Voltage A major concern to carry out the monitoring method is to measure the ripple component of the capacitor voltage because the voltage contains a much larger amount of dc-bias voltage than the ripple component.

Figure 7 shows the relation between the dc-link voltage of the low-voltage inverter, v_{dclink}, and the voltages across the bypassing capacitor, v_{bypass}, and that across the capacitor under test, v_{CUT}. The dc-link voltage v_{dclink} is given by

$$v_{dclink} = v_{bypass} + v_{CUT} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (5)$$

The peak-to-peak amplitude of the ripple component of the dc-link voltage, Δv_{dclink}, is also given by

$$\Delta v_{dclink} = \Delta v_{bypass} + \Delta v_{CUT} \cdots\cdots\cdots\cdots\cdots\cdots\cdots (6)$$

where Δv_{bypass} and Δv_{CUT} are peak-to-peak amplitudes of the ripple component of v_{bypass} and v_{CUT}, respectively. Hence, one can obtain the ripple component of the capacitor voltage by means of measuring the dc-link voltage. From equation (2), the ripple ratio of v_{dclink}, r_{dclink} is given by

$$\begin{aligned} r_{dclink} &= \frac{\frac{1}{2}\Delta v_{dclink}}{V_{LV}} = \frac{\frac{1}{2}\Delta v_{bypass} + \frac{1}{2}\Delta v_{CUT}}{V_{LV}} \\ &= \frac{\frac{1}{2}\Delta v_{bypass} + \frac{1}{2}\Delta v_{CUT}}{V_{HV}} \times \frac{V_{HV}}{V_{LV}} \\ &= \left(r_{bypass} + r_{CUT}\right) \times n \cdots\cdots\cdots\cdots\cdots\cdots (7) \end{aligned}$$

where r_{bypass} and r_{CUT} are ripple ratios of v_{bypass} and v_{CUT} with respect to V_{HV}, respectively, and n corresponds to the ratio between voltage ratings of the full-scale inverter and the small inverter. Note that the ripple ratio is defined as the ratio between the peak value of the ripple component, i.e., half the peak-to-peak amplitude, and its corresponding dc component, so that Equations (7) include a coefficient of 1/2. Equations (7) suggest that the ripple ratio of the dc-link voltage is multiplied by n, so that the dc-link voltage has a large amount of ripple ratio even though the two capacitors contain a small amount of ripple component with respect to their dc-bias voltages. This improves the voltage resolution of the ripple amplitude of the capacitor under test. For example, for V_{HV} = 1000 V and V_{LV} = 100 V, a 100-V class voltage sensor is available although the voltage across the capacitor under test is 1000 V.

Although this method obtains the sum of impedances of the two capacitors C_{bypass} and C_{UT}, it can trace the variation of the ESR and capacitance of the capacitor under test, C_{UT}.

As for the accelerated test shown in Fig. 2(a), only the C_{UT} degrades due to the high temperature, so that the variation results only from the C_{UT}. When the evaluation circuit tests multiple capacitors shown in Fig. 2(b), the method obtains some of the impedances of all the capacitor under test.

4. Effect of Ripple Voltage to Current Waveform

The low-voltage inverter is forced to have a large ripple amplitude of the dc-link voltage, which is a constraint on reducing the power rating of the inverter. This section provides an intensive discussion on the effect of the ripple amplitude to the ripple current waveform.

4.1 Relation between DC-link Voltage and Ripple Current The ripple current waveform is synthesized by the output current and pulse pattern of the three-phase inverter. The dc-link voltage of the inverter does not have an influence on the ripple current waveform unless it affects the output current. In general, however, the output current of voltage-source converters depends on the dc-link voltage and the load of the inverter. Figure 8 shows the three-phase inverter indicating the relation between the ripple amplitude and the output current, in which an inductive load is connected. The ripple component, i.e., ac component, of the dc-link voltage is expressed as

$$\tilde{v}_{dclink} = \frac{1}{2}\Delta v_{dclink} \cdot \sin \omega_R t \cdots\cdots\cdots\cdots\cdots\cdots (8)$$

where $\tilde{v}_{dclink}$ is assumed to be a sinusoidal waveform with an angular frequency of ω_{R}. The line-to-neutral voltage of the inverter, v_{u} is given by

$$v_u = \frac{V_{dclink} + \tilde{v}_{dclink}}{2\sqrt{2}} \cdot m \cdot \sin \omega t \cdots\cdots\cdots\cdots\cdots\cdots (9)$$

where m is the modulation index of the inverter. The output current i_{O} is calculated by the following equations:

$$\begin{aligned} i_O &= \frac{1}{L_O}\int v_u dt = \frac{1}{L_O}\int \frac{V_{dclink} + \tilde{v}_{dclink}}{2\sqrt{2}} \cdot m \cdot \sin \omega t dt \\ &= \frac{V_{dclink} \cdot m}{2\sqrt{2}L_O}\int \sin \omega t dt + \frac{m}{2\sqrt{2}L_O}\int \tilde{v}_{dclink} \cdot \sin \omega t dt \\ &= -\frac{m \cdot V_{dclink}}{2\sqrt{2}\omega L_O}\cos \omega t + \frac{m}{2\sqrt{2}L_O}\int \tilde{v}_{dclink} \cdot \sin \omega t dt \end{aligned}$$
$$\cdots\cdots\cdots\cdots\cdots\cdots (10)$$

where ω is the output angular frequency. The output current is divided into the following equations:

$$i_{\mathrm{OO}} = -\frac{m \cdot V_{dclink}}{2\sqrt{2}\omega L_O}\cos \omega t \cdots\cdots\cdots\cdots\cdots\cdots (11)$$

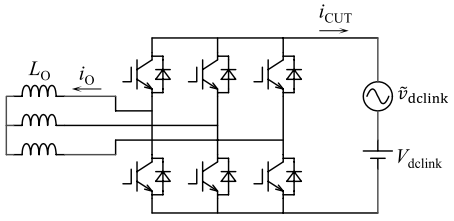


Fig. 8. Three-phase inverter that indicates the relation between the ripple amplitude of the dc-link voltage, $\tilde{v}_{dclink}$, and the ripple current flowing out of the inverter, i_{CUT}

$$i_{\mathrm{OR}} = \frac{m}{2\sqrt{2}L_{\mathrm{O}}}\int \tilde{v}_{dclink} \cdot \sin \omega t dt \cdots\cdots\cdots\cdots\cdots (12)$$

where i_{OO} is the output-frequency component, and i_{OR} is the component affected by the ripple amplitude. Substituting (8) into (12) gives

$$\begin{aligned} i_{\mathrm{OR}} &= \frac{m \cdot \Delta v_{dclink}}{4\sqrt{2}L_{\mathrm{O}}}\int \sin \omega_R t \cdot \sin \omega t dt \\ &= \frac{m \cdot \Delta v_{dclink}}{8\sqrt{2}L_{\mathrm{O}}}\int \{\cos(\omega_R - \omega)t - \cos(\omega_R + \omega)t\} dt \\ &= \frac{m \cdot \Delta v_{dclink}}{8\sqrt{2}L_{\mathrm{O}}}\left\{\frac{1}{\omega_R - \omega}\sin(\omega_R - \omega)t - \frac{1}{\omega_R + \omega}\sin(\omega_R + \omega)t\right\} \end{aligned}$$
$$\cdots\cdots\cdots\cdots\cdots\cdots (13)$$

The amplitudes of i_{OO} and i_{OR} are given as follows:

$$|i_{\mathrm{OO}}| = \frac{m \cdot V_{dclink}}{2\sqrt{2}\omega L_O} \cdots\cdots\cdots\cdots\cdots\cdots (14)$$

$$\begin{aligned} |i_{\mathrm{OR}}| &= \frac{m \cdot \Delta v_{dclink}}{8\sqrt{2}L_{\mathrm{O}}}\left\{\frac{1}{\omega_R - \omega} + \frac{1}{\omega_R + \omega}\right\} \\ &= \frac{m \cdot \Delta v_{dclink}}{4\sqrt{2}L_{\mathrm{O}}} \cdot \frac{\omega_R}{\omega_R^2 - \omega^2} \end{aligned} \cdots\cdots\cdots\cdots\cdots\cdots (15)$$

Equations (7), (14) and (15) yield the ratio of the component affected by the ripple amplitude with respect to the output-frequency component as follows:

$$\frac{|i_{\mathrm{OR}}|}{|i_{\mathrm{OO}}|} = \frac{\Delta v_{dclink}}{2V_{dclink}} \cdot \frac{\omega_R \omega}{\omega_R^2 - \omega^2} = r_{dclink} \times \frac{\omega_R \omega}{\omega_R^2 - \omega^2}$$
$$\cdots\cdots\cdots\cdots\cdots\cdots (16)$$

Figure 9 shows the ratio of the component obtained by equation (16), in which the output frequency is 50 Hz. In general, a switching frequency is much larger than an output frequency of inverters, i.e., $\omega_R \gg \omega$. Therefore, Equation (16) gets a greatly small value even though the ripple amplitude gets as large as the nominal dc-link voltage. As a result, the ripple amplitude has no net effect to the output current waveform as well as the ripple current flowing into the capacitor under test, unless it exceeds the nominal dc-link voltage as discussed in the following subsection.

4.2 Allowable Ripple Ratio In case the ripple amplitude of the dc-link voltage exceeds the nominal dc-link voltage, the dc-link voltage falls below 0 V, which results in a forward voltage to diodes. Hence, diodes keep turning on even though turn-on signals are applied to IGBTs. This changes

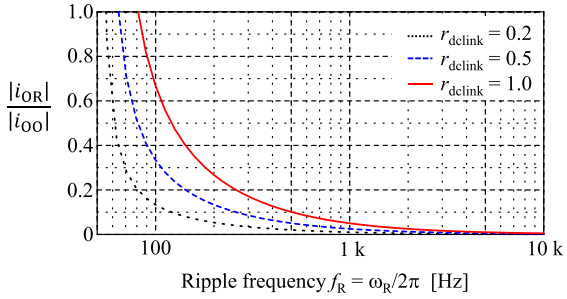


Fig. 9. Ratio of the component affected by the ripple amplitude with respect to the output-frequency component

the pulse pattern of the ripple current. Thus, the ripple ratio of the dc-link voltage, r_{dclink} has to be less than unity in order not to make the dc-link voltage negative as follows:

$$r_{dclink} \leq 1 \cdots\cdots (17)$$

Substituting (17) into (7) gives

$$r_{bypass} + r_{CUT} \leq \frac{1}{n} \cdots\cdots (18)$$

Equation (18) suggests that ripple ratios of C_{bypass} and C_{UT} determine the lower limit of the power rating of the low-voltage inverter.

5. Experiment

5.1 Circuit Configuration and Parameters Table 1 summarizes the ratings and circuit parameters of the experimental circuit. Although the power rating of the inverter is 2.8 kVA that is 1/25 of that of the full-inverter, the circuit acts as a 69-kVA full-scale inverter. Sinusoidal PWM is applied to the low-voltage inverter with a unity modulation index. The capacitor under test C_{UT} employs metalized polypropylene capacitors. The inverter drives only reactive power in this experiment. The ripple current waveform somewhat changes according to the power factor of the output power but always contains multiple frequency components. Thus, the proposed method is effective even though the power factor changes.

5.2 Conditions to Present Capacitance and ESR Changes Reference (10) describes that degradation of film capacitors near the end of their lifetime results in a decrease in capacitance by around 10% and a significant increase in ESR by a factor of 10 to 100. Thus, this paper introduces four conditions corresponding to this result as follows:

1) Condition A: $C_{\mathrm{UT}} = 360\,\mu$F.
2) Condition B: $C_{\mathrm{UT}} = 360\,\mu$F with an intentionally-connected series resistance of 0.1 Ω, which shows the effect of an increase in ESR.
3) Condition C: $C_{\mathrm{UT}} = 320\,\mu$F, which presents the effect of a decrease in capacitance by 11%.
4) Condition D: $C_{\mathrm{UT}} = 320\,\mu$F with a series resistance of 0.1 Ω.

The capacitor under test used for the experiment has a typical ESR of 3.4 mΩ, so that the series resistance is 30 times as large as the typical ESR.

Table 1. Ratings and circuit parameters of the evaluation circuit used in experiment

System Power rating	P	69 kVA
Power rating of the inverter	P_{inv}	2.8 kVA
AC current rating	I_{O}	54 A
AC voltage rating	V_{O}	29 V
Low-voltage dc source	V_{LV}	48 V
High-voltage dc source	V_{HV}	1200 V
Load inductor	L_{O}	1 mH
Carrier frequency	f_{SW}	3 kHz
Output frequency	f_{O}	50 Hz
High-voltage choke resistor	R_{HV}	1 kΩ
Low-voltage choke inductor	L_{LV}	4 mH
Capacitors under test	C_{UT}	320 or 360 μF
Unit capacitance constant of the capacitors under test [18]	H_{CUT}	3.3 ms (320 μF) 3.8 ms (360 μF)
Bypassing capacitor	C_{bypass}	320 μF

5.3 Results and Discussions Figure 10 shows time-domain waveforms of the ripple current, i_{CUT}. All the waveforms were almost the same as expected. Figure 11 shows the FFT results of the ripple current. Figure 12 shows experimental waveforms of the dc-link voltage, where the ripple amplitude of the voltage increased when the capacitance was reduced as well as the ESR was increased. Since all the waveforms had the ripple ratio r_{dclink} less than unity, there was a room for reducing the low-voltage source V_{LV}, i.e., making the power rating or the inverter smaller.

Figure 13 shows experimental waveforms of the voltage across the capacitor under test. All the waveforms stayed at 1200 V that were equal to V_{HV}.

Figure 14 shows impedance profiles of the capacitor against each frequency component along with fitting curves. The impedance profiles are obtained from FFT results of the capacitor current shown in Fig. 11 and those of the dc-link voltage shown in Fig. 12. The fitting curves are modeled by Equation (4). Note that the impedance profile shows the sum of impedances of C_{bypass} and C_{UT}. Hence, C_{UT} is calculated from the sum of impedance under a condition of $C_{\mathrm{bypass}} = 320\,\mu$F. In Fig. 14(a), the capacitance was almost the same as the series-connected capacitance of C_{bypass} and C_{UT}, and the ESR was 0 Ω. In Fig. 14(b), the fitting curve has a larger value in a high-frequency region, which indicates that the ESR increased to 0.1 Ω that was the same as

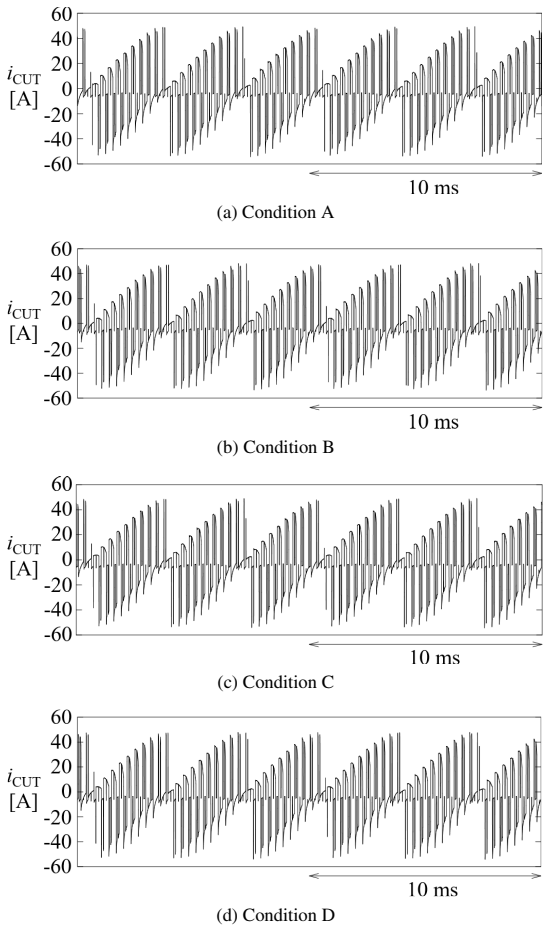


Fig. 10. Experimental waveforms of the ripple current i_{CUT}

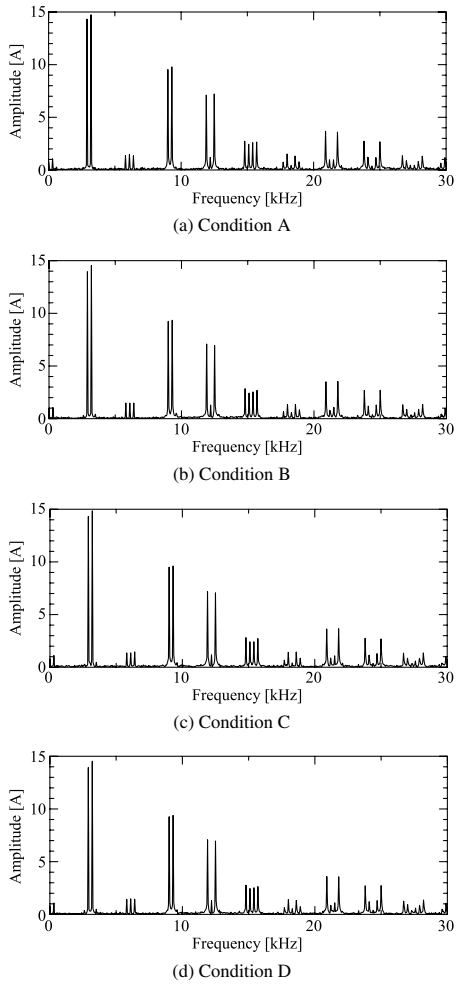


Fig. 11. FFT results of the ripple current i_{CUT}

the intentionally-connected resistance. Note that the series resistance is larger than the reactance of C_{UT} in a range more than 3 kHz, which makes an error in the capacitance. For this reason, C_{UT} changed to 333 μF.

In Fig. 14(c), the impedance in a low-frequency region were slightly larger than that of Fig. 13(a) due to a smaller capacitance. In Fig. 14(d), the ESR increased to 0.1 Ω because of the intentionally-connected series resistance. These results confirmed that the monitoring method well observed both the ESR and capacitance changes.

The reason why the fitting curves in Figs. 14(a) and (c) were somewhat lower than the FFT results in a range over 10 kHz is that the ripple voltage in the range is significantly small because the capacitor has a greatly small impedance. The voltage sensor used in this experiment would not have enough resolution to sense such a small voltage. If the fitting curves further approached the FFT results, the ESR would become an imaginary value. On the other hand, those in Figs. 14(b) and (d) well agreed with the FFT results even in the range because the existence of the intentionally-connected resistance increased the ripple voltage.

6. Conclusion

This paper has presented a condition monitoring method of dc-link capacitors used in a high-power three-phase PWM inverter with an evaluation circuit. Introduction of the FFT to the ripple current and voltage of the capacitor makes it possible to extract both the ESR and capacitance. In addition, this paper has investigated the possible power rating of the

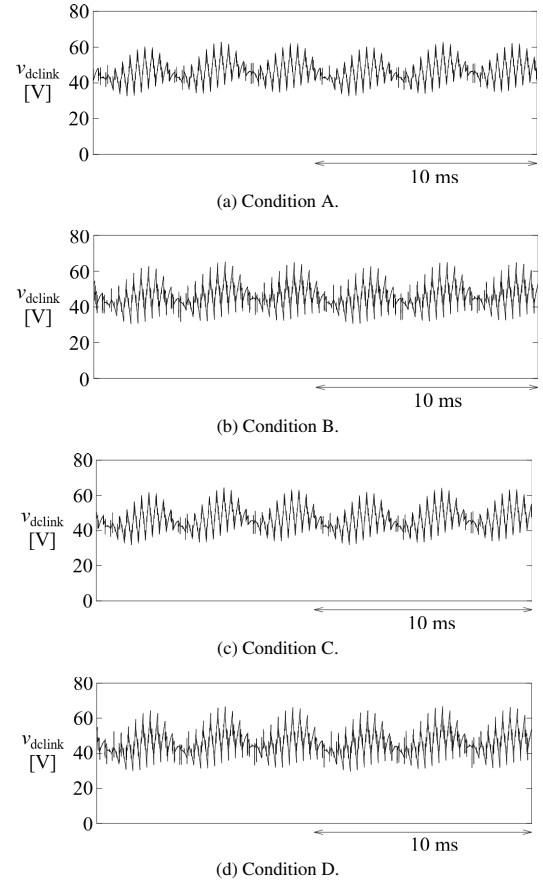


Fig. 12. Experimental waveforms of the DC-link voltage of the low-voltage inverter at V_{LV} = 48 V

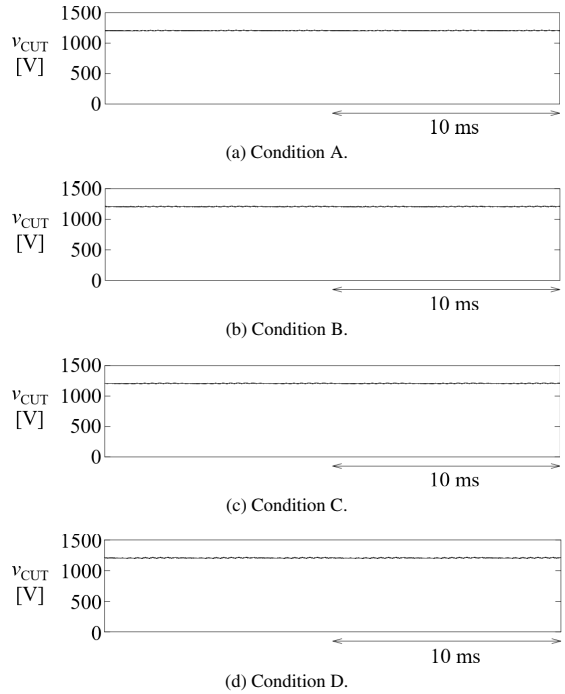


Fig. 13. Experimental waveforms of the voltage across the capacitor under test, v_{CUT} at V_{HV} = 1200 V

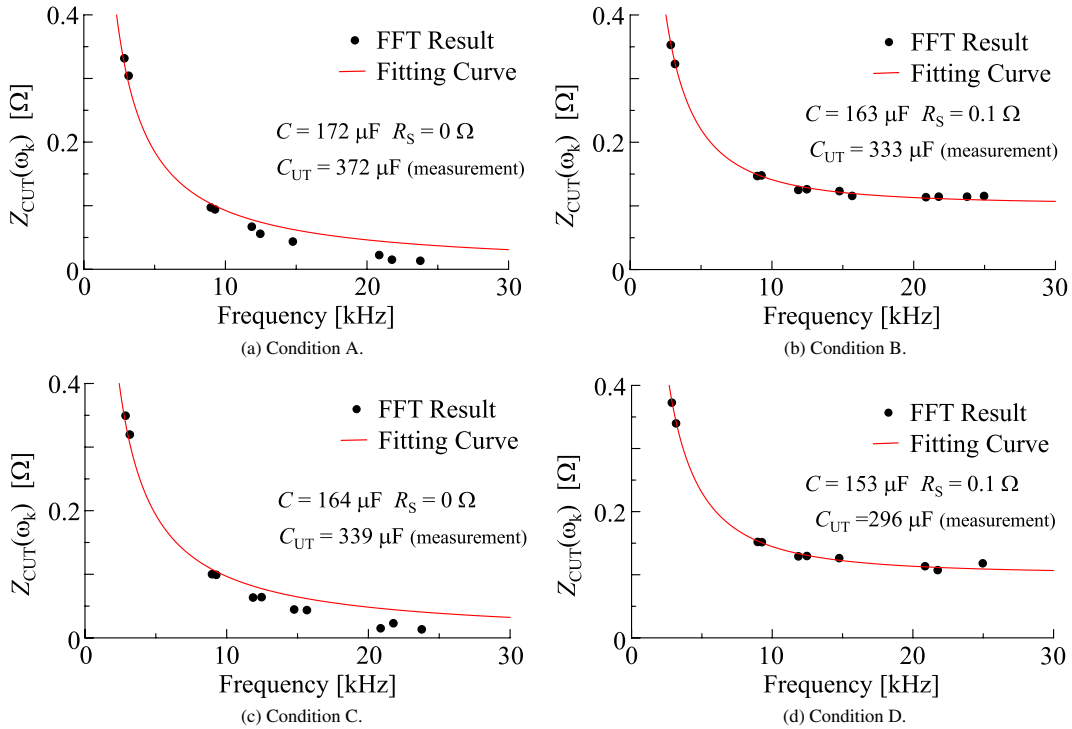


Fig. 14. Impedance profiles obtained from FFT results along with fitting curves indicating the ESR and capacitance

evaluation circuit, verifying that the power rating is 1/25 or lower of a full-scale high-power inverter. Experimental results obtained from a 1200-V 69-kVA system have verified that the monitoring method independently extracts the capacitance and ESR of the dc-link capacitor from the actual current generated by the inverter.

References

(1) J.W. Kolar, U. Drofenik, J. Biela, M. Heldwein, H. Ertl, T. Friedli, and S. Round: "PWM converter power density barriers", *IEE Japan Trans. Ind. Appl.*, Vol.128, No.4, pp.468–480 (2008)

(2) H. Wang and F. Blaabjerg: "Reliability of capacitors for dc-link applications in power electronic converters—an overview", *IEEE Trans. Ind. Appl.*, Vol.50, No.5, pp.3569–3578 (2014)

(3) K. Abe, H. Haga, K. Ohishi, and Y. Yokokura: "Current Ripple Suppression Control Based on Prediction of Resonance Cancellation Voltage for Electrolytic-Capacitor-Less Inverter", *IEEJ J. Ind. App.*, Vol.6, No.1, pp.1–11 (2017)

(4) S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner: "An Industry-Based Survey of Reliability in Power Electronic Converters", *IEEE Trans. Ind. Appl.*, Vol.47, No.3, pp.1441–1451 (2011)

(5) K. Harada, A. Katsuki, and M. Fujiwara: "Use of ESR for deterioration diagnosis of electrolytic capacitor", *IEEE Trans. Power Electron.*, Vol.8, No.4, pp.355–361 (1993)

(6) P. Venet, F. Perisse, M.H. El-Husseini, and G. Rojat: "Realization of a smart electrolytic capacitor circuit", *IEEE Ind. Appl. Mag.*, Vol.8, No.1, pp.16–20 (2002)

(7) A.M.R. Amaral and A.J.M. Cardoso: "Estimating aluminum electrolytic capacitors condition using a low frequency transformer together with a dc power supply", in Proc. of IEEE ISIE, pp.815–820 (2010)

(8) K. Abdennadher, P. Venet, G. Rojat, J.M. Retif, and C. Rosset: "A Real-Time Predictive-Maintenance System of Aluminum Electrolytic Capacitors Used in Uninterrupted Power Supplies", *IEEE Trans. Ind. Appl.*, Vol.46, No.4, pp.1644–1652 (2010)

(9) H. Soliman, H. Wang, and F. Blaabjerg: "A Review of the Condition Monitoring of Capacitors in Power Electronic Converters", *IEEE Trans. Ind. Appl.*, Vol.52, No.6, pp.4976–4989 (2016)

(10) H. Wang, D.A. Nielsen, and F. Blaabjerg: "Degradation testing and failure analysis of DC film capacitors under high humidity conditions", *Microelectron. Rel.*, Vol.55, No.9-10, pp.2007–2011 (2015)

(11) M. Makdessi, A. Sari, P. Venet, P. Bevilacqua, and C. Joubert: "Accelerated Ageing of Metallized Film Capacitors Under High Ripple Currents Combined with a DC Voltage", *IEEE Trans. Power Electron.*, Vol.30, No.5, pp.2435–2444 (2015)

(12) K. Hasegawa, K. Tsuzaki, and S. Nishizawa: "DC-bias-voltage dependence of degradation of aluminum electrolytic capacitors", *Microelectron. Rel.*, Vol.83, pp.115–118 (2018)

(13) RIPPLE CURRENT TESTER MODEL 11800/11801/11810, Chroma ATE Inc. 2014. [Online]. available: http://www.chromaate.com/File/DownLoad/42014

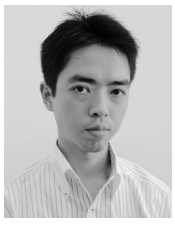
(14) B.P. McGrath and D.G. Holmes: "A general analytical method for calculating inverter DC-link current harmonics", *IEEE Trans. Ind. Appl.*, Vol.45, No.5 (2009)

(15) K. Hasegawa, K. Kozuma, K. Tsuzaki, I. Omura, and S. Nishizawa: "Temperature rise measurement for power-loss comparison of an aluminium electrolytic capacitor between sinusoidal and square-wave current injections", *Microelectron. Rel.*, Vol.64, pp.98–100 (2016)

(16) K. Hasegawa, I. Omura, and S. Nishizawa: "Design and Analysis of a New Evaluation Circuit for Capacitors Used in a High-Power Three-Phase Inverter", *IEEE Trans. Ind. Electron.*, Vol.63, No.5, pp.2679–2687 (2016)

(17) K. Hasegawa, I. Omura, and S. Nishizawa: "A New Evaluation Circuit with a Low-Voltage Inverter Intended for Capacitors Used in a High-Power Three-Phase Inverter", *IEEE APEC.*, pp.3032–3037 (2016)

(18) H. Fujita, S. Tominaga, and H. Akagi: "Analysis and design of a dc voltage-controlled static var compensator using quad-series voltage-source inverters", *IEEE Trans. Ind. Appl.*, Vol.32, No.4, pp.970–977 (1996)



Kazunori Hasegawa (Member) received the B.S. degree in electrical engineering from Tokyo Metropolitan University, Tokyo, Japan, in 2007, and the M.S. and Ph.D. degrees in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2009 and 2012, respectively. He is currently an associate professor with Kyushu Institute of Technology, Kitakyushu, Japan. His research interests include power conversion systems, reliability-related issues of power converters and components, and motor drives. Dr. Hasegawa was the recipient of the Student Paper Award at the 2010 IEEJ/IEEE International Power Electronics Conference-Sapporo and the 2018 IEEE Transactions on Power Electronics Prize Letter Award.

Shin-ichi Nishizawa (Non-member) received the B.Eng., M.Eng., and Dr.Eng. in chemical engineering from Waseda University, Tokyo, Japan, in 1989, 1991, and 1994, respectively. He then joined Waseda University as a Research Associate. In 1996, he joined the Electrotechnical Laboratory, Tsukuba, Japan (since 2001, the National Institute of Advanced Industrial Science and Technology). Since 1998, he has worked on SiC bulk crystal growth and epitaxy, and promoted the research of semiconductor wafer processes for advanced power devices. From 2013 to 2017, he was a Visiting Professor at Kyushu Institute of Technology, Kitakyushu, Japan. Since 2017, ha has been a professor at Kyushu University, Fukuoka, Japan. He is the author or coauthor of over 150 publications and 20 patents. His research interests include semiconductor wafer technologies for power devices, power electronics components, and systems. Dr. Nishizawa is a member of the Japan Society of Applied Physics, the Japanese Association for Crystal Growth, and the IEEE Electron Devices and Power Electronics Societies.

Ichiro Omura (Member) received the M.S. degree from Osaka University, Osaka, Japan, and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, in 1987 and 2001, respectively. In 1987, he joined Toshiba Corporation, Kawasaki, Japan, where he was engaged in research on power semiconductors, including high-voltage IGBTs, superjunction MOSFETs, and GaN power devices. From 1996 to 1997, he was a visiting researcher at ETH. Since 2008, he has been with Kyushu Institute of Technology, Kitakyushu, Japan. He has authored and coauthored over 100 journals and conference papers, has filed more than140 patent applications, and holds more than 40 patents in the field of power semiconductors. He has been the Director of the Next Generation Power Electronics Research Center, Kyushu Institute of Technology, since 2012. His research interests include new power semiconductor device design, reliability testing with new monitoring systems, and advanced gate drive system technology.