Current Imbalance Monitoring in SiC-MOSFET under Unclamped Inductive Switching by Tiny PCB Rogowski Coil

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Abstract

We monitored the current imbalance in a SiC-MOSFET chip under unclamped inductive switching condition by using our printed circuit board Rogowski coils. The current imbalance varied significantly from sample to sample. The SiC-MOSFET with a larger current imbalance was destroyed with lower avalanche current than other samples. It is assumed that the chip was destroyed due to partial temperature rise accompanying current concentration from current distribution and thermal simulation. The result shows that the current monitoring system is effective for analysis of avalanche robustness.

Keywords: SiC-MOSFET, Current Imbalance, Unclamped Inductive Switching (UIS), Rogowski coil, Printed Circuit Board (PCB), Thermal simulation.

INTRODUCTION

Power semiconductor devices are widely applied to various power electronics products and fields, such as hybrid electric vehicles, railway and High Voltage Direct Current (HVDC) transition and the market is rapidly expanding. Since the destruction of a power semiconductor device may lead to a serious risk, power semiconductor devices are required to have high reliability. Destruction under Unclamped Inductive Switching (UIS) is a typical catastrophic phenomenon. To prevent the destruction, high avalanche breakdown robustness is required for the devices.

SiC-MOSFET is expected to have low power loss and high-speed switching capability. The avalanche breakdown robustness of SiC-MOSFET has been reported in previous studies [1-6]. In previous studies, the causes of the destruction have been classified into current concentration and temperature rise overall chip [2]. Since current concentration leads to a local temperature rise in the chip, destruction occurs with lower current than the temperature rises overall chip. In other words, the current concentration is more serious than the temperature rise. Several studies have monitored the current distribution in the chip or the heat distribution on the surface. In this study, we used Printed Circuit Board (PCB) Rogowski coils for the current imbalance monitoring in SiC-MOSFET under the UIS condition [7-11]. There are two reasons for employing a PCB Rogowski coil. First, current can monitor high time resolution and one pulse. Second, it is possible to put on real wiring the same as the power module structure by using a PCB Rogowski coil.

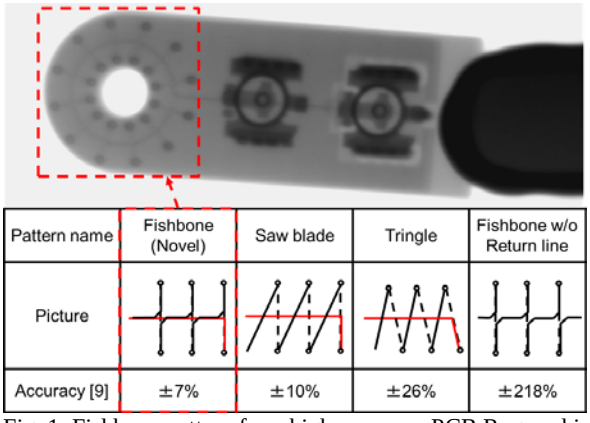

Fig. 1: Fishbone pattern for a high-accuracy PCB Rogowski coil and other typical coil patterns

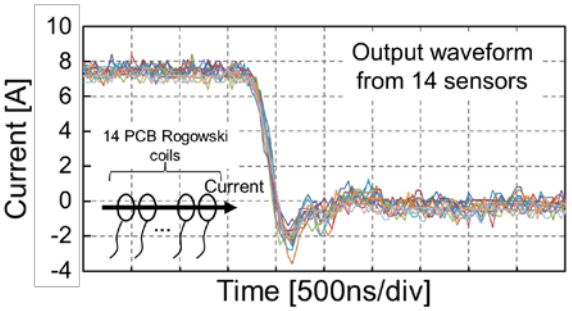

Fig. 2: Output waveform from 14 PCB Rogowski coils with integral amplifier and digitizer

EXPERIMENTAL SETUP FOR CURRENT IMBALANCE MONITORING UNDER UIS CONDITION

Current Sensor Using Tiny PCB Rogowski Coil

In our previous studies, we proposed a current sensor using a tiny PCB Rogowski coil with a fishbone pattern [7-8]. The sensor is extremely small, thin and inexpensive. The pattern we proposed has less noise than any typical PCB Rogowski coil pattern, resulting in higher accuracy. The PCB Rogowski coil was experimentally produced, and the noise caused by the non-measurement current was inspected. As a result, it confirmed that the PCB Rogowski coil having a fishbone pattern has high accuracy (Fig. 1). Further improvement of the accuracy of the PCB Rogowski coil was advanced using noise shield layers and a microwave coaxial interface between PCB and cables now. These characteristics such as very small size and high accuracy make it suitable for current imbalance monitoring in power devices under a noisy environment. The PCB Rogowski coil has a high frequency bandwidth up to 40MHz, which is comparable to commercially available current sensors. Because the manufacturing error of the PCB is small, many of the same PCB Rogowski coils show the same switching current waveform with small signal variation (Fig. 2)

Experimental Setup

The current imbalance in SiC-MOSFET is monitored by UIS test circuit (Fig. 3). The SiC-MOSFET chip is simply connected to the inductor in series. Since two bonding wires are connected to one chip, we monitored two current waveforms.

The current monitoring system consist of PCB Rogowski coils, integral amplifier, digitizer, PC, commercially available current sensor and an oscilloscope (Fig. 4). The PCB Rogowski coils generate a flux signal corresponding to the current following through each source pad of the

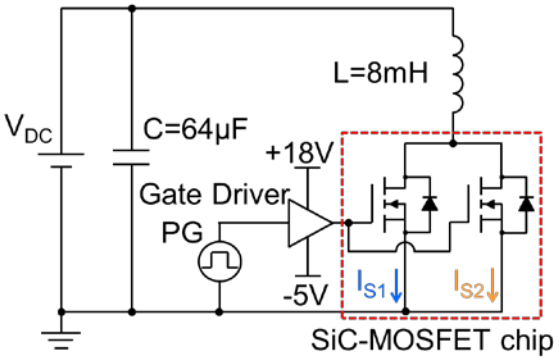

Fig. 3: Schematic of Unclamped Inductive Switching test circuit

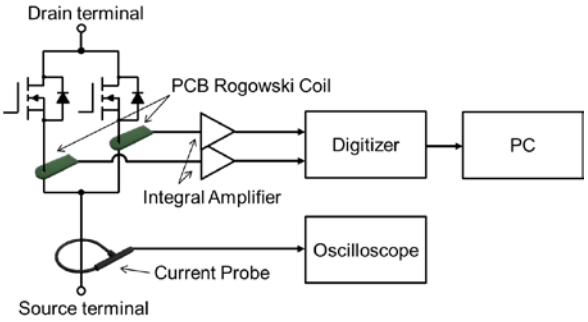

Fig. 4: Schematic of cuurrent monitoring system

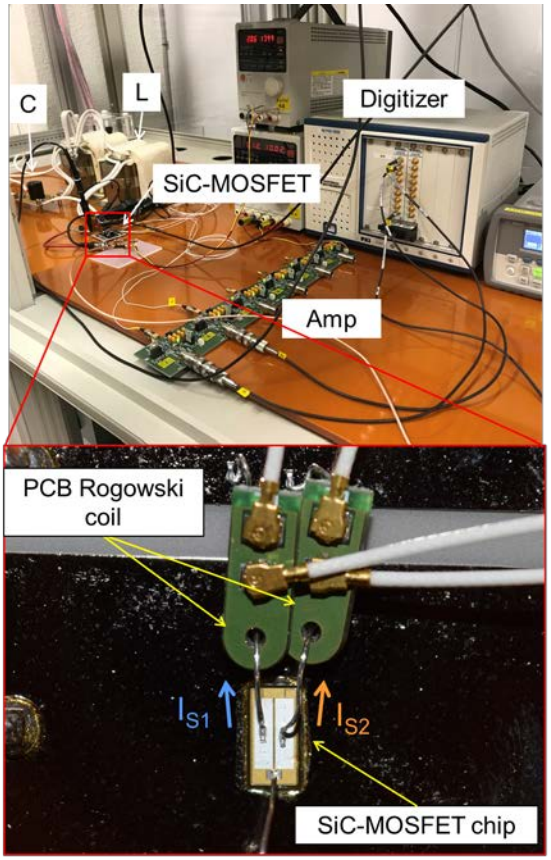

Fig. 5: Exerimental setup for current imbarance monitoring

SiC-MOSFET (I_{S1} and I_{S2}). The integral amplifiers integrate and amplify the signals from the respective PCB Rogowski coils. The digitizer converts the analogue signals into digital data. The PC uses LabVIEW software to perform offset correction and droop correction of the input signals from the digitizer [11]. This system uses a commercially available current probe with an oscilloscope to monitor the total source current (I_S) for the confirmation of the current with PCB Rogowski coil. The chip size of sample SiC-MOSFET is 3.1 mm by 5.9 mm. The source electrode is divided into two pads and

aluminium wires are bonded to each pad (Fig. 5). The rated blocking voltage and DC current are 1200 V and 63 A respectively. The current imbalance was monitored for three samples under several UIS conditions.

RESULTS OF CURRENT IMBALANCE MONITORING

The total current measured by the PCB Rogowski coils corresponded with the current measured by a commercially available sensor thanks to the fishbone pattern of the PCB Rogowski coil and noise shield layers (Fig. 6) [8]. This agreement shows the validity of the measurement results.

The UIS test was carried out from avalanche peak current (I_{AV}) of 1 A until chip destruction in 1 A increments for three samples. The current imbalance varied significantly from sample to sample (Fig. 7 to Fig. 9). Sample A and B shows small current imbalance and withstands higher I_{AV} of 21 A and 22 A respectivery (Fig. 7 and Fig. 8). In contrast, sample C shows a large current imbalance at just after turn-off, failed at I_{AV} of 18 A (Fig. 9). The damaged point of sample C was found on the pad with a large current (Fig10). From the waveforms and the damaged point of the chip, it is assumed that sample C is destroied due to partial temperature rise accompanying current concentration. This result shows that the current monitoring system is effective for analysis of avalanche robustness.

RESULTS OF CURRENT IMBALANCE SIMULATION

We simulated the pertial tmeparature for each emitter pad. The simulation model is composed with thermal resistance and thrmal capacitance (Fig. 11) [12-13]. The SiC chip is devied into 10 unit in the thickness direction and the solder layer is 1 unit. The input power is calculated from the product of the current of one pad and voltage betwen drain and source.

The tenparature imbalance coresponds the curent imbalance and reaches about 800 C (Fig. 12 to Fig. 14). The distruction is happened on the higher current pad at the highest temparature time with all samples. At the moment of distruction, the temparature of other pad is decreased by a few degrees from peak temparature.

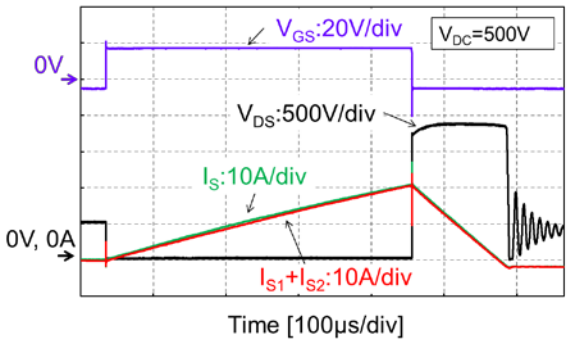

Fig. 6: Exerimental V_{GS}, V_{DS}, I_S and I_{S1}+ I_{S2} waveform at avalanche peak current of 21 A in sample B

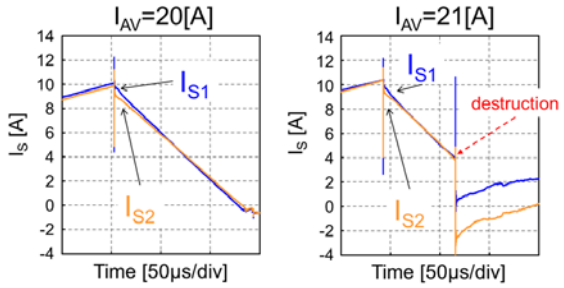

Fig. 7: I_{S1} and I_{S2} waveform at avalanche peak current of 20 A and 21 A in sample A

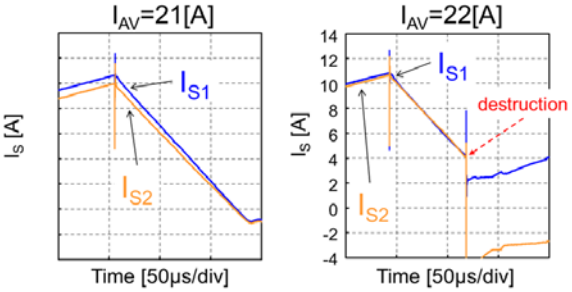

Fig. 8: I_{S1} and I_{S2} waveform at avalanche peak current of 21 A and 22 A in sample B

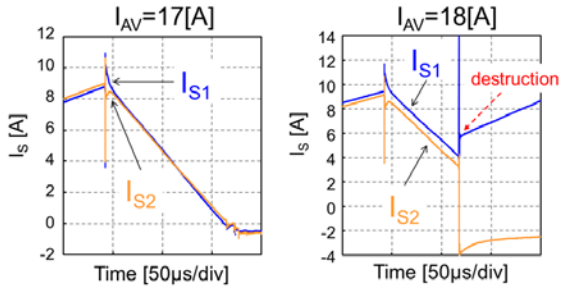

Fig. 9: I_{S1} and I_{S2} waveform at avalanche peak current of 17 A and 18 A in sample C

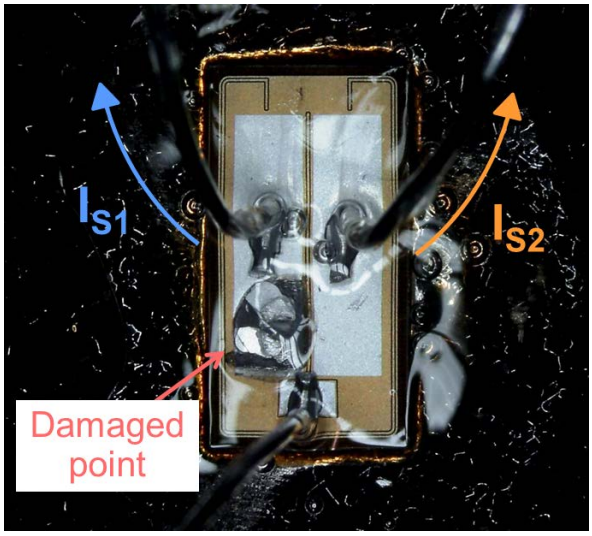

Fig. 10: Damaged point of SiC-MOSFET for sample C at avaranche peak current of 18 A

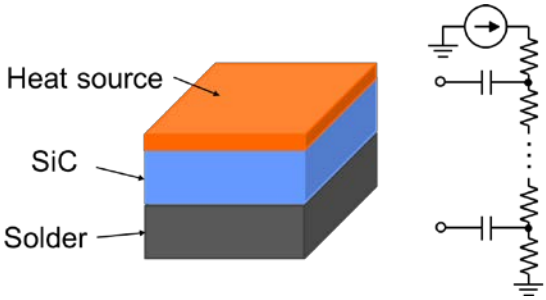

Fig.11: Thermal simulation model for one emitter pad

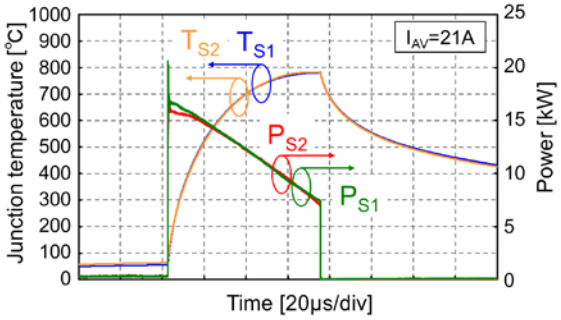

Fig. 12: Simulated junction temperature and power for each pad at device destruction in sample A

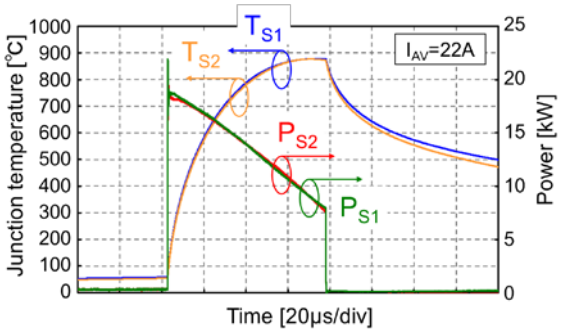

Fig. 13: Simulated Junction temperature and power for each pad at device destruction in sample B

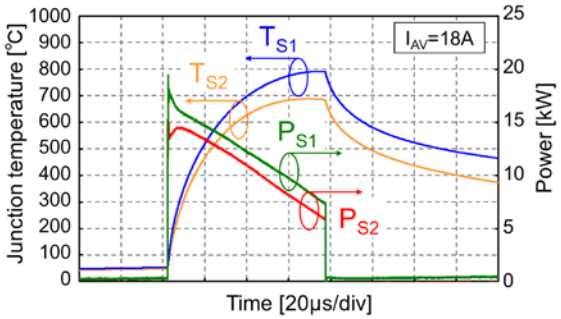

Fig. 14: Simulated Junction temperature and power for each pad at device destruction in sample C

CONCLUSION

We succeeded to monitor current imbalance in a SiC-MOSFET chip under UIS test by using a tiny PCB Rogowski coil. The current imbalance is different from sample to sample. The SiC-MOSFET with a larger current imbalance was destroyed with lower avalanche current than other samples. It is assumed that the chip was destroyed due to partial temperature rise accompanying current concentration from current distribution and thermal simulation. These results show that the current monitoring system is effective for analysis of avalanche robustness.

ACKNOWLEDGEMENT

The authors would like to thank Wataru Saito at Toshiba Electronic Devices & Storage Corporation for significant discussion on this work.

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