An Investigation on FPGA Implementation of Model Predictive Control for Three-Phase Voltage Source Inverters: Model-Based Design (MBD) Approach, Hardware-in-the-Loop (HIL) Simulation and FPGA Resource Optimization

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ABSTRACT

Model predictive control (MPC), a modern switching control method, has gained considerable interest in performing control objectives of power converters. One of the categories in a wide family of MPC is finite control set-MPC (FCS-MPC) that utilizes the discrete-time model of a power converter having a limited number of switching states for solving the optimization problem online. In FCS-MPC, a discrete-time model of the power converter is used to predict future values of control parameters and an optimization function (cost function) is used to select the optimized switching state of the converter. High computational requirements of the FCS-MPC is a concern for the system implementation. Field-programmable gate array (FPGA) is an effective alternative to handle the computational burden of the control algorithm because of its parallel processing nature.

In general, the MPC algorithm is performed through a programming approach either for DSP or FPGA. However, digital resource utilization is another concern for the development and real-time system implementation. Digital resource optimization requires a high value of in-depth knowledge to write the hardware descriptive code. Moreover, debugging is also a tedious and time-consuming task that is not appropriate for the development and analysis of the controller as well as prototyping. In this work, the implementation of FCS-MPC is performed by adopting the modelling approach in a digital simulator that provides a virtual FPGA environment for system development. In addition, hardware-in-the-loop (HIL) technique is used for testing of controller performance before experimental validation.

The current prediction is a core part of the FCS-MPC and a coefficient used for the current prediction that is computed using the system parameters affects the controller performance. In this work, a novel approach is presented to update the predictive model, called an adaptive predictive model, corresponding to a change in the load resistance while keeping a fixed value of load inductance. The fixed, approximated and adaptive values of a coefficient are adopted for current prediction to investigate the behaviour of the controller.

The performance of the FCS-MPC depends on the sampling frequency used for the discretization of the converter model that governs the switching frequency of the

converter. The performance can be improved with higher sampling frequency, however, resulting in higher switching frequency that ultimately increases the switching losses in the power devices. Apart from that, a non-zero steady-state error is one of the concerns of the FCS-MPC implementation.

In general, dedicated constraints for the reduction in average switching frequency and SSE are incorporated inside a cost function in conventional FCS-MPC. Nevertheless, that ultimately increases the computational burden. A modified cost function based on a novel constraint is proposed for the improvement in SSE as well as a reduction in the switching frequency using the modified FCS-MPC approach. To validate the performance of the proposed constraint, a comparative analysis is presented with the constraint of a change in switching state considering indices SSE as well as average switching frequency. Moreover, the different load currents and sampling time are considered to evaluate SSE considering similar load current ripples. To evaluate the robustness of the FCS-MPC algorithms, a step-change in reference current is considered for the demonstration of dynamic performance.

Moreover, an analytical approach based implementation strategies is proposed for FPGA resource optimization of the FCS-MPC development in a digital simulator for the FPGA-based system implementation. The implementation of FCS-MPC in stationary αβ and rotating dq frames is adopted for in-depth system analysis. The implementation strategies are compared based on FPGA resource requirements for the FCS-MPC in both frames corresponding to the fixed, approximated and adaptive coefficient values of the predictive model.

The optimum design based controller model is used for the FPGA-based experimental system implementation. Xilinx system generator (XSG) as a digital simulator that is an integrated platform with MATLAB/Simulink is used for the development of the controller. The FCS-MPC is implemented for the load-side current control of a three-phase voltage source inverter (VSI) system. A Xilinx FPGA board (Zedboard Zynq Evaluation and Development Kit) is used for the HIL simulation as well as the real-time system implementation.

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Journal Papers

(1) V. K. Singh, R. Tripathi, and T. Hanamoto, "HIL Co-simulation of Finite Set-Model Predictive Control using FPGA for a Three-Phase VSI System," *Energies*, vol. 11, no. 4, 909, April 2018.

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Conference Papers

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(5) V. K. Singh, R. Tripathi, and T. Hanamoto, "Comparative Analysis of Finite Control Set MPC for Voltage Source Inverter," in *5th International Conference on Electric Power and Energy Conversion Systems* (EPECS 2018), Kitakyushu, Japan, April 23–25, 2018.

Co-authored

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(3) I. Mishra, R. Tripathi, V. K. Singh, and T. Hanamoto, "Comparative Analysis of Continuous PWM and Discontinuous PWM for PMSM Drive", in *6th International Symposium on Applied Engineering and Sciences* (SAES 2018), Kitakyushu, Japan, Dec 15–16, 2018.

Chapter 1

INTRODUCTION

1.1 Energy Demand and Challenges

In recent years, the energy demand has been growing at a rapid rate, because of the population, technological advancement, and economic growth. The global energy demand will continue to increase further due to the rapid increase of consumption in domestic as well as industries. Much of the energy demand is concentrated in developing countries (India, China, and others) according to the geography of global energy demand shown in Fig. 1.1, where rising prosperity and improving living standards support increasing energy consumption per head [1]. Since 1970, the energy demand has been mainly satisfied by conventional or non-renewable energy sources such as fossil fuels (mainly oil, coal, and gas) as shown in Fig. 1.2. According to the energy consumption forecast, the increased energy demand will be satisfied mainly by fossil fuels until 2030 [2]. However, dependency on fossil fuels will be decreased significantly due to the revolutionary efforts in other non-conventional energy resources.

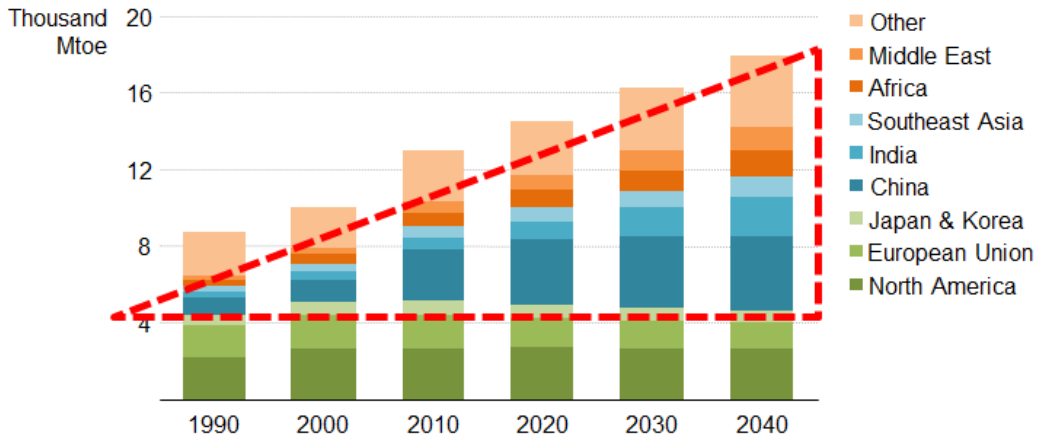


Fig. 1. 1. Geography of global energy demand by region in the new policies scenario (source: International Energy Agency (IEA), WEO-2016) [1].

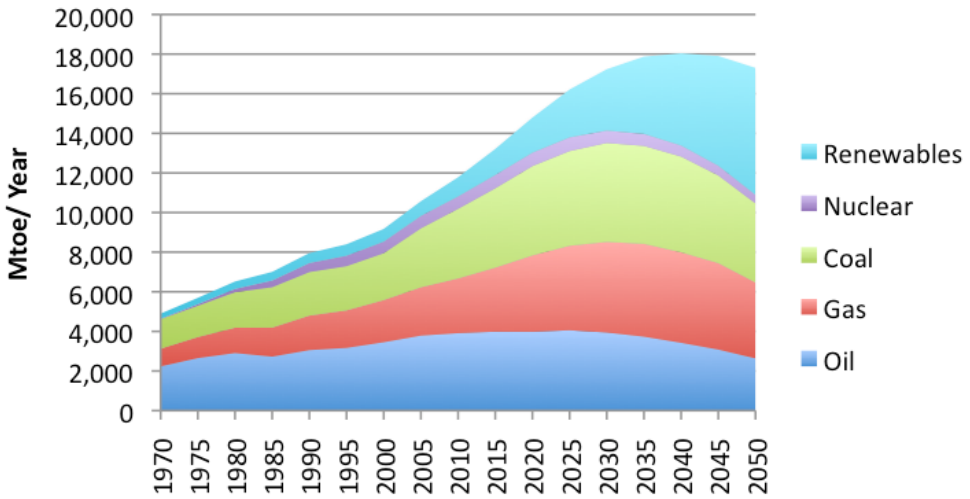


Fig. 1. 2. Energy consumption forecast with the share of various energy resources (source: a book '2052-A Global Forecast for the Next Forty Years') [2].

The higher consumption of fossil fuels leads to higher greenhouse gas emissions, particularly carbon dioxide (CO2), which contribute to global warming. Moreover, the depletion of conventional energy sources has become important matters of global concern due to the rise in energy demand. Hence, while accompanied by greater prosperity, rising demand creates new challenges. The customized living standards, energy security concerns, provide access to modern energy services, use energy more efficiently, protect the global environment and ensure reliable energy supplies, etc. are the possible challenges. A sustainable energy future will require new thinking and new systems – essentially a transformation in the way we produce, deliver and consume energy [3]. The energy generation from non-conventional or renewable sources has to play a major role to fulfill energy demand and to tackle environmental issues. Some adequate renewable sources such as solar, wind, biomass, ocean, and geothermal, are capable of accomplished clean and green energy without affecting the environment. Solar photovoltaic (PV) and wind are prominent among available renewable sources to generate power.

1.2 Role of Power Electronics

To harvest the power from those renewable energy sources, a suitable high-efficiency energy conversion system for the industrial processes are essential. Power Electronics plays a vital role in the control and conversion of electric power with the smart application of solid-state devices [4]. Power electronics have already found an important place in modern technology and are now used in a great variety of high power

product, including heat controls, light controls, electric motor control, power supplies, vehicle propulsion system, high voltage direct current (HVDC) systems and to name a few. The silicon power semiconductor devices such as thyristor, power MOSFET, insulated gate bipolar transistor (IGBT), Triac, gate turn-off thyristor (GTO), and integrated gate-commuted thyristor (IGCT) have been utilized according to the applications.

Power electronics technology is associated with efficient energy conversion as well as control and conditioning of electrical energy from source to load. Power electronics converters are the backbone of the conversion systems that convert the one form of electrical power in another form such as conversion from AC to DC, altering the magnitude, phase or frequency of voltage and current, etc. The improvement in the efficiency of power electronics converters is one of the challenging topics. In this process, the key steps are being taken by researchers such as the evolution of faster devices, improved topologies, and advanced controls. The power converter that converts DC to AC (inverter) has a wide variety of practical applications including adjustable speed drives (ASD), uninterruptible power supplies (UPS), flexible AC transmission systems (FACTS), and voltage compensators [5]. There is two most common type of inverters: voltage source inverter (VSI) and current source inverter (CSI). According to their names, VSIs are fed with constant voltage and CSIs are fed with constant currents.

VSIs are one of the common types of inverters that have been used for various applications such as renewable energy systems, AC motor drives, DC battery, induction heating, AC UPS, high voltage DC (HVDC) power transmission, active power filter, etc. [6]. One very common application of VSI is commercially available inverter units used in homes and offices to power some essential AC loads in case the utility AC supply gets interrupted. The battery supply is used as the input DC voltage source and then the DC voltage is converted into AC voltage of desired frequency as well as amplitude. There are many classifications of VSIs according to different criteria. They can be classified based on the number of phases in the output (commonly single-phase and three-phase). Another type of VSI classification is based on their ability to control the output parameters such as

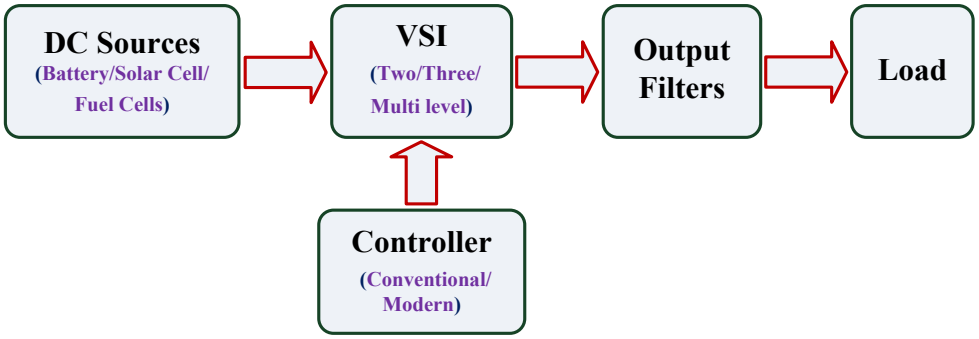


Fig. 1. 3. General block diagram of the power conversion system with VSI.

frequency, voltage, harmonic content. VSIs may also be classified according to their topologies. Some inverter topologies are suitable for low and medium voltage applications (e.g. two-level three-phase VSI) whereas some others are suitable for high voltage applications (e.g. multilevel inverter topologies).

The performance of VSIs is dependent on the controller used to control the desired parameters (e.g. voltage, current, torque, flux). The desired control objectives are satisfied through the appropriate switching of power devices used in the VSI. A general block diagram of a VSI system is depicted in Fig. 1.3. The DC input supply for the VSI system can be connected through the battery, solar PV or fuel cells. The output filters are generally utilized for the desired quality of sinusoidal output voltage and current. The controller is a driving component of the power conversion system. Several control schemes have been utilizing according to the application as well as the power devices. Historically, thyristors with lower switching frequencies have been controlling by regulating the firing angle with the analog control circuit. The analog control circuits were later on replaced by digital control platforms with the possibility of implementing more advanced control schemes with the introduction of power transistors with faster switching frequencies [4]. The control schemes for power converters and drives are briefly summarized in the next subsection.

1.3 Power Converter Control

The several conventional and modern control schemes have been studied and proposed in the literature to improve the performance of power converters. The control schemes for power converters and drives are summarized in Fig. 1.4 [7], [8]. The conventional control

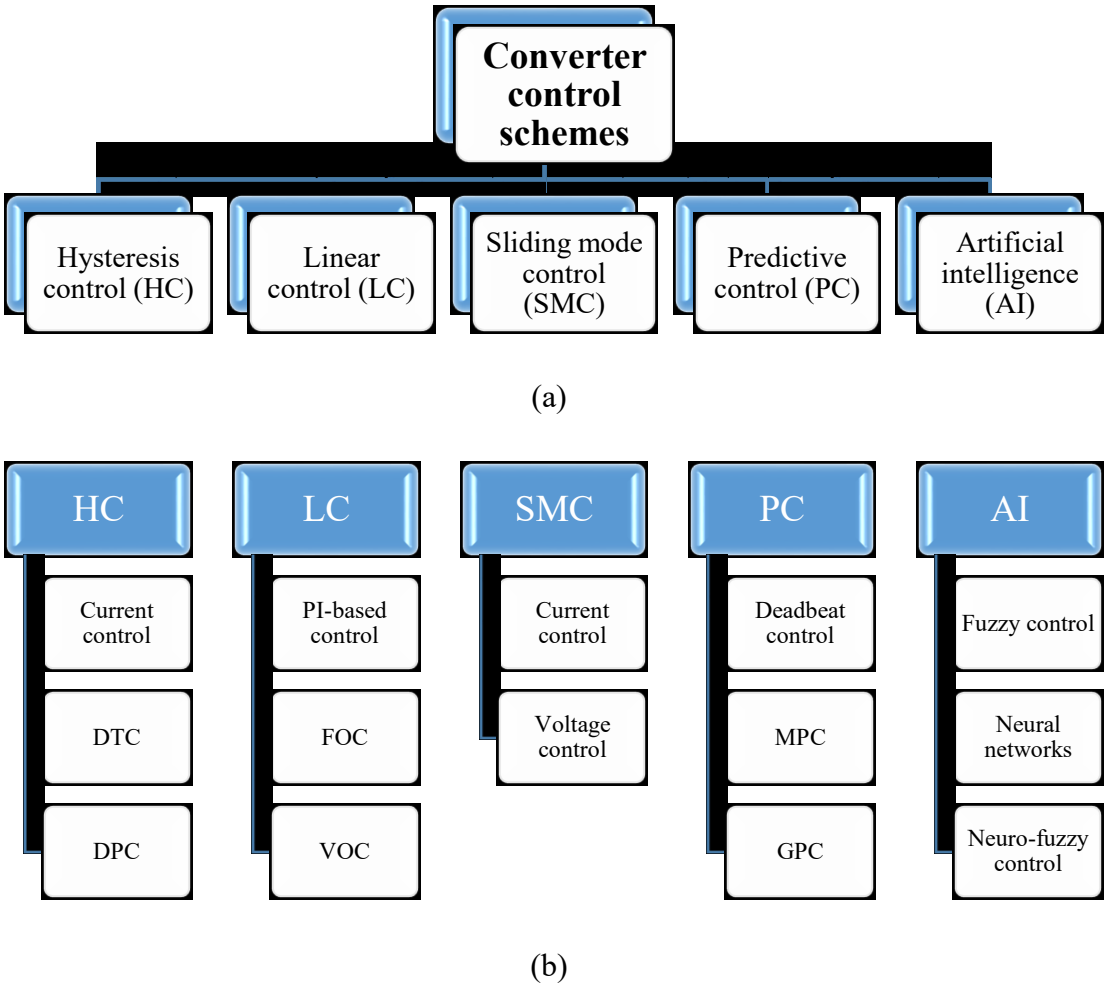


Fig. 1. 4. Classification of control schemes for power converters and drives.

schemes are hysteresis control and linear control (mainly pulse width modulation (PWM), space vector modulation (SVM)). There are some categories of modern control strategies such as sliding mode control (SMC), model predictive control (MPC) and artificial intelligence (AI).

Hysteresis control is one of the mature control schemes for industrial applications due to simple nature. It is the type of non-linear control and the switching signals of the power devices are determined by the comparison of the measured variable with the reference variable. The concept is to keep the error within the specified tolerance called hysteresis band/error band. The inversely proportional relation of the switching frequency and hysteresis band results in the varying switching frequency corresponding to the upper and lower specified hysteresis band. This scheme provides a fast dynamic response, but, the variable switching frequency results in a spread spectrum and resonance problems in some applications. Normally this scheme is implemented through analog circuits due to its inherent nature, however, to implement it in a digital

platform, a very high sampling frequency is required. This control scheme has been utilized not only for the simple current control applications but also for complex applications of direct torque control (DTC) [9], [10] as well as direct power control (DPC) [11].

Linear control behavior of power converters can be obtained by a modulation technique such as pulse width modulation (PWM) or space vector modulation (SVM) [12], [13]. SVM is just a variation of regular sampled PWM. The PWM signal is generated by comparing a lower frequency reference signal to a high-frequency carrier. The linear control scheme with a modulation technique normally requires additional coordinate transformations. In a linear control of power converters and drives, there are normally three types of widely used control schemes: proportional-integral (PI) based controllers for both current and voltage control, voltage-oriented control (VOC) [14] for grid-connected inverters and field-oriented control (FOC) [10], [15] for motor drive applications. These control schemes have been widely used in the industries, however, these can be challenging for some converter topologies such as matrix converters and multi-level converters due to several design steps with the additional modulation stage that increases complexity.

Sliding mode control (SMC) is a non-linear control scheme where the control action is discontinuous and follows a predefined control switching law [16], [17]. It works on the principle that the system states can be driven onto a surface in the state space, called a sliding surface. There are mainly two parts of controller design. In the first part, the sliding surface is designed such that the sliding motion satisfies design requirements. The latter part involves the selection of a control law that results in switching surface attractive to the system state. This scheme is suited to control the effect of model parameter uncertainties, disturbance, and nonlinearity in a system. There are some remarkable features of SMC such as accuracy, robustness and easy tuning.

Predictive control has been receiving popularity for the control of power converters and drives [18]–[20]. It comprises a wide family of controllers with different approaches. Predictive control is characterized by the use of a model of the system to predict the future behavior of the controlled variables, and the use of an optimization criterion for selecting the optimum actuation. The deadbeat control, one of the basic predictive control, uses the idea where a prediction is made for the optimum actuation

so that the error between the reference and the controlled variables will be zero at the next sampling instant for the first-order system. Among the various classifications of predictive control, model predictive control (MPC) is one of the most popular control schemes due to its several attractive features. MPC is the main focus of this thesis and the detailed explanation with the literature review is presented in the next subsection.

1.4 Literature Background

MPC is considered as an advanced method of process control for complex multiple-input multiple-output (MIMO) process. The process control using MPC has been performed in the process industries such as chemical plants and oil refineries with low sampling requirements since the 1980s. After that, the idea of MPC was applied in the field of power electronics considering high power systems with low switching frequency. Since the last decade, the availability of high-speed microprocessors has triggered research in MPC for power electronics and drive applications. Although MPC implementation requires high computations, it has gained attention in the power electronic research community due to its distinctive features such as fast dynamic response, intuitive and logical concept, handling complex MIMO cases, flexibility in constraint inclusion and handling system nonlinearities. The role of MPC in the evolution of power electronics was presented in [18] and a comparative description is given with the different control schemes. In [19], a wide review of the applications of MPC in power electronics is presented considering various applications such as grid-connected converters using active front end (AFE) and active power filter (APF), control of a matrix converter, control of multilevel inverters, inverters with output LC filter and high-performance drives. In [20], a survey of various MPC schemes was presented for the power converters and drives with a detailed comparative analysis including future trends.

The basic principle of MPC is based on a model to predict the future behavior of the control variables over a prediction horizon. Then, the control function or cost function is evaluated for the desired behavior of the system and the optimum actuation is selected according to the minimum cost function. One of the major deciding factors for MPC performance is the model precision that gives an accurate prediction. MPC strategies are broadly classified as continuous control set-MPC (CCS-MPC) and finite control set-MPC (FCS-MPC). The CCS-MPC computes continuous control signals

with constant switching frequency by using a modulator, whereas FCS-MPC implements the MPC algorithm by utilizing the discrete nature of the power converter and applies the switching signals directly to the power converter without the need for an external modulator that results in variable switching frequency. FCS-MPC is designed to reduce the computational burden of the algorithm by utilizing the set of possible switching states of power converters for solving the optimization problem online.

One of the characteristics of FCS-MPC is to control multiple variables using a single cost function and is more favorable for controlling complex power converters and electric motor drive systems. Moreover, the direct application of optimized control action without need a modulation stage is an awesome feature of this control scheme. In the literature FCS-MPC is sometimes termed as finite-set model predictive control (FS-MPC) [21], [22] or finite-state model predictive control (FS-MPC) [23], [24] or direct model predictive control (D-MPC) [25]. Various literatures have reported with FCS-MPC application in power converters such as two-level VSI [30], [31], three-level neutral point clamped (NPC) [32], [33], cascaded H-bridge (CHB) multilevel converters [34], [35], flying-capacitor converter (FCC) [21], [36], AFE rectifiers [40]–[42], matrix converters [47]–[56] etc. A list of different power converter topologies is depicted in Fig. 1.5.

The application of FCS-MPC as current control of a two-level inverter is discussed in [30]–[32]. Similarly, the current control of three and four-level inverters using the FCS-MPC is presented in [31]–[33], [57] and [58] respectively. A comparative assessment of FCS-MPC with linear current control schemes based on the comparable switching frequencies is presented in [30], [59]. The FCS-MPC has been implemented for the voltage control of converters with second-order LC output filters in [60]–[62].

Despite several attractive features, the FCS-MPC encounters some major drawbacks. The variable switching frequency is one of the drawbacks of the FCS-MPC scheme which causes switching losses and unwanted resonances [32], [63]. Moreover, variable switching

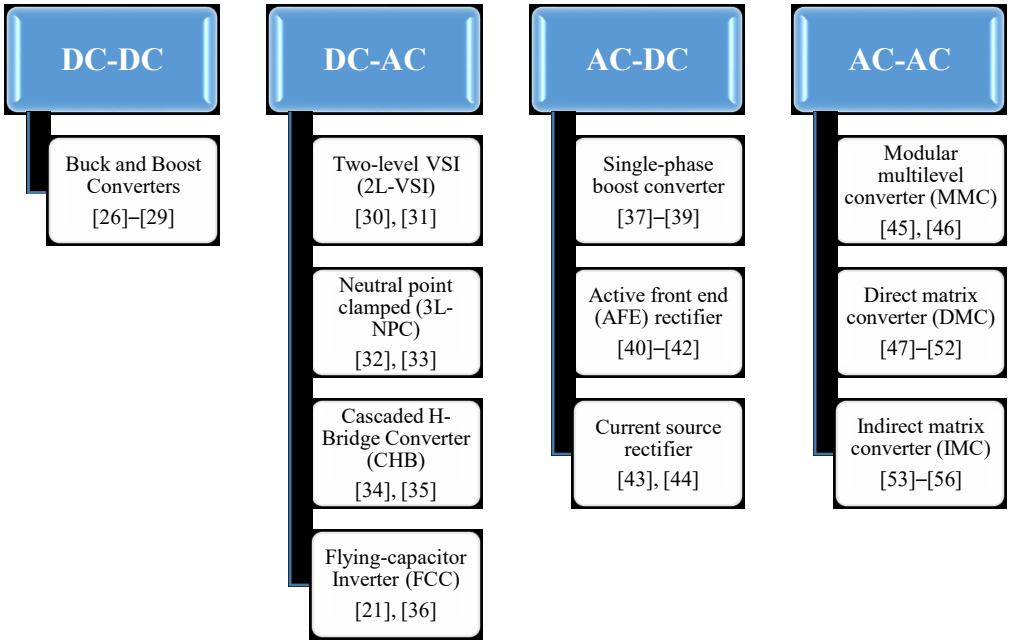


Fig. 1. 5. A literature review for the application of FCS-MPC in different power converters.

frequency results in a spread spectrum of voltage and current over a wide range of frequencies. In FCS-MPC, the sampling time for the discretization of the converter model governs the switching frequency of the converter and the system performance improves with lower sampling time i.e. higher sampling frequency. However, the higher sampling frequency is one of the causes of higher switching frequency that results in even higher switching losses [63]. The functionality of incorporating additional parameters inside a cost function can be utilized for switching frequency reduction to optimize the switching frequency with primary control parameters simultaneously and to implement the system with lower sampling time depending on the permissible maximum switching frequency of the power devices. The problem of switching frequency has been addressed and some methodologies have been presented towards the reduction of switching frequency for multilevel active rectifiers [64], cascaded H-bridge multilevel converter [65], modular multilevel converter [66] and three-level inverter-fed induction motor drives [67]. The fundamental idea to minimize control effort with switching frequency reduction has been studied and analyzed with the inclusion of constraint inside the cost function such as the change in switching state to control the number of commutations of the power switches [32], [68] and change in voltage vector [32], [69]. Moreover, the computational burden for change in switching state constraint is comparatively low and preferred for implementation as compared to the change in voltage vector constraint.

Another issue with FCS-MPC is the nonzero steady-state error (SSE). This error is more significant when operated with lower switching frequency or lower amplitude of current reference [70-72]. In [70], the concepts of intermediate sampling, as well as integral error term, were proposed to face the problem of SSE and results were presented for the current control of the four-quadrant chopper converter. In [71], the problem of SSE during model parameter mismatch was addressed and an approach to incorporate past current errors as a constraint inside a cost function with a variable weighting factor was proposed towards the elimination of SSE.

In general, dedicated constraints for the reduction in average switching frequency and SSE are incorporated inside a cost function in conventional FCS-MPC. Nevertheless, that ultimately increases the computational burden. An approach presented in [73] for modified FCS-MPC to reduce the computational burden of the conventional FCS-MPC by the elimination of the current prediction step. In the modified FCS-MPC, the reference voltage vector is evaluated once in each sampling interval as a single current prediction. In addition, change in switching state constraint is incorporated with modified FCS-MPC for the reduction of the average switching frequency. However, the SSE is not considered and compared with conventional FCS-MPC. It is desirable to achieve improved SSE with a reduction in average switching frequency considering the computational burden for implementation of the FCS-MPC.

Moreover, due to the high computational requirements, practical implementations of predictive control for power converters mainly depend on micro-processing solutions such as digital signal processor (DSP) [18]–[20]. The FCS-MPC algorithm can be implemented with a single prediction horizon that makes it one of the most suitable schemes of MPC due to less computational requirements than other MPC schemes and ease of implementation. However, real-time implementation of FCS-MPC encounters computational delay issues when the number of switching states increases in a power converter (e.g. multilevel converter [33]–[36]) and hence, requires efforts to overcome computational issues. The computations required for the implementation of an algorithm should strictly complete within a given sampling interval. However, delay in the computation of optimum switching state is a concern that deteriorates the quality of waveforms [30], [74]. To cope with this issue, delay compensation techniques have been often used to compute the optimum switching state within the specified sampling

interval [75], [76]. Nevertheless, delay compensation techniques encounter additional issues of an increased computational burden and average switching frequency [75].

Field programmable gate array (FPGA) is a pragmatic choice for the implementation of MPC because of parallel processing capability [21], [77]–[82]. The real-time controller implementation using FPGA requires the hardware description language (HDL) code for the particular system. However, writing specific HDL codes needs special training and hence, it is considered a complex and time-consuming task even for skilled researchers or engineers with an increase in the level of controller complexity [83], [84]. The different alternative ways to get the HDL code of the system have been utilized for the real-time implementation of the MPC. In [77], a comparative analysis among various digital control platforms including FPGA is presented for the implementation of model predictive control and different implementation approach is adopted for FPGA-based system implementation. In [78], an FPGA platform of NI-CRIO reconfigurable system is utilized to implement MPC for a back-to-back converter. The FPGA implementation of MPC is performed using a model-based design (MBD) through MATLAB/Simulink in [79], [80] and the FPGA code was generated with the help of hardware description language (HDL) coder functionality of Simulink. In [81], a high-speed FCS-MPC implementation is presented with a control algorithm coded in C++ using PROTOIP toolbox and HDL code was generated through Xilinx Vivado HLS. Xilinx system generator (XSG) as a digital simulator adopting the MBD platform was used to implement an FPGA-based predictive current controller in [21], [82]–[85].

The XSG platform provides a virtual FPGA environment for the designing, testing, and development of digital controllers. The integrated platform of MATLAB/Simulink-XSG provides the functionality of automatic HDL code generation that can be further utilized for the straightforward implementation of FPGA-based experimental system prototypes without the additional knowledge of HDL programming [86]–[88]. XSG provides a modelling-based design approach for digital system implementation. Therefore, XSG-based system modelling is required for the development of real-time systems using FPGA through automatic HDL code generation. Further, the recent availability of a model-based FPGA design platform integrated with MATLAB/Simulink provides the functionality of hardware-in-the-loop (HIL) co-simulation.

In addition to the implementation approach, FPGA resource utilization is another key aspect of FPGA-based system control implementation. The system control implementation based on FPGA resource utilization is compared in [81] and [82] for Xilinx FPGA. In [81], the prediction horizon is considered for the comparison of FPGA resource utilization. In [82], semi-parallel and fully serial implementation approaches for MPC are adopted and resource utilization is compared for the same. The look-up tables (LUTs), flip-flops and DSP slices are the main digital logic indices that considered for resource utilization in the aforementioned papers. However, a different approach is adopted for FPGA-based control implementation.

There is a possibility to adopt different implementation strategies for a specific FPGA implementation approach to enhance resource utilization. In this way, the MBD approach can be advantageous by allowing different implementation strategies under the same environment and to compare the FPGA resource utilization. Moreover, the MBD approach provides better system visualization and easy debugging that is appealing for rapid controller prototyping.

1.5 Objectives

The various conventional, as well as modern control schemes, have been applied to different power converters for the specific control objectives as discussed in the previous subsections. The control schemes have to deal with various pros and cons, however, every control scheme has its distinctive characteristics that make the particular control scheme more suitable for a specific application. MPC, as a modern control scheme, is used in this study to have an insight into the distinctive characteristics. The objectives that are taken into account and the key contribution of the research are as follows:

The first procedure is to review various literature related to the MPC control applied to different power converters and to search for the issues related to the control. After that, to understand the algorithm of FCS-MPC that is one of the most popular classifications of MPC and to implement it for two-level VSI using MATLAB/Simulink. As the real-time implementation of FCS-MPC is performed on digital platforms, the first objective is to map the control algorithm on to a digital simulator considering an FPGA-based implementation, an alternative way to handle the computational burden of the control algorithm. In order to get a hassle-free HDL code

required for FPGA to perform the real-time implementation, there is a need to develop the controller on to a digital simulator having the functionality of an automatic HDL code generation from the developed controller. XSG, as a digital simulator of Xilinx, is used in this work for the design and development of the controller, however, a modelling-based approach is required for the controller design considering the MBD platform of the XSG. The step-by-step validation with the MATLAB/Simulink design is required through simulations for the precise design.

Before the actual experimental system implementation, an intermediate level of system verification between the software simulation and the actual experimental system implementation using the HIL simulation technique is an effective process that may help to prevent the system failure or any component damage that occurs with direct experimental system implementation. As XSG also provides the functionality of HIL co-simulation, the controller performance is validated in this work using this functionality as well.

The key issue of high switching frequency obtained during FCS-MPC implementation with high sampling frequency for enhanced system performance is also considered in this work. In order to have reduced switching frequency, a constraint for a reduction in the average switching frequency of the converter is incorporated inside the same cost function together with the primary control objectives (voltage or current). In this way, the system can be implemented with a higher sampling frequency depending on the permissible maximum switching frequency of the power devices. The performance of the controller with the constraint aiming switching frequency reduction is validated through the simulation as well as real-time implementation using FPGA.

The performance of the FCS-MPC is highly dependent on the model used for the prediction of the control variables that depend on the system parameters. Any change in system parameters because of any reasons leads to a model parameter mismatch. Considering the issue of model parameter mismatch in the FCS-MPC implementation, an approach is proposed to compensate for the effect of change in model parameters during physical system implementation. The performance is verified through the simulation and experimental results.

Apart from the issue of model parameter mismatch in the FCS-MPC, an issue of a non-zero steady-state error (SSE) is a concern for the FCS-MPC. This error is more

prominent when the system is operated with lower switching frequency or lower reference currents. The functionality of constraint inclusion inside a single cost function has been normally used to control the additional parameters together with the primary control parameters, however, the dedicated constraints are required to handle the individual objectives. In this work, a modified cost function based on a novel constraint is proposed considering the improvement in SSE together with a reduction in the switching frequency. To validate the effectiveness of the proposed constraint, a comparative analysis is presented with the constraint of a change in switching state.

The FPGA resource utilization is another key aspect of the FPGA-based system control implementation considering an optimum design and development of the controller to reduce the overall resource requirements. Considering the same issue, there is a need to analyze the design by incorporating different implementation strategies aiming reduction in the overall FPGA resource utilization. An analytical approach based on implementation strategies using the MBD approach is adopted in this study to determine the appropriate strategy considering a reduction on FPGA resources.

1.6 Organization and Overview

The dissertation is divided into the following chapters:

Chapter 1: Introduction

This chapter presents an overview of world energy demand and future challenges, role of power electronics to fulfill the energy demand and to solve energy issues, the different control schemes used to handle the various control objectives of the power electronic converters, and applications of model predictive control (MPC) in power electronics that is the main controller used in this work. Moreover, detailed literature background of finite control set-MPC (FCS-MPC) with the fundamental concepts is presented including the objectives of the dissertation.

Chapter 2: Finite control set-model predictive control

This chapter presents the working principle of the FCS-MPC algorithm including the formulation of the discrete-time model of a three-phase two-level voltage source inverter (VSI). The predictive model and design of cost function for load current control of the three-phase VSI are presented for the FCS-MPC in stationary $\alpha\beta$ as well

as rotating *dq* coordinates. The modelling and implementation of the FCS-MPC in both frames are discussed in the next chapter.

Chapter 3: Model-based controller design and HIL simulation

A model-based design (MBD) approach for the design and development of the FCS-MPC algorithm is presented in this chapter. Moreover, the controller design in a digital simulator of the Xilinx system generator (XSG) is presented considering the straightforward FPGA-based system implementation. After the controller developed in XSG, the controller performance is validated through the simulation results and a comparative analysis is presented with the controller developed in MATLAB/Simulink.

This chapter also presents the hardware-in-the-loop (HIL) simulation methodology to validate the digitally developed controller. The controller performance is further verified through the experiment conducted with FPGA-based system implementation. The system implementation without any constraint is considered in this chapter considering the only primary objective of the load current control of the three-phase VSI system. The results obtained through the real-time experiments are compared with the results obtained through the HIL simulation for the proper validation of the experimental results.

Chapter 4: Advanced FCS-MPC: Adaptive predictive model and modified cost function

This chapter presents an approach to compensate for the effect of any system parameter mismatch that occurred during the real-time system implementation. To update the predictive model, the effect of a change in load resistance is considered and the model is named as an adaptive predictive model. The system performance with the adaptive predictive model is validated and a comparative analysis is presented considering an exact and approximated model of the system. The performance is also investigated with the constraint of a switching frequency reduction. The system performance is verified through the simulation as well as experimental results considering the performance indices: THD in load current and average switching frequency.

The novel constraint for the reduction in steady-state error as well as switching frequency is also proposed in this chapter. A simplified FCS-MPC is utilized considering the reduction in computational complexity and the optimization function is designed based on the reference voltage vector. A constraint of change in reference

voltage vector is proposed in this chapter and a comparative analysis with the constraint of a change in switching state is performed for the validation of the steady-state error reduction.

Chapter 5: FPGA resource optimization

This chapter describes the digital logic resources utilized in the FPGA-based system design including the fundamental FPGA architecture. An analytical approach to reduce the overall FPGA resource requirements is presents in this chapter. Moreover, in-depth analysis of the system implementation with the fixed, approximated and adaptive values of the coefficient used in current prediction is presented. Furthermore, a comparative analysis with different implementation strategies is presented for the selection of the optimum design with respect to the system performance.

Chapter 6: Conclusions and future work

The conclusions of the work presented in the dissertation and the possibility of future research work followed by the presented work are mentioned in this chapter.

Chapter 2

FINITE CONTROL SET – MODEL PREDICTIVE CONTROL

2.1 Fundamental Principle

Finite control set-model predictive control (FCS-MPC) is one of the most trendy control schemes of the wide family of model predictive control (MPC). It is characterized by the use of a discrete-time model of the system to predict the future behavior of the variables to be controlled based on the possible switching states of the power converter. The FCS-MPC does not require a cascaded structure of the control loop and does not need a modulator to generate switching signals of the power switches.

The system is considered as a finite set of linear discrete-time models corresponding to the finite switching states. These models are used for the prediction of the future behavior of controlled variables for each switching state to determine the optimum actuation in each sampling interval to achieve the control objectives. The control objectives are governed by a predefined objective function or cost function that is formulated considering controlled variables and desired references. The optimum actuation is selected according to the minimum cost function in each sampling interval and directly applied to the power converter.

The block diagram of a general FCS-MPC scheme applied to power converters and drives is depicted in Fig. 2.1. The power converter shown in the figure can be of any one of the power converter topologies and any number of phases. The generic load in the figure can be represented by any form of electrical load such as passive load, active load, electrical

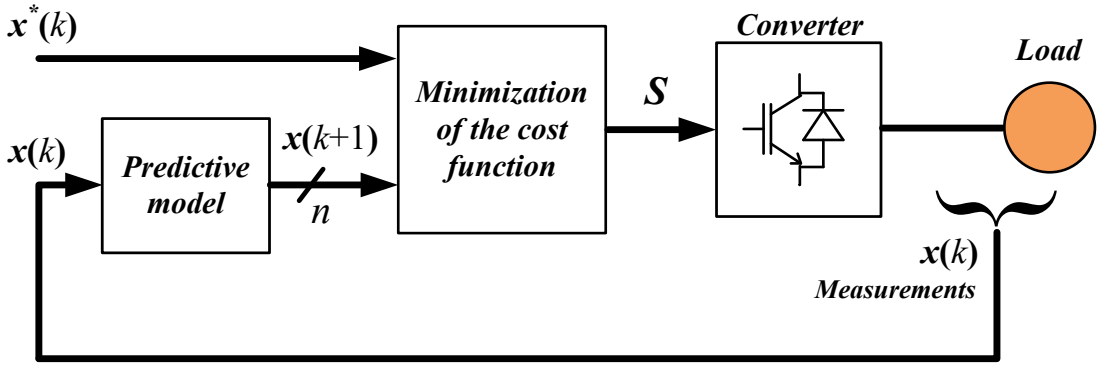


Fig. 2. 1. General block diagram of the FCS-MPC scheme for power converters [32].

machine, and the grid. In the FCS-MPC scheme, a sampled form of measured variables $x(k)$ is used in the model to calculate predicted controlled variables $x(k+1)$ for each one of the n possible actuations, that is, switching states, voltages, or currents. After the completion of the prediction step, the values of the corresponding cost functions are evaluated with respect to the error between the predicted $x(k+1)$ and reference values $x^*(k)$. Finally, the optimum actuation $\boldsymbol{S}$ is selected corresponding to the minimum cost function and applied to the converter.

2.1.1 System model

In FCS-MPC, the converter is considered as a finite set of linear models, where each model is treated with a specified switching state. In each phase arm (leg) of a power converter, there are two power switches and both switches operates in a complementary fashion, that is, when the upper switch will be turned *on* (state '1'), the lower switch will be turned *off* (state '0') and vice-versa. The number of possible switching combinations or switching states of a power converter is given by

$$N = 2^m \tag{2.1}$$

where N is the number of switching states and m is the number of converter legs. If, for instance, a full-bridge converter is used, there are two legs ($m = 2$) and hence, $N = 2^2 = 4$. Similarly, there are 3 legs ($m = 3$) in a two-level three-phase VSI, and hence, $N = 2^3 = 8$.

The model of a system is defined by deriving equations that describe the dynamic behavior of the controlled variables. In power electronics, when choosing voltages,

currents, flux linkages as state and output variables, the system is usually modelled by a linear continuous-time state-space representation as

$$\frac{dx(t)}{dt} = \boldsymbol{A}_c x(t) + \boldsymbol{B}_c u(t) \tag{2.2a}$$

$$y(t) = \boldsymbol{C}_c x(t) + \boldsymbol{D}_c u(t) \tag{2.2b}$$

where $\boldsymbol{A}_c$, $\boldsymbol{B}_c$, $\boldsymbol{C}_c$, and $\boldsymbol{D}_c$ are the system matrix, input matrix, output matrix, and any system disturbance matrix respectively.

The FCS-MPC algorithm is formulated in the discrete-time domain using a constant sampling interval T_S. The value of state variables is restricted to change only at discrete sampling instants, that is, at the time instant $t = kT_S$, where $k = 0, 1, 2,\ldots\ldots N_S$ (number of samples) denotes the time steps. The discrete-time state-space representation can be easily computed by integrating (2.2a) from $t = kT_S$ to $t = (k+1)T_S$ and maintaining constant $u(t)$ during this time interval and equal to $u(k)$. The resulting discrete-time state-space equation is expressed as

$$x(k+1) = \boldsymbol{A}_d x(k) + \boldsymbol{B}_d u(k) \tag{2.3a}$$

$$y(k) = \boldsymbol{C}_d x(k) + \boldsymbol{D}_d u(k) \tag{2.3b}$$

where discrete-time state-space matrices $\boldsymbol{A}_d$, $\boldsymbol{B}_d$, $\boldsymbol{C}_d$, and $\boldsymbol{D}_d$ can be computed from their continuous-time counterparts and formulated as

$$\boldsymbol{A}_d = e^{\boldsymbol{A}_c T_S} \tag{2.4a}$$

$$\boldsymbol{B}_d = \int_0^{T_S} e^{\boldsymbol{A}_c \tau} \boldsymbol{B}_c d\tau \tag{2.4b}$$

$$\boldsymbol{C}_d = \boldsymbol{C}_c \tag{2.4c}$$

$$\boldsymbol{D}_d = \boldsymbol{D}_c \tag{2.4d}$$

The discrete-time state-space representation (2.3a) is further used as the predictive model for the calculation of the future values of the controlled sate variables.

2.1.2 Cost function design

The cost function describes an objective function that considers each control variable or system parameter. The additional control parameters or constraints can be incorporated inside a single cost function simultaneously with the primary control parameters such as voltage, current, torque or flux [83]. However, handling of two or more parameters inside a single cost function is not an easy task because of the non-identical nature of parameters like different units and different magnitudes. Any additional control parameter can be managed inside a cost function using a multiplying factor called the weighting factor which is used for the tuning of the additional parameter with the other control parameters. Hence, the general form of a cost function is as follows

$$g = \sum_{n=1}^{l} \lambda_n \left| x_n^* - x_n^p \right| + \sum_{n=l+1}^{m} \lambda_n C_n, \quad n < l < m \tag{2.5}$$

where λ_n is the weighting factor associated with each term, x_n^* is the desired reference input, x_n^p is the predicted value of the controlled state variables, and C_n is any additional constraints. The first two terms denote a reference tracking by evaluating the respective tracking errors. The examples of reference tracking with respect to the power converter and drive are the objectives to control current, voltage, power, torque and speed.

The tracking error is defined as the distance between the reference and the predicted state variables. It can be formulated using absolute value or the squared value of the error. In this case, the cost function can be expressed as

$$g = \left| x^* - x^p \right| \qquad \text{(absolute value)} \tag{2.6}$$

$$g = \left(x^* - x^p \right)^2 \qquad \text{(squared value)} \tag{2.7}$$

When the cost function contains only one control objective, the system performance will be similar for the absolute value and squared value error. However, when more than two control variables are incorporated inside a cost function, the squared value error performs better tracking and reduced ripple [32].

The next section describes the current control application of the FCS-MPC in a two-level three-phase VSI system.

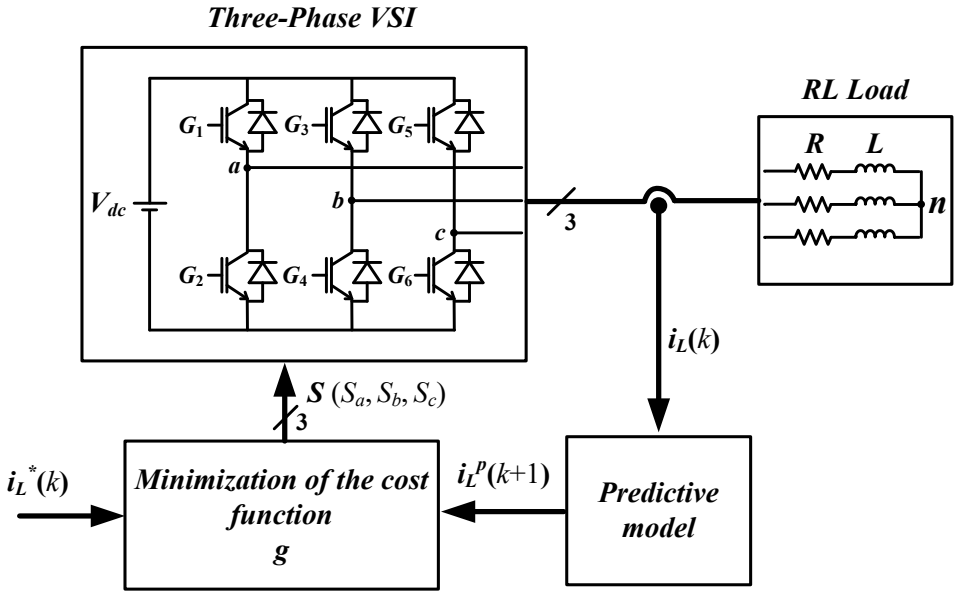


Fig. 2. 2. Schematic diagram for the current control of three-phase VSI using FCS-MPC [83].

2.2 Current Control of Three-Phase VSI

The block diagram of the FCS-MPC applied to a two-level three-phase VSI for the control of the load current is shown in Fig. 2.2. The steps of current control using FCS-MPC is as follows:

- The load side three-phase current $\boldsymbol{i_L}(k)$ at the k^{th} sampling interval is measured and provided to the predictive model for the prediction of the future variables.
- The discrete-time model of the inverter system is used to predict the value of the load current in the $(k+1)^{\text{th}}$ sampling interval for each of the possible switching states of the inverter.
- The value of cost function g is evaluated for all the predicted load currents based on the error between predicted load current $\boldsymbol{i}_L{}^p(k+1)$ and desired reference current $\boldsymbol{i}_L{}^*(k)$, obtained from an outer control loop.
- According to the minimum cost function, the optimum switching state is selected and applied to the inverter in the next sampling interval.

The cost function for only one control objective, that is, load current control can be expressed using absolute value error as

$$g = \left| \boldsymbol{i}_L^* - \boldsymbol{i}_L^p \right| \tag{2.8}$$

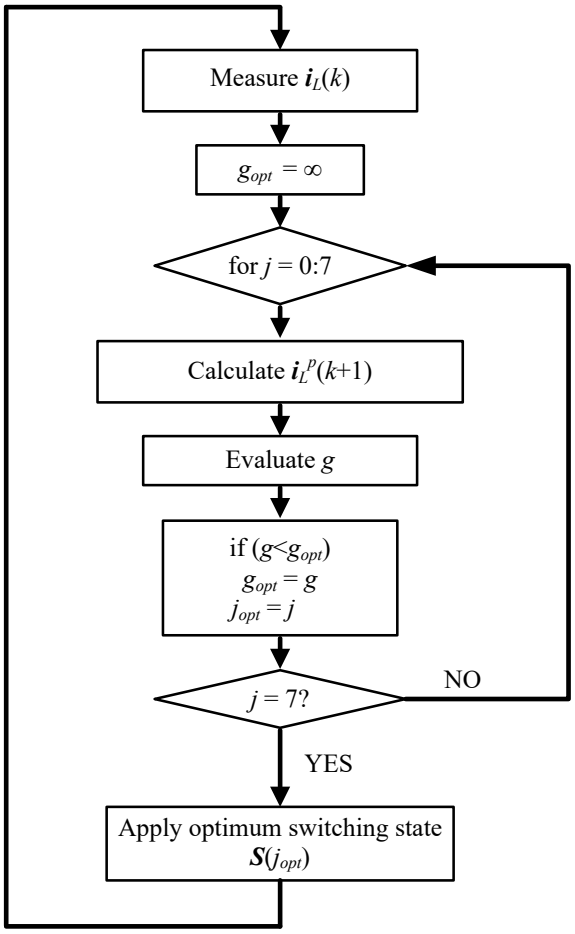


Fig. 2. 3. A flow diagram representing the control algorithm of the FCS-MPC [32].

The control algorithm is also represented as a flow diagram shown in Fig. 2.3. According to the diagram, the outer loop is executed in each sampling interval, and the inner loop is executed for each possible switching state to obtain the optimum switching state to be applied to the power converter during the next sampling period.

2.2.1 Three-phase VSI system model

The power circuit of a three-phase VSI system in Fig. 2.4 consists of a three-phase RL load and a dc supply to the VSI, where V_{dc} is the dc voltage; v_{aN}, v_{bN}, and v_{cN} are the phase-to-neutral voltages of the inverter; i_{La}, i_{Lb}, and i_{Lc} are the load currents; R is the load resistance; L is the load inductance. The three-phase VSI consists of three legs (a, b, and c) with two power switches (e.g. IGBT) in each leg: G_1-G_2 (leg 'a'), G_3-G_4 (leg 'b') and G_5-G_6 (leg 'c'). G_1, G_3, G_5 are termed as upper switches and G_2, G_4, G_6 lower switches.

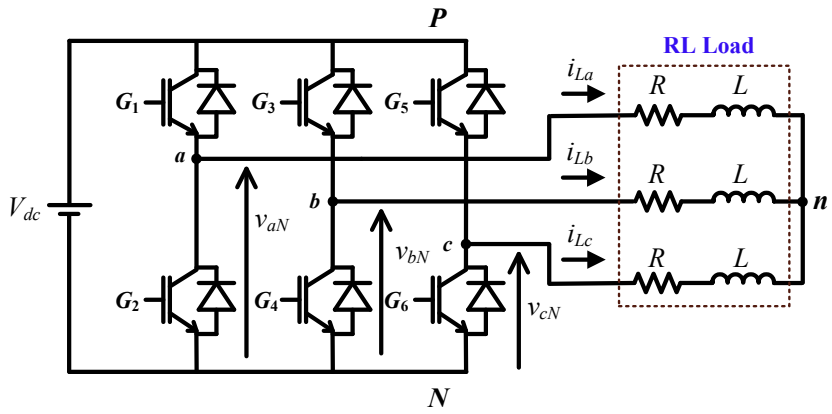


Fig. 2. 4. Schematic diagram for the current control of three-phase VSI using FCS-MPC.

Table 2. 1. Gating signals of inverter power switches.

Leg a, S_a	Leg b, S_b	Leg c, S_c
G_1 ON, 1	G_3 ON, 1	G_5 ON, 1
G_2 OFF, 0	G_4 OFF, 0	G_6 OFF, 0
G_1 OFF, 0	G_3 OFF, 0	G_5 OFF, 0
G_2 ON, 1	G_4 ON, 1	G_6 ON, 1

2.2.1.1 Inverter model

Switching states of VSI are interpreted corresponding to the switching signals applied to the upper and lower switches that are complementary to each other. The switching states S_a, S_b, S_c in Table 2.1 denotes the switching signals applied to the power switches corresponding to three legs. The switching states $\boldsymbol{S}$ can be expressed in vector form as

$$\boldsymbol{S} = \frac{2}{3}\left(S_a + e^{j(2\pi/3)}S_b + e^{j(4\pi/3)}S_c\right) \tag{2.9}$$

The output voltage space vectors generated by the inverter are defined by

$$\boldsymbol{v} = \frac{2}{3}\left(v_{aN} + e^{j(2\pi/3)}v_{bN} + e^{j(4\pi/3)}v_{cN}\right) \tag{2.10}$$

Then, the load voltage vector $\boldsymbol{v}$ can be related to the switching state vector $\boldsymbol{S}$ by

$$\boldsymbol{v} = \boldsymbol{S}V_{dc} \tag{2.11}$$

Considering all possible switching combinations of gating signals, eight switching states and hence, eight voltage vectors are obtained as shown in Table 2.2. The two voltage

Table 2. 2. Switching states and voltage vectors.

Switching states				Voltage vectors	Index number
$\boldsymbol{S}$	S_a	S_b	S_c	$\boldsymbol{v}$	
$\boldsymbol{S}_0$	0	0	0	$\boldsymbol{v}_0 = 0$	0
$\boldsymbol{S}_1$	1	0	0	$\boldsymbol{v}_1 = 2V_{dc}/3$	4
$\boldsymbol{S}_2$	1	1	0	$\boldsymbol{v}_2 = V_{dc}/3 + j\sqrt{3}V_{dc}/3$	6
$\boldsymbol{S}_3$	0	1	0	$\boldsymbol{v}_3 = -V_{dc}/3 + j\sqrt{3}V_{dc}/3$	2
$\boldsymbol{S}_4$	0	1	1	$\boldsymbol{v}_4 = -2V_{dc}/3$	3
$\boldsymbol{S}_5$	0	0	1	$\boldsymbol{v}_5 = -V_{dc}/3 - j\sqrt{3}V_{dc}/3$	1
$\boldsymbol{S}_6$	1	0	1	$\boldsymbol{v}_6 = V_{dc}/3 - j\sqrt{3}V_{dc}/3$	5
$\boldsymbol{S}_7$	1	1	1	$\boldsymbol{v}_7 = 0$	7

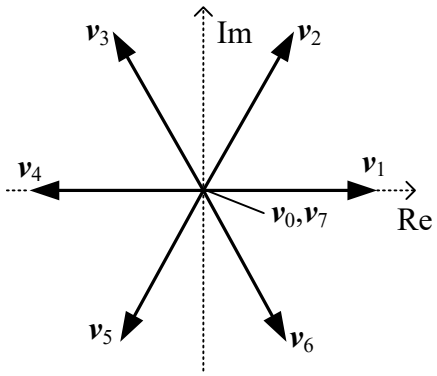


Fig. 2. 5. Voltage vectors generated by the inverter.

vectors $\boldsymbol{v}_0$ and $\boldsymbol{v}_7$ are the same, resulting in only seven different voltage vectors, as shown in Fig. 2.5.

2.2.1.2 Load model

For the balance three-phase RL load, the load current can be defined using a space vector form as follows

$$\boldsymbol{i}_L = \frac{2}{3}\left(i_{La} + e^{j(2\pi/3)} i_{Lb} + e^{j(4\pi/3)} i_{Lc}\right) \tag{2.12}$$

The load current dynamics can be described by a simple vector equation as given below

$$\boldsymbol{v} = R\boldsymbol{i}_L + L\frac{d\boldsymbol{i}_L}{dt} \tag{2.13}$$

2.2.1.3 Discrete-time model

The load current dynamics (2.13) defines a continuous-time model and a discrete-time model can be obtained by discretization of the continuous-time model for a sampling time T_S. Forward-Euler approximation method is one of the simplest discretization methods that gives an approximated value of the derivative $d\boldsymbol{i}_L/dt$ as

$$\frac{d\boldsymbol{i}_L}{dt} \approx \frac{\boldsymbol{i}_L(k+1)-\boldsymbol{i}_L(k)}{T_S} \tag{2.14}$$

After substituting (2.14) into (2.13), an expression of the predicted future load current at the next sampling interval $k + 1$ can be obtained as

$$\boldsymbol{i}_L(k+1)=\left(1-\frac{RT_S}{L}\right)\boldsymbol{i}_L(k)+\frac{T_S}{L}\boldsymbol{v}(k) \tag{2.15}$$

where $\boldsymbol{i}_L(k+1)$ denotes the predicted future load currents at time $k+1$, $\boldsymbol{i}_L(k)$ is the measured load currents at instant k and the inverter voltage $\boldsymbol{v}(k)$ is the decision variable to be calculated by the controller. The discrete-time model (2.15) represents a predictive model and is used for the future predictions of the load current from each voltage vectors and the measured load currents at the present sampling instant k.

For the simplicity and to reduce a computational burden, the FCS-MPC algorithm is normally implemented in a stationary $\alpha\beta$-frame by representing the current and voltage vectors as

$$\boldsymbol{i}_L=\begin{bmatrix} i_{L\alpha} & i_{L\beta}\end{bmatrix}^T \qquad \boldsymbol{v}=\begin{bmatrix} v_\alpha & v_\beta\end{bmatrix}^T \tag{2.16}$$

1. Predictive model in $\alpha\beta$-frame

After substituting the value of current and voltage vectors (2.16) into (2.15), the predictive model in $\alpha\beta$ frame can be formulated as

$$\begin{aligned} i_{L\alpha}^{p}(k+1) &= k_1 i_{L\alpha}(k)+k_2 v_\alpha(k) \\ i_{L\beta}^{p}(k+1) &= k_1 i_{L\beta}(k)+k_2 v_\beta(k) \end{aligned} \tag{2.17}$$

where $k_1=\left(1-\frac{RT_S}{L}\right)$, $k_2=\frac{T_S}{L}$

$i_{L\alpha}(k)$, $i_{L\beta}(k)$ and $i^p_{L\alpha}(k+1)$, $i^p_{L\beta}(k+1)$ denote the measured load currents at instant k and the predicted future load currents at instant $k+1$, respectively.

The coordinate transformations from three-phase *abc* to stationary $\alpha\beta$ are computed using mathematical relation defined by Clarke transformation given as

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.18}$$

where x can be any quantity voltage or current.

2. Predictive model in dq-frame

The predicted load currents in rotating dq-frame considering feed-forward terms for the decoupling of the d and q components of the current using forward Euler discretization is given below

$$\begin{aligned} i^p_{Ld}(k+1) &= k_1 i_{Ld}(k) + k_2 \left\{ v_d(k) + k_3 i_{Lq}(k) \right\} \\ i^p_{Lq}(k+1) &= k_1 i_{Lq}(k) + k_2 \left\{ v_q(k) - k_3 i_{Ld}(k) \right\} \end{aligned} \tag{2.19}$$

where $k_1 = \left(1 - \frac{RT_S}{L}\right)$, $k_2 = \frac{T_S}{L}$, $k_3 = \omega^* L$

ω^* is an angular frequency of the current reference. The voltages v_d, v_q and currents i_{Ld}, i_{Lq} can be computed using Park transformation relation to get dq from $\alpha\beta$ components given as

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos\theta^* & \sin\theta^* \\ -\sin\theta^* & \cos\theta^* \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{2.20}$$

where θ^* is the reference phase angle for the coordinate conversion.

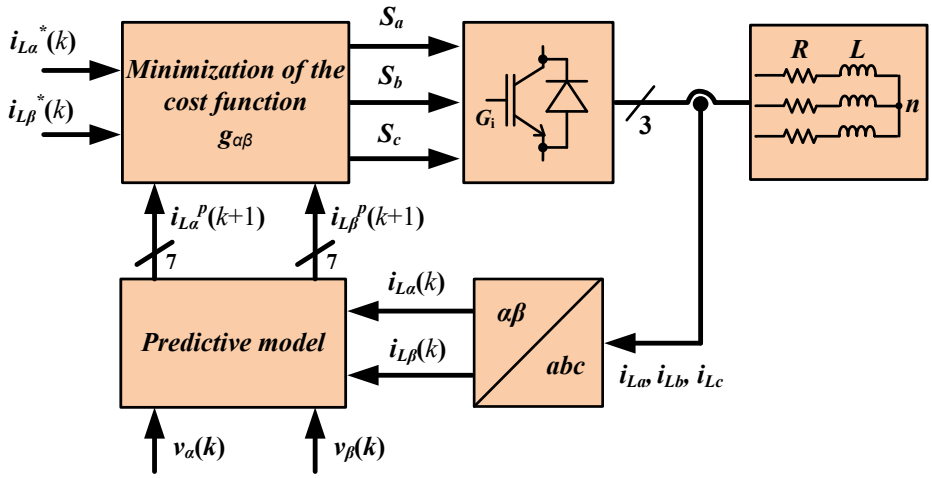
2.2.2 Cost function

The appropriate cost functions to perform load current reference tracking using the predictive model in $\alpha\beta$ as well as dq frames are summarized here.

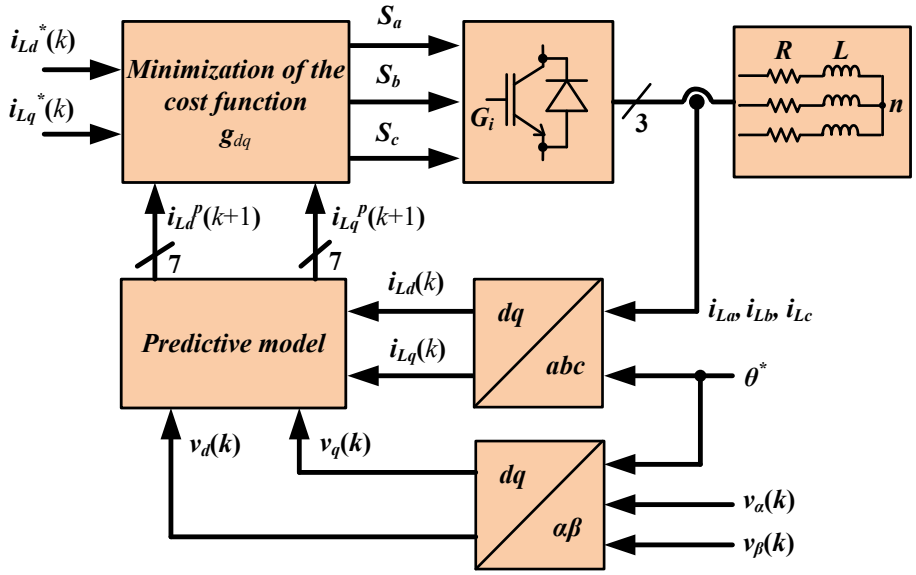
1. Cost function in $\alpha\beta$-frame

A simple cost function is represented in $\alpha\beta$-frame using the predictive model in (2.17) as

$$g_{\alpha\beta} = \left| i^*_{L\alpha}(k+1) - i^p_{L\alpha}(k+1) \right| + \left| i^*_{L\beta}(k+1) - i^p_{L\beta}(k+1) \right| \tag{2.21}$$



(a)



(b)

Fig. 2. 6. A schematic diagram representing the load current control using the FCS-MPC in (a) $\alpha\beta$-frame, and (b) dq-frame.

where $i^*_{L\alpha}$ and $i^*_{L\beta}$ are the real and imaginary components of the reference load current. The future reference current value required by (2.24) can be predicted using the Lagrange extrapolation method discussed in [30]. However, for sufficient small T_S, a simple approximation $i^*_L(k+1) \approx i^*_L(k)$ can be adopted and the additional complex extrapolation process can be omitted. The same approximation is considered in this work.

2. Cost function in *dq*-frame

A cost function to control the load current using the predictive model in *dq*-frame (2.19) can be represented as

$$g_{dq} = \left|i^*_{Ld}(k+1) - i^p_{Ld}(k+1)\right| + \left|i^*_{Lq}(k+1) - i^p_{Lq}(k+1)\right| \tag{2.22}$$

where i^*_{Ld} and i^*_{Lq} are the reference load currents in *d* and *q* components respectively.

The schematic block diagram representing the load current control using the FCS-MPC in *αβ*-frame and *dq*-frame is depicted in Fig. 2.6 (a) and 2.6 (b), respectively.

2.3 Summary

The FCS-MPC is one of the most utilized control schemes of the MPC categories. The fundamental concept behind the FCS-MPC algorithm is to use a discrete-time model (predictive model) of the power converter system to predict the future values of the controlled variables and to utilize the advantages of the limited number of switching states of a power converter.

An objective function or a cost function is designed considering each prediction of control variables including any system constraint. In every sampling interval, the calculation of prediction and simultaneous cost computation is performed corresponding to each possible switching state. The optimum switching state is selected according to the minimum cost function in each sampling and directly applied to the power converter switches.

The application of the FCS-MPC scheme is described for the load current control of a two-level three-phase VSI system. The FCS-MPC algorithm is formulated in the stationary *αβ* as well as rotating *dq* coordinates. The predictive models are represented in (2.17) and (2.19) for the *αβ* and *dq* coordinates, respectively considering a fixed value of load parameters for the calculation of coefficients.

The next chapter describes the design and development of the FCS-MPC algorithm for the load current control of the three-phase VSI system implementation through a digital platform.

Chapter 3

MODEL-BASED DESIGN AND HIL SIMULATION

3.1 Introduction

The practical implementations of predictive controls for power converters mainly depend on micro-processing solutions such as digital signal processor (DSP), a software-based control [18-20], [32] due to the large computational requirements. These micro-programmable solutions have advantages such as simple circuitry, software-based control, and flexible control adaptability to different applications. The computation required for the algorithm should strictly complete within a given sampling interval. However, delay in the computation of the optimum switching state has been observed that deteriorates the quality of waveforms [30], [74]. To cope with this issue, delay compensation techniques are necessary to compute optimum switching state within the specified sampling interval [75], [76]. Nevertheless, delay compensation techniques encounter additional issues of increased computational burden and an increased average switching frequency [75].

Field programmable gate array (FPGA) is a solution of choice because of parallel processing capability [21], [77-82] and in addition, the possibility to determine accurate latency at each computational step. Further, the FPGA-based system implementation makes system compact, cost-effective for controller prototyping and flexibility of functional interfacing of devices of our own choices due to its characteristics of configurability and programmability. However, the system implementation using FPGA requires specific programming skills in the hardware description language (HDL) that leads to the tedious and time-consuming controller development process and considered more cumbersome with an increase in the level of controller complexity [79], [82].

The controller development approach is crucial for real-time implementation considering the FPGA-based real-time system implementation with an aspect of the straightforward utilization of the product in industrial applications. The digital simulator as a realistic virtual FPGA platform is advantageous considering the controller development process that facilitates an automatic code generation through the developed system to ease the FPGA-based system implementation.

The Xilinx system generator (XSG) as a digital simulator provides a virtual FPGA environment for the designing, testing, and development of digital controllers. The integrated platform of MATLAB/Simulink-XSG provides the functionality of automatic HDL code generation through the developed system for the FPGA [86-88]. However, XSG a model-based design (MBD) platform for digital system implementation that requires system modelling at the initial stage. In this work, the FCS-MPC algorithm is developed through the MBD approach for the FPGA-based system implementation. Furthermore, a hardware-in-the-loop (HIL) technique is used for the validation of the developed controller before the actual experimental system implementation.

3.1.1 MBD approach

Model-based design (MBD) is a technique that consists of designing models using elementary mathematical building blocks (continuous-time as well as discrete-time) and using these models for the analysis and designing of complex systems [89]. The traditional design methodology is based on the extensive software code which is difficult to design and understand (e.g. debugging, designing the architecture, reducing the complexity and then testing). However, the MBD approach facilitates the design of a complex controller through a step-by-step system development by analyzing the intermediate outputs during the simulation that provides easy debugging. Hence, it provides a platform for rapid system development and prototyping that is a fast and cost-effective way to control signal processing and verify design at an early stage. The controller can be modified and upgraded rapidly according to the system requirements with easy expansion capabilities.

MBD is an efficient approach for the designing of embedded systems, control systems, communication systems, and signal processing systems [89] [90]. The MBD approach has been using in industrial control, motion control, aerospace, and automotive applications

[89]. Effective use of the MBD approach for system design provides a single design platform to optimize the overall system design.

The XSG, an MBD platform for the development of digital controllers is used for the FPGA design. The integrated platform of MATLAB/Simulink-XSG provides an additional Xilinx blockset in the Simulink library. The integrated platform facilitates an automatic HDL code generation that can be further utilized for the straightforward implementation of the FPGA-based experimental system. Moreover, the integrated platform of MATLAB/Simulink-XSG provides the functionality of HIL co-simulation.

3.1.2 HIL Overview

HIL simulation is a technique for validating the controller by creating a virtual real-time environment that represents the physical system to be controlled [91]. It helps to test the behavior of the control algorithm without physical prototypes. HIL simulation is considered as an intermediate level of system verification approach between the software simulation and implementation of the controller on the actual experimental system [92]–[94]. Before the actual experimental system implementation, system verification using the HIL simulation technique is an effective process that may help to prevent the system failure or any component damage that occurs with direct experimental system implementation. Hence, it is the most suitable technique for testing a controller where the real physical system is expensive or dangerous. This technique is widely used in the automotive, machinery industries, aerospace and defense applications [95].

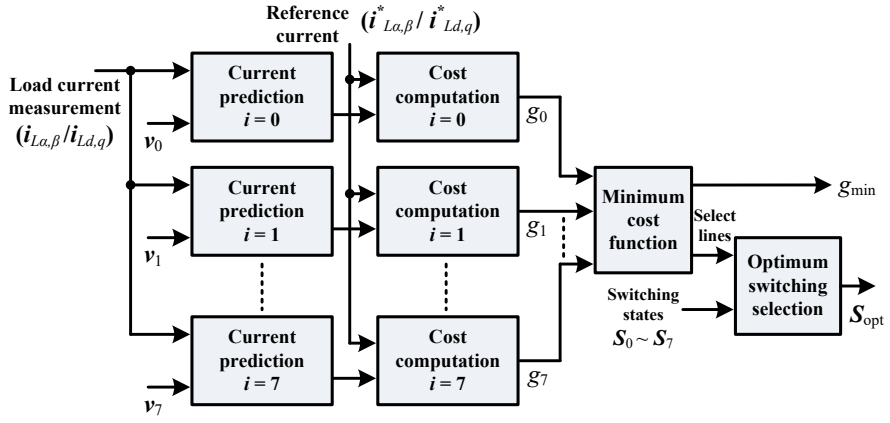


Fig. 3. 1. Schematic diagram for the current control of three-phase VSI using FCS-MPC.

3.2 Modelling of FCS-MPC Algorithm

The modelling of the control algorithm of the FCS-MPC is performed using fundamental mathematical blocks. At the initial stage, the FCS-MPC is developed in MATLAB/Simulink using Simulink blockset. Then, the implemented controller in the MATLAB/Simulink platform is modelled in the digital platform of XSG using Xilinx blockset in Simulink.

The modelling of the FCS-MPC is performed based on the schematic diagram shown in Fig. 3.1. This is a fully parallel implementation approach and the control algorithm is divided into three steps: prediction of future load currents, computation of cost functions, and selection of optimum switching state. The steps for modelling of the controller are described in the following subsections.

3.2.1 Computation of cost function

The cost function is computed using the predictive model which describes the discrete-time mathematical equations for the FCS-MPC in $\alpha\beta$-frame (2.17) as well as dq-frames (2.19) mentioned in chapter 2. The modelling for the computation of cost function is performed using fundamental mathematical blocks as shown in Fig. 3.2, a block diagram representation, considering a voltage vector (for ex. $\boldsymbol{v}_3$) for the FCS-MPC in $\alpha\beta$-frame. In the digital platform of XSG, the modelling of the cost computation is demonstrated in

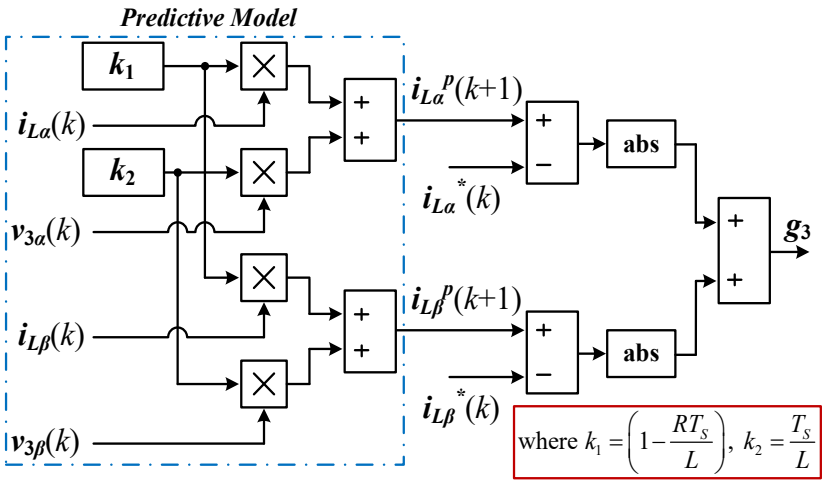


Fig. 3. 2. Block diagram to demonstrate the modelling steps in the cost function computation for the FCS-MPC in $\alpha\beta$-frame.

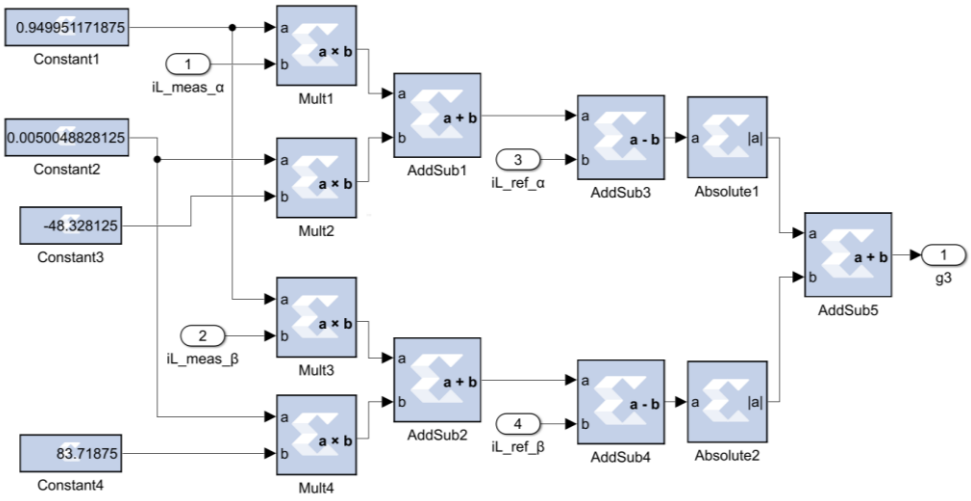


Fig. 3. 3. The modelling steps for the cost function computation developed in the digital platform of XSG for the FCS-MPC in $\alpha\beta$-frame.

Fig. 3.3 using basic mathematical Xilinx blockset (Constant, AddSub, Mult, and Absolute). The modelling for the calculation of predicted load currents and the computation of cost function is demonstrated for the FCS-MPC in $\alpha\beta$-frame using (2.17) and (2.21), respectively.

Similarly, a block diagram in Fig. 3.4 represents the modelling steps for the cost computation using the predictive model in the dq-frame of the FCS-MPC for the same voltage vector ($\boldsymbol{v}_3$) and further modelling in XSG is demonstrated in Fig. 3.5. The modelling for the load current prediction and the cost function computation is performed

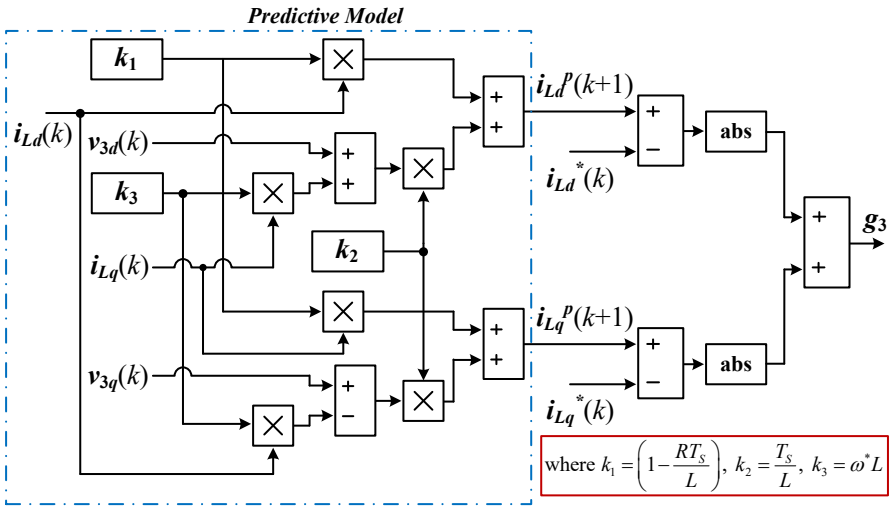


Fig. 3. 4. Block diagram to demonstrate the modelling steps in the cost function computation for the FCS-MPC in dq-frame.

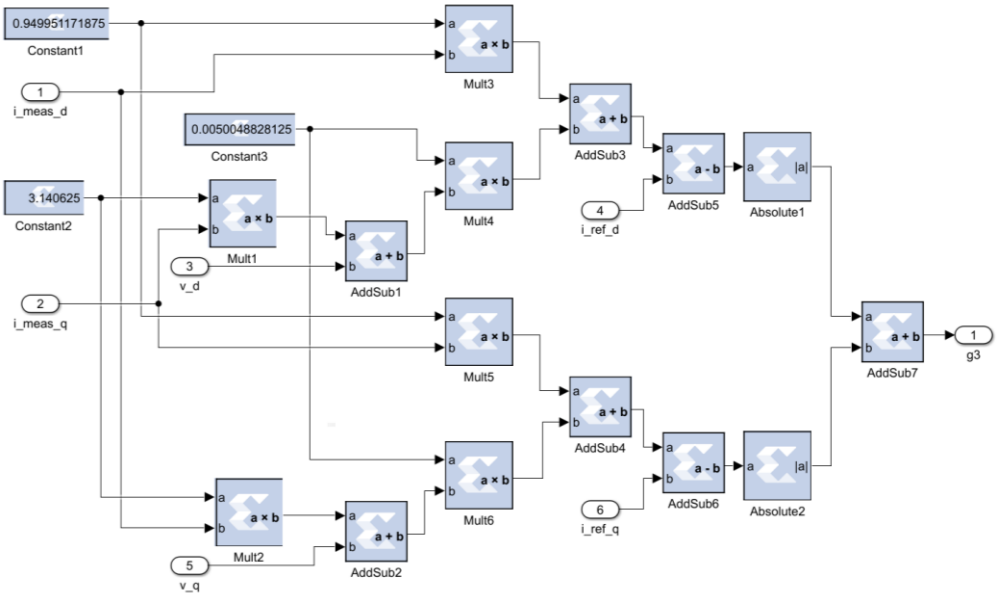


Fig. 3. 5. The modelling steps for the cost function computation developed in the digital platform of XSG for the FCS-MPC in *dq*-frame.

using (2.19) and (2.22) respectively for the FCS-MPC in *dq*-frame.

Although only a single voltage vector ($\boldsymbol{v}_3$) is considered for the demonstration of the modelling steps during the computation of cost function, the cost functions need to be computed for each inverter voltage vectors ($\boldsymbol{v}_0$ – $\boldsymbol{v}_7$) defined for corresponding switching states (S_a, S_b, S_c) as given in Table 2.2 (chapter 2) to select minimum cost function in each sampling interval.

3.2.2 Selection of optimum switching state

The block diagram for the selection of an optimum switching state $\boldsymbol{S}_{opt}$ corresponding to the minimum cost function g_{min} for each sampling interval is shown in Fig. 3.6. A simple pipelining method is used to find the minimum among the computed cost functions. A logic to select a minimum between two consecutive cost functions is developed using a comparator (C) and a 2:1 multiplexer (M). The output of the comparators (binary digit '0' or '1') are used as select lines (sel_0~sel_6) for the multiplexers in the combined C&M (C&M0 ~ C&M6) to select the minimum cost function (g_{m0}~g_{m6}) out of the two as shown in Fig. 3.6 (a). Similar to the selection of g_{min}, an optimum switching state $\boldsymbol{S}_{opt}$ is selected using the corresponding select lines (sel_0~sel_6) fed to the multiplexers (M0 ~ M6) by taking consecutive two switching states as shown in Fig. 3.6 (b).

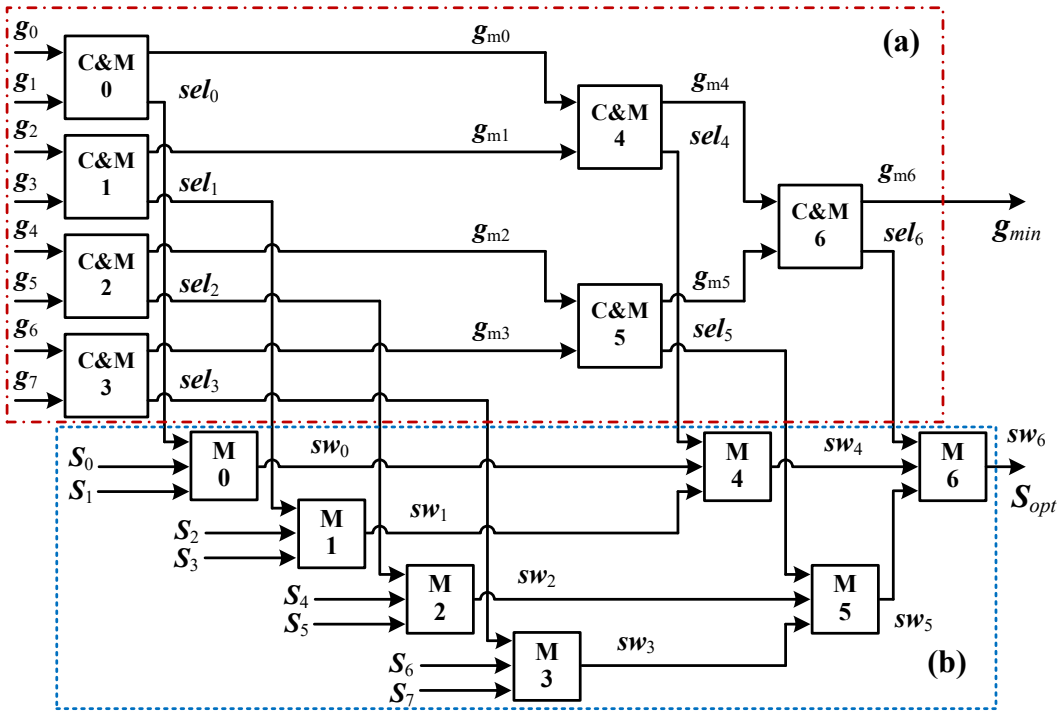


Fig. 3. 6. Block diagram to represent logic for the (a) selection of minimum of cost function, and (b) selection of optimum switching state.

3.2.3 Generation of switching signal and index number

The switching signals corresponding to selected $\boldsymbol{S}_{opt}$ is also generated through modelling. The 3-bit binary combination of $\boldsymbol{S}_{opt}$ is sliced to generate switching signals for respective upper switches (G_1, G_3, G_5). And, complementary switching conditions are applied to lower switches (G_2, G_4, G_6).

An index number is considered for an in-depth analysis purpose corresponding to eight possible voltage vectors ($\boldsymbol{v}_0$~$\boldsymbol{v}_7$) as mentioned in Table 2.2. The index numbers are defined considering the decimal equivalent of the binary values of S_a, S_b, S_c. For example, the index number is defined as '4' corresponding to $\boldsymbol{v}_1$ having {S_a, S_b, S_c} as {1, 0, 0}. The $\boldsymbol{S}_{opt}$ corresponding to the g_{min} is used to select an index number that replicates the definite switching state selection in each sampling time.

The complete FCS-MPC algorithm modelled in the digital platform of XSG is depicted in Fig. 3.7. Part (a) is a subsystem that contains the modelling of cost functions according to different voltage vectors. Part (b) is a logic for the selection of minimum cost function using Relational and Mux blocks of Xilinx blockset. The selection of minimum cost

function and accordingly an optimum switching state are demonstrated using a logic diagram corresponding to Fig. 3.6. Finally, part (d) shows a logic to apply the optimum switching to the inverter switches.

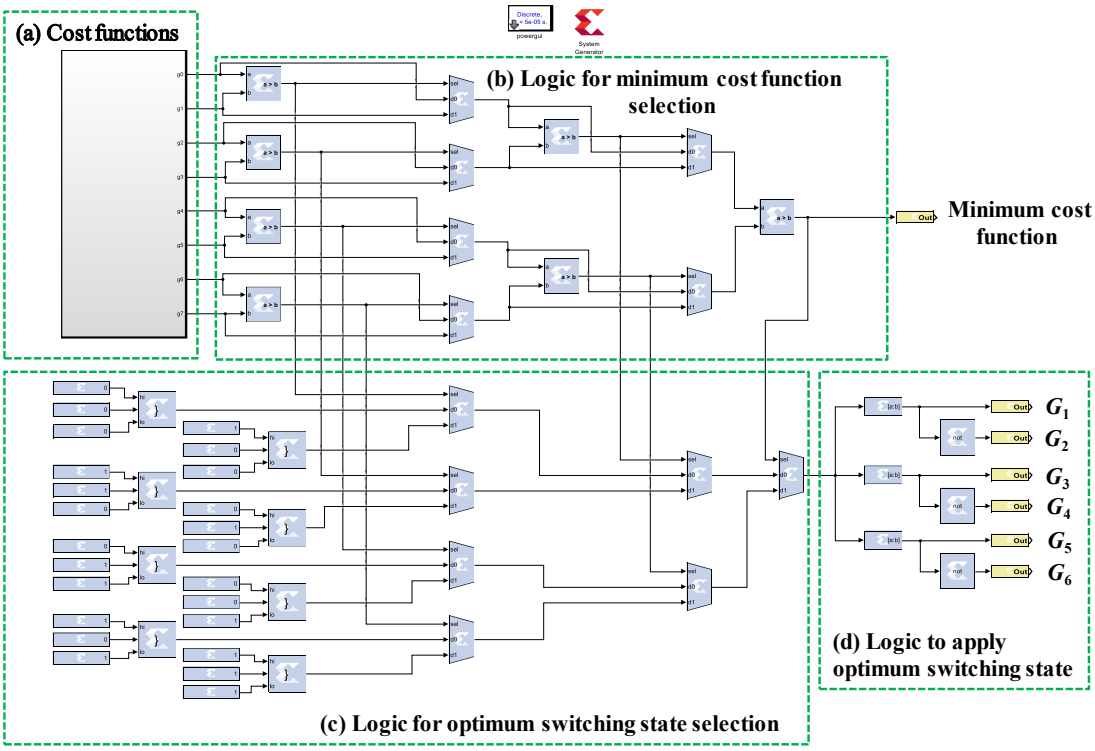


Fig. 3. 7. XSG modelling of the FCS-MPC: (a) computation of cost function, (b) selection of minimum cost function, (c) selection of optimum switching state, and (d) application of optimum switching state.

3.3 HIL Co-simulation Methodology

HIL simulation (Software + Hardware) is a technique that is used increasingly in the rapid development and testing of complex real-time embedded systems. The HIL simulation and rapid prototyping methodologies provide an intermediate level of system verification between software simulation and hardware testing. It is considered an effective method to test the performance of any novel controller or any modified controller on a simulator before implementing it on the real environment. In this approach, the design is deployed to hardware and runs in real-time. However, the surrounding components are simulated in a software environment.

In this work, the HIL co-simulation testing is performed on the XSG-based real-time simulator of FPGA (as a hardware device). The flowchart of the HIL co-simulation using

FPGA is shown in Fig. 3.8 with the three-stage validation process. At the initial stage, the controller and VSI system is modelled in MATLAB/Simulink and the performance is verified. Further, controller modelling is developed using the XSG digital platform and

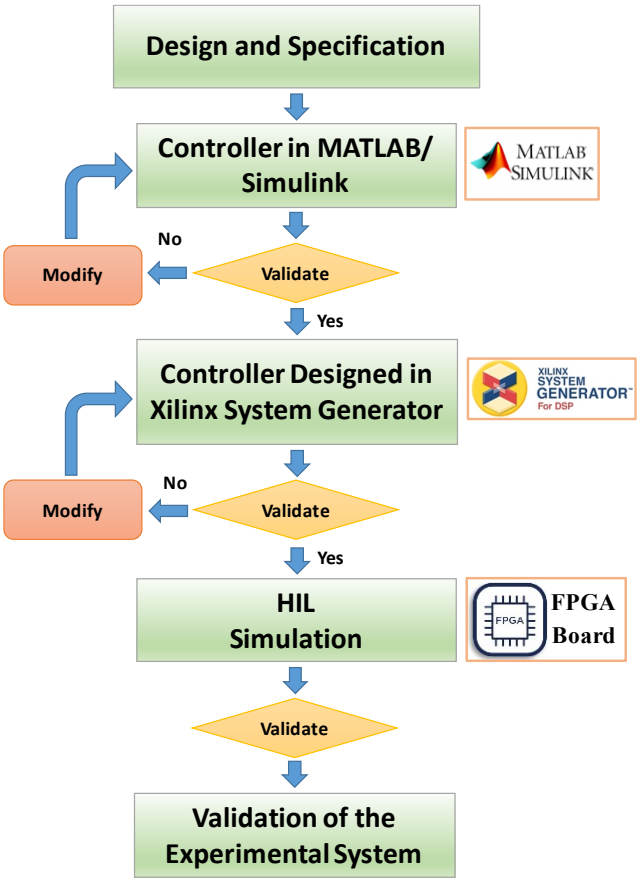


Fig. 3. 8. Flowchart of HIL co-simulation using FPGA.

the performance is analyzed considering the model of the control using Simulink. The digital modelling of the controller is validated at the later stage through the real-time HIL co-simulation.

The HIL co-simulation is considered for validation of the controller by implementing it on the hardware system through the interaction with the software system as shown in Fig. 3.9 (a). In this work, the co-simulation is performed using FPGA as actual hardware by interacting with the computer as shown in Fig. 3.9 (b). Firstly the modelling of the controller is developed in the XSG and further validation is performed using the co-simulation functionality of the XSG platform. The HIL co-simulation is performed by implementing the FCS-MPC in the FPGA through its interaction with the VSI system in

MATLAB/Simulink as represented in Fig. 3.9 (b). The co-simulation prototype block is generated by selecting the appropriate FPGA evaluation board using the XSG token in MATLAB/Simulink. The co-simulation prototype block enables the MATLAB/Simulink system to interact with the FPGA. The signal ports are assigned in the co-simulation block

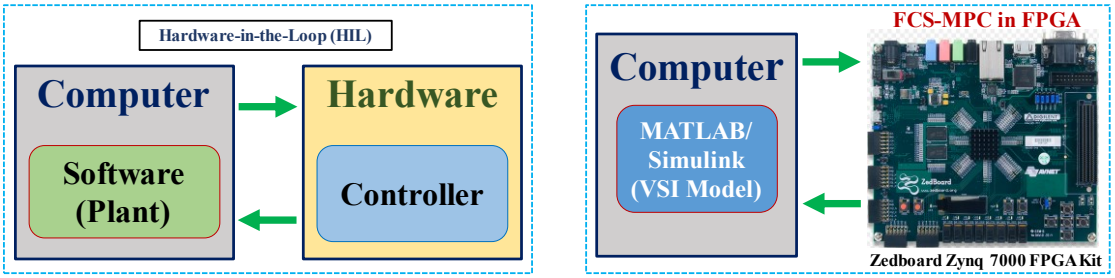


Fig. 3. 9. HIL co-simulation for controller in hardware (a) general block diagram; (b) VSI interaction with the controller in FPGA.

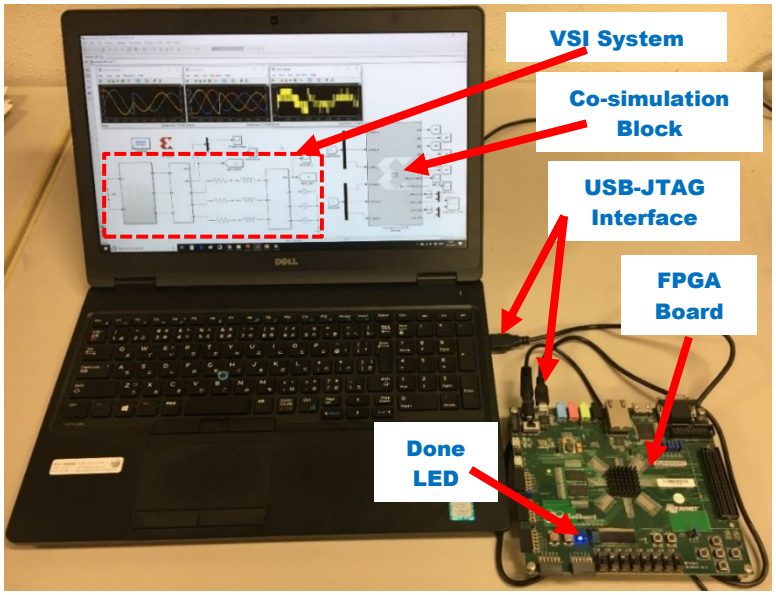


Fig. 3. 10. HIL co-simulation methodology for FCS-MPC implementation.

corresponding to the input signal from Simulink to the XSG and output signal from the XSG to Simulink.

The HIL co-simulation methodology for the FCS-MPC implementation is shown in Fig. 3.10 where the co-simulation block is generated through the digital system modelling in the XSG. The co-simulation block of the FCS-MPC contains the FPGA files that are programmed in the FPGA while performing a co-simulation and the input-output signals

are exchanged between the FPGA and MATLAB/Simulink. The FCS-MPC in $\alpha\beta$-frame and three-phase VSI system with a motor type load are considered for the simulation through XSG and HIL. The signal ports of the VSI system are connected through the signal ports assigned for the co-simulation block in MATLAB/Simulink. The validation of the controller system through co-simulation is performed using an FPGA device (Zedboard Zynq evaluation and development kit). The FPGA kit is physically connected to the computer using micro-USB cable for the exchange of signals through MATLAB/Simulink. The micro-USB cable connects the Joint Test Action Group (JTAG) port of the FPGA and a USB port of the computer to perform HIL co-simulation.

3.4 Simulation Results

Simulation methodology in Fig. 3.11 is represented using a block diagram to express a common development approach of the controller in $\alpha\beta$ as well as dq frames. The power circuit of three-phase VSI is developed in MATLAB/Simulink using the simscape power

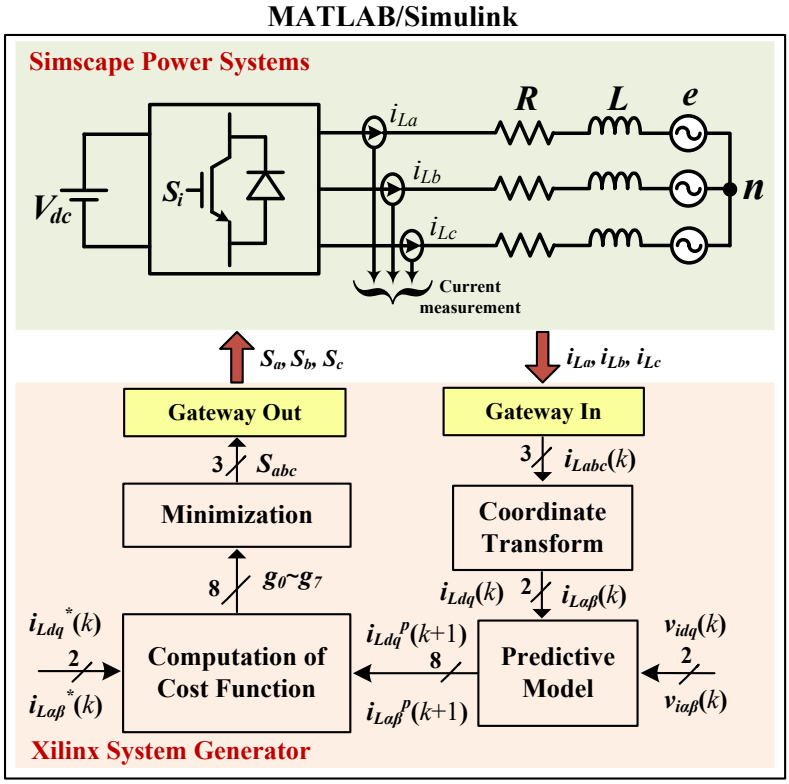


Fig. 3. 11. Block diagram representation of methodology for simulation.

Table 3. 1. Simulation parameters for the three-phase VSI system.

Description	Parameter	Value
DC supply voltage	V_{dc}	650 V
Load resistor	R	10 Ω
Load inductor	L	10 mH
Sinusoidal Back EMF	e	100 V
Frequency	f	50 Hz
Sampling period	T_S	50 µs

system toolbox, whereas the controller is developed in the digital environment of XSG using the Xilinx toolbox. Due to the non-identical platforms, a signal from simscape to XSG is interfaced using Xilinx 'Gateway In' block and a signal from XSG to simscape is interfaced using Xilinx 'Gateway Out' block.

The performance of the three-phase VSI system is validated through the implementation of the controller in MATLAB/Simulink as well as XSG environments and HIL co-simulation. The parameters considered for the VSI system with a motor type load are depicted in Table 3.1. The system performance is analyzed considering intermediate responses, the effect of sampling time and tracking performance.

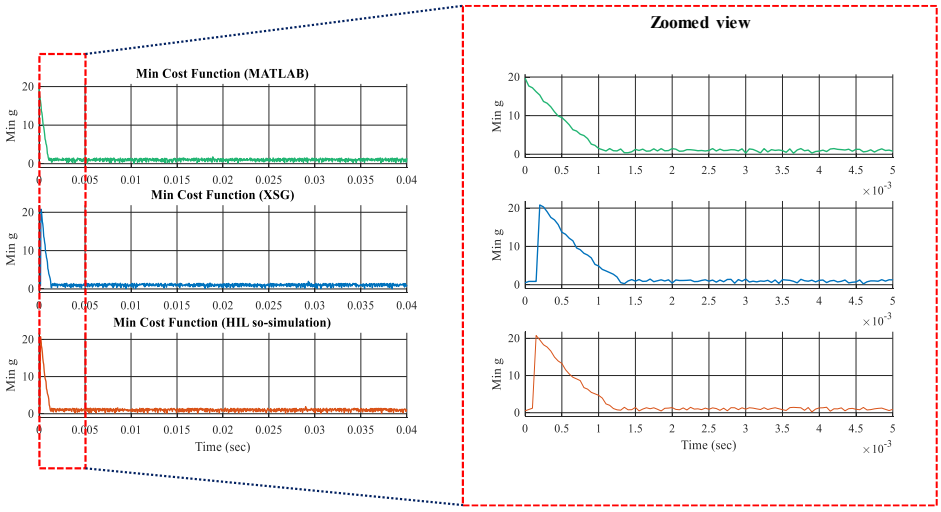


Fig. 3. 12. Minimum cost function g_{min} in each sampling interval obtained using simulation through MATLAB/Simulink, XSG and HIL.

3.4.1 Intermediate response

The intermediate responses are vital not only for the design and development of controller but also for in-depth analysis. The MBD approach for the development of the FCS-MPC is adopted considering the mentioned purpose. The performance of FCS-MPC is also analyzed considering intermediate responses: index number of the optimum switching state $\boldsymbol{S}_{opt}$ and minimum cost function g_{min}. The selected index number (0-6) represents the decimal equivalent of the binary digits for selected $\boldsymbol{S}_{opt}$ as per Table 2.2 (chapter 2), and the selected g_{min} represents the minimum current error corresponding to the sampling interval.

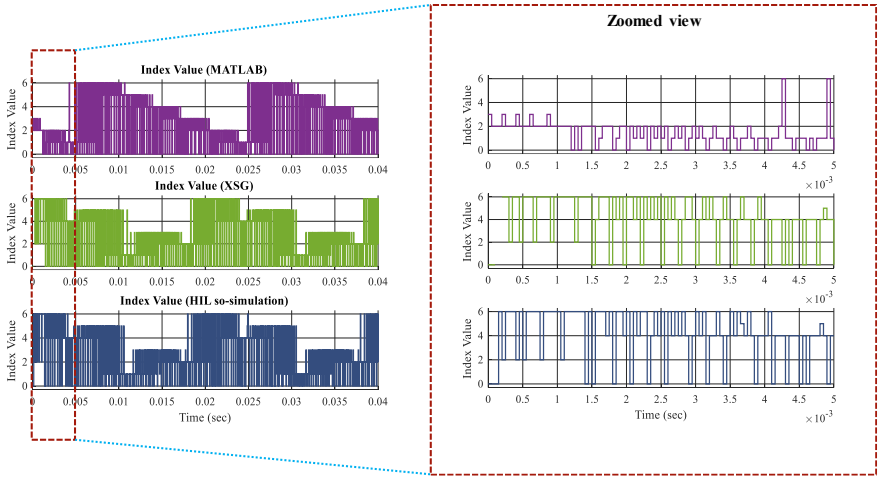


Fig. 3. 13. Index value of selected optimum switching state $\boldsymbol{S}_{opt}$ obtained using simulation through MATLAB/Simulink, XSG and HIL.

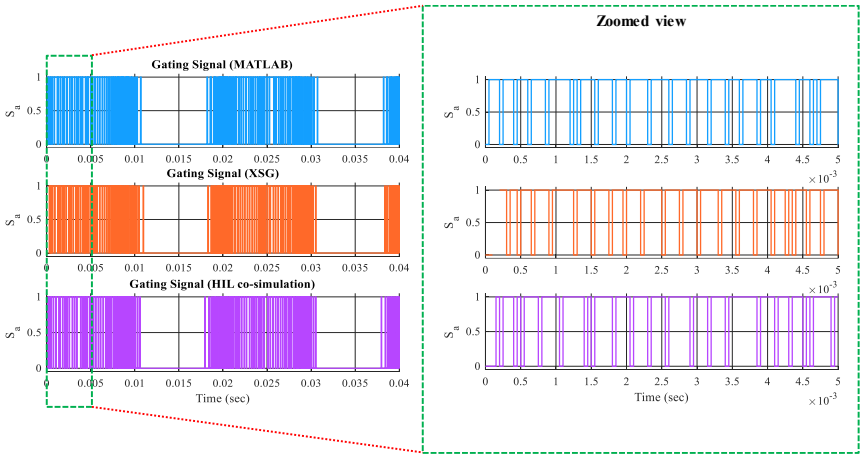


Fig. 3. 14. Switching signal for upper switch (S_a) of leg 'a' in VSI obtained using simulation through MATLAB/Simulink, XSG and HIL.

The intermediate responses: the selection of g_{min} and the index number of selected $\boldsymbol{S}_{opt}$, are analyzed for modelling and implementation of the FCS-MPC. A sampling time (T_S) of 50 µs was chosen for the selection of g_{min} for each sampling time as depicted in Fig. 3.12. The minimum cost function response results in the minimized current error. The minimized current error is required for improved performance of the system to feed quality power output. The selection of index number $\boldsymbol{S}_{opt}$ for each T_S is represented in Fig. 3.13.

The intermediate responses for Simulink are different as compared to the XSG and HIL co-simulation platforms. The responses for the XSG and HIL co-simulation are quite similar due to the digital-based platform. The small difference observed in the XSG and HIL co-simulation might be due to the prompt response during co-simulation as the controller is operating in real-time through the FPGA. The prompt response of the controller for co-simulation as compared to the XSG can be observed for the selection of g_{min} in Fig. 3.12. Further, the switching signals are generated corresponding to index number selection in each T_S that will be applied to the VSI. The switching signals in Fig. 3.14 are demonstrated for the upper power switch of leg '*a*' in VSI considering the controller implemented in all three platforms.

3.4.2 Effect of sampling time

The performance of the controller depends on the sampling time T_S selected for the discretization of the continuous-time model. Different T_S is considered for the discretization of the VSI system to analyze and validate the performance of the controller. The T_S governs the maximum switching frequency that is half of the sampling frequency. Therefore, the increase in T_S results in the decrease in the maximum switching frequency of the VSI system and vice versa. The operation of the FCS-MPC is considered for T_S = 50, 100 and 20 µs to analyze the effect of T_S. As well as, the effect of change in T_S is compared for the implementation of the FCS-MPC in MATLAB/Simulink, XSG and HIL co-simulation. The three-phase load currents are demonstrated for T_S = 50 µs in Fig. 3.15, T_S = 100 µs in Fig. 3.16 and T_S = 20 µs in Fig. 3.17.

The load current for the steady-state condition is almost similar for the implementation using all three platforms. However, the transient performances are not similar for MATLAB/Simulink and HIL co-simulation as demonstrated in an enlarged view of the

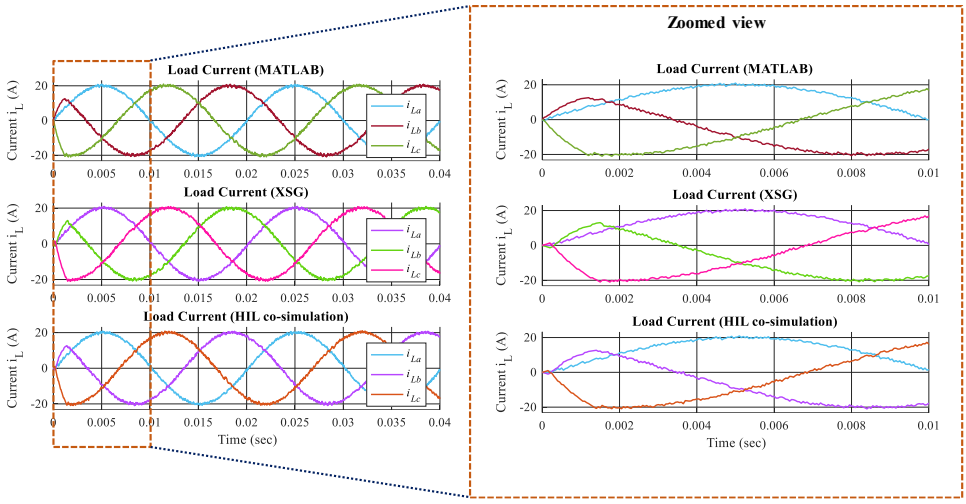


Fig. 3. 15. Three-phase load currents (i_{La}, i_{Lb}, i_{Lc}) obtained using simulation through MATLAB/Simulink, XSG and HIL with T_S = 50 µs.

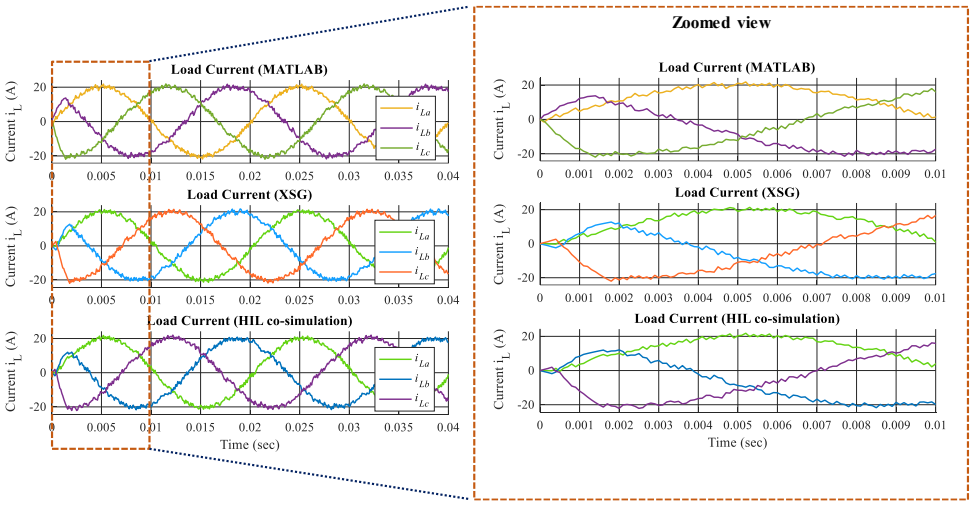


Fig. 3. 16. Three-phase load currents (i_{La}, i_{Lb}, i_{Lc}) obtained using simulation through MATLAB/Simulink, XSG and HIL with T_S = 100 µs.

load currents. The controller performance is delayed in the case of HIL co-simulation for all the sampling times considered for the demonstration. And, the similar controller response for XSG and HIL co-simulation during transients verified that the delay is due to the response of the controller rather than delay introduced due to interaction of actual hardware and computer. The delay in response is higher for high sampling time due to the operation of the controller at the low sampling frequency.

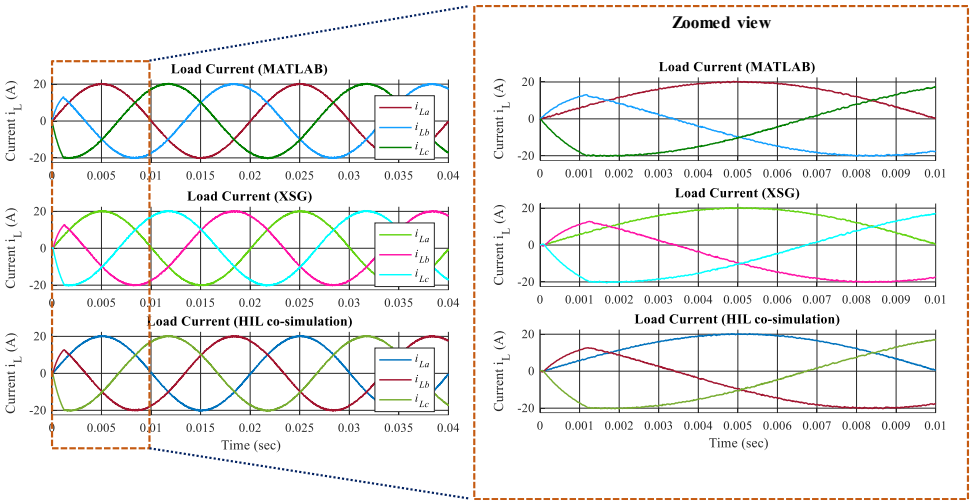


Fig. 3. 17. Three-phase load currents (i_{La}, i_{Lb}, i_{Lc}) obtained using simulation through MATLAB/Simulink, XSG and HIL with T_S = 20 µs.

3.4.3 Tracking performance

The tracking of the load current with respect to the reference is a significant characteristic to analyze the performance of a given controller. The tracking of the load current: real component ($i_{L\alpha}$) and imaginary component ($i_{L\beta}$) with respect to the sinusoidal reference current, is demonstrated in Fig. 3.18 for sampling time T_S = 50 µs. The tracking performance is

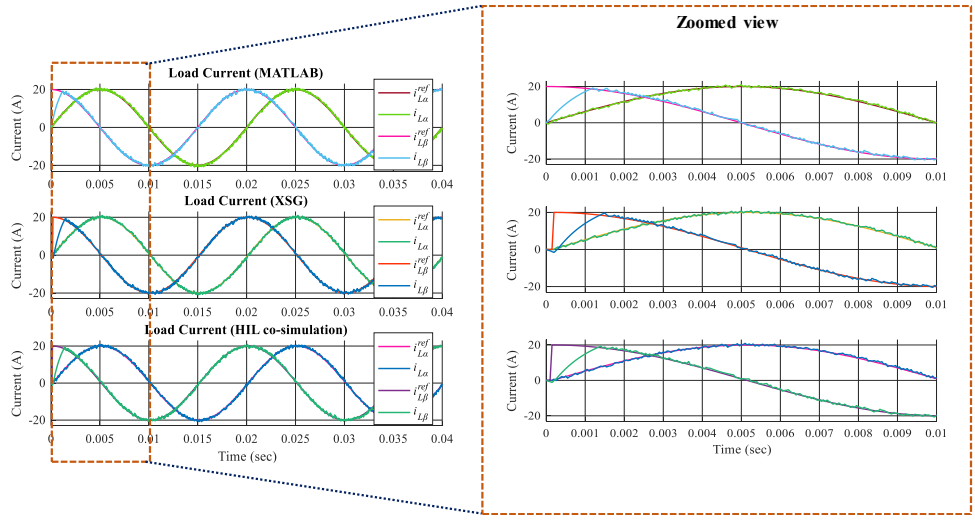


Fig. 3. 18. Current tracking for real and imaginary components of load current ($i_{L\alpha}$ and $i_{L\beta}$) obtained using simulation through MATLAB/Simulink, XSG and HIL for T_S = 50 µs.

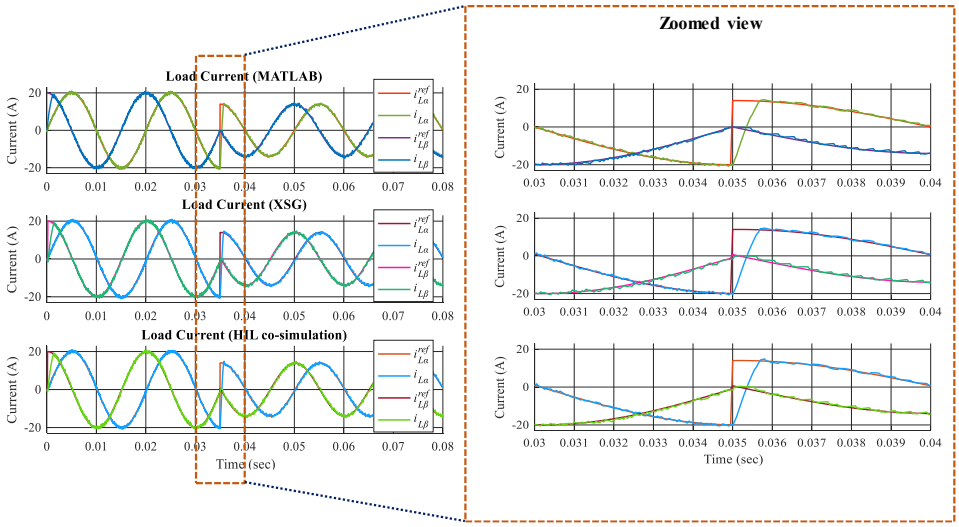


Fig. 3. 19. Current tracking for real and imaginary components of load current ($i_{L\alpha}$ and $i_{L\beta}$) for a step-change in reference obtained using simulation through MATLAB/Simulink, XSG and HIL for T_S = 50 µs.

analyzed during transients due to perturbation in the reference current as in Fig. 3.19 to demonstrate the dynamic response of the controller. The good tracking performance is obtained as the load current properly tracks the reference current at each moment during normal operating conditions as well as the transient condition. An extreme transient case is considered: change in magnitude (from 20 A to 15 A) and phase (phase difference of 180°) at the same instant with respect to normal operating conditions.

The tracking performance for all three platforms is similar to the normal operating condition as well as under dynamic conditions. However, the slight delay in response to the XSG and HIL co-simulation compared to the MATLAB/Simulink platform can be seen in the enlarged view as shown in Fig. 3.18. But, there is no delay in response for XSG and HIL co-simulation that indicates the advantage of co-simulation through the operation of the controller in a real-time environment.

3.5 Experimental Results

3.5.1 Experimental setup

The FPGA architecture of the FCS-MPC with the schematic block diagram representation of the experimental setup in Fig. 3.20 is developed for a complete understanding of the FPGA-based implementation of the system. An adequate latency is provided to blocks used to predict load current and to compute cost function for proper completion of the

computational task by the corresponding block. To ensure the selection of the optimum switching state in the given sampling interval, the sampling clock is generated as a synchronizer. The sampling clock is used as an enabling signal and given to the multiplexer

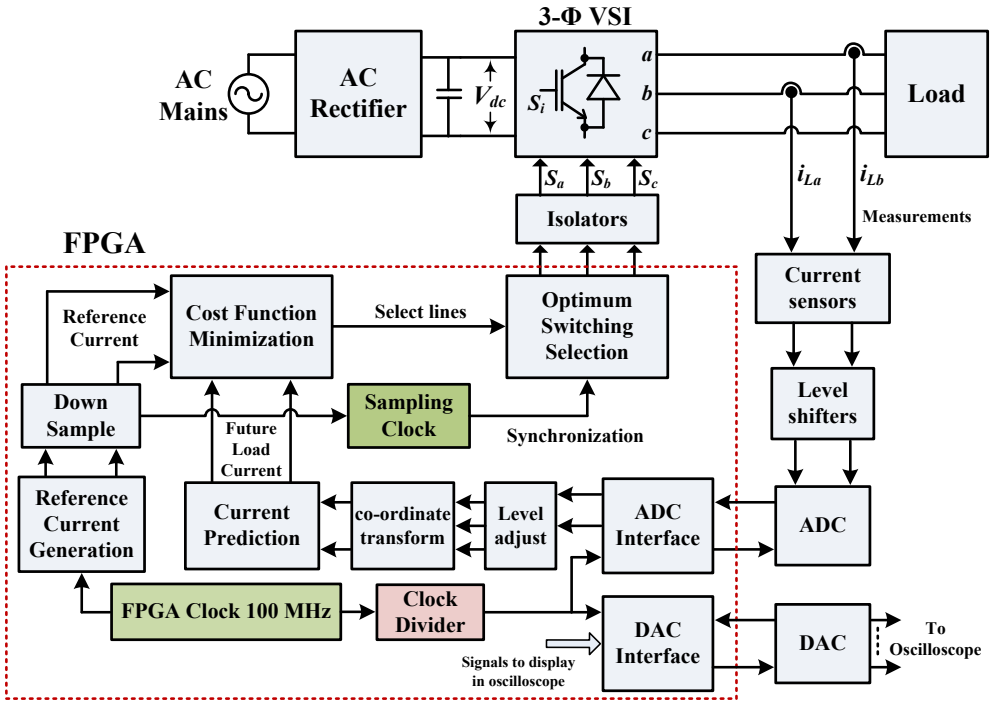


Fig. 3. 20. FPGA architecture of the FCS-MPC with the schematic block diagram of experimental setup.

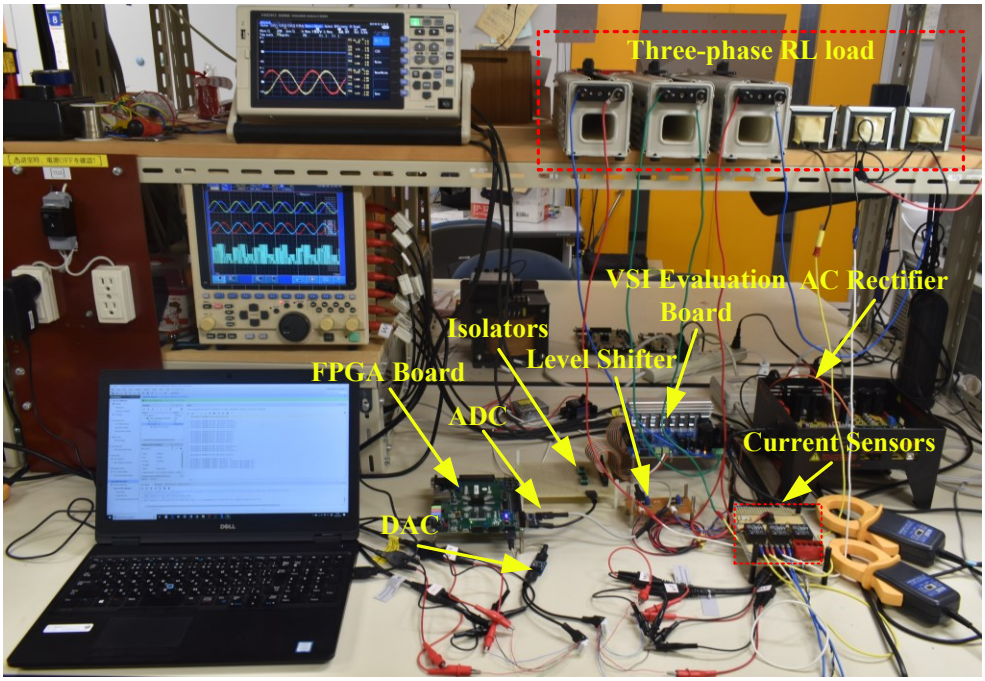


Fig. 3. 21. Laboratory prototype of the experimental setup.

that is used for the selection of optimum switching state. Before sending switching signals directly to the VSI, the isolator circuit is used for electrical isolation of the FPGA board and inverter board considering safety precautions of the FPGA board. The generation of bitstream file required to the FPGA for the execution of the XSG-based FCS-MPC is performed through the Xilinx Vivado Design Suite 2018.3 installed in the personal computer (PC). The generated bitstream files are downloaded to the FPGA using the Vivado hardware manager through the USB-JTAG interface.

The laboratory prototype of the experimental setup is demonstrated in Fig. 3.21. A summary of the components used for the experimental setup are listed here:

- **Inverter:** The STEVAL-IHM023V3 evaluation board of 1 kW three-phase inverter featuring L6390 high and low-side driver with the STMicroelectronics STGP10H60DF IGBTs is used for the system implementation.
- **DC supply:** The DC bus voltage of a high voltage digital motor control (DMC) and power factor correction (PFC) board (THDSHVMTRPFCKIT) provided by Texas Instruments is used.
- **Current sensor:** The current transducers LA 25-NP with measuring the resistance of 120 Ω and turn ratio of 3/1000 for the measurement are used for the measurement of the currents through phase ‘a’ and ‘b’.
- **ADC:** The measured sampled currents required for the execution of the FCS-MPC algorithm are governed by Digilent PmodAD1 featuring a two-channel 12-bit analog-to-digital converter (ADC) with a maximum sampling frequency of 1 µs. ADCs are interfaced through the PMOD of an FPGA board having power supply VCC of 3.3 V.
- **Level shifter:** Since PmodAD1 supports only unipolar analog signals swings from zero to positive full-scale, analog level shifters are required to sufficiently shift the dc level of analog signals. Level shifters are designed by using operational amplifiers LM385N and passive elements.
- **Isolator:** Isolators are used for the processing of switching signals to the inverter considering as a protection circuit between the FPGA board and the inverter. The quad-channel, high-speed digital isolators ADuM3440 with the power supply VCC 3.3 V is used for the mentioned purpose.

- **DAC:** In order to observe the necessary analog waveforms on the oscilloscope, Digilent PmodDA4 12-bit digital-to-analog converters (DACs) are used having eight analog output and an FPGA PMOD interface functionality like PmodAD1.
- **FPGA device:** The FPGA board Zedboard Zynq Evaluation and Development Kit having a clock frequency of 100 MHz is utilized for the real-time digital implementation of the FCS-MPC algorithm.

The performance of the FCS-MPC is evaluated for the load current control of the VSI system during the simulation and experiment through the controller implemented in $\alpha\beta$ as well as dq frames. The experimental data are obtained through HIOKI 8855 memory hicorder. Further, the data are plotted with the help of MATLAB plotting tool for demonstration and analysis of experimental results. The system parameters considered for the simulation and the experimental validation are listed in Table 3.2.

Table 3. 2. Parameters for system implementation.

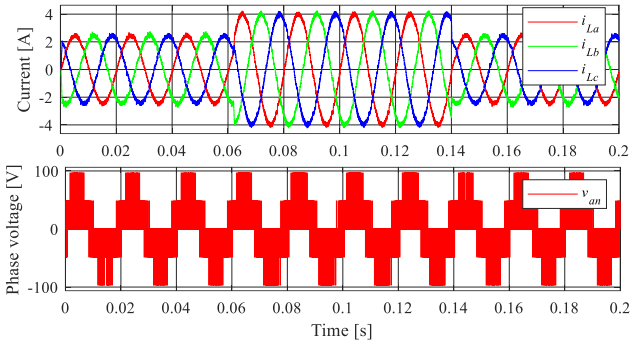
Parameter	Symbol	Value
Supply dc voltage	V_{dc}	145 V
Load resistance	R	10 Ω
Load inductance	L	10 mH
System frequency	f	50 Hz
Sampling frequency	f_S	20 kHz
FPGA clock frequency	f_{CLK}	100 MHz

3.5.2 System performance

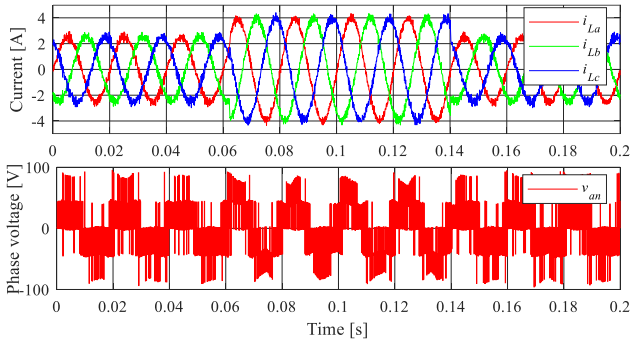
3.5.2.1 Load current and inverter voltage

The thee-phase load current waveform (i_{La}, i_{Lb}, i_{Lc}) and inverter phase voltage (phase 'a': v_{an}) in Fig. 3.22 and Fig. 3.23 are demonstrated to investigate the performance of the VSI system during the simulation as well as an experiment through the FCS-MPC implemented in $\alpha\beta$ and dq frames, respectively. Moreover, a step changes in the reference current is considered for the performance validation and analysis of FPGA-based FCS-MPC. In order to investigate the quality of current, the harmonic content in the load current is also analyzed. The THD spectrum is shown in Fig. 3.24 with the FCS-MPC in $\alpha\beta$-frame for 2.5

A (Fig. 3.24 (a) through simulation and Fig. 3.24 (b) through experiment) as well as for 4 A (Fig. 3.24 (c) through simulation and Fig. 3.24 (d) through experiment). Similarly, Fig. 3.25 shows the THD spectrum with the FCS-MPC in *dq*-frame for 2.5 A (Fig. 3.25 (a) through simulation and Fig. 3.25 (b) through experiment) as well as for 4 A (Fig. 3.25 (c) through simulation and Fig. 3.25 (d) through experiment).

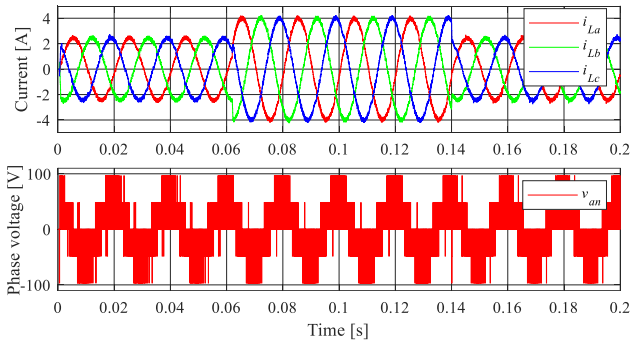


(a)

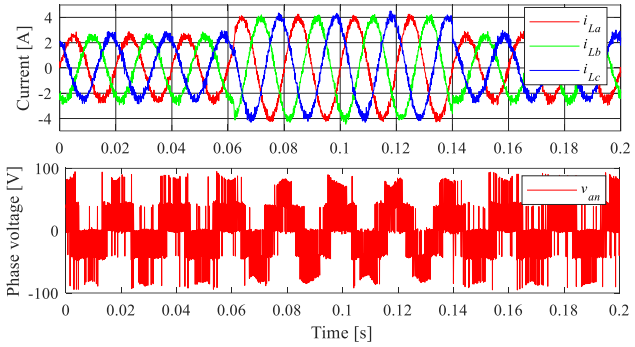


(b)

Fig. 3. 22. Three-phase load current and phase voltage (phase 'a') for the FCS-MPC in $\alpha\beta$-frame through the (a) simulation, and (b) experiment.

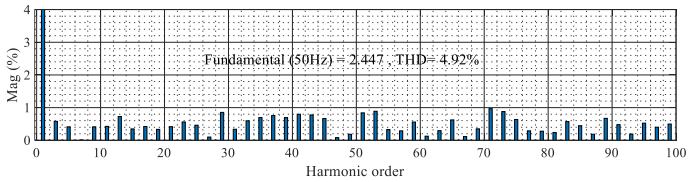


(a)

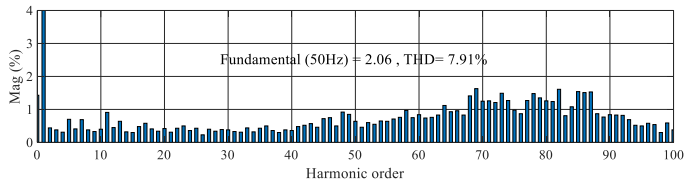


(b)

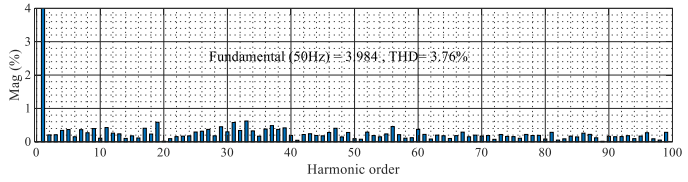
Fig. 3. 23. Three-phase load current and phase voltage (phase 'a') for the FCS-MPC in *dq*-frame through the (a) simulation, and (b) experiment.



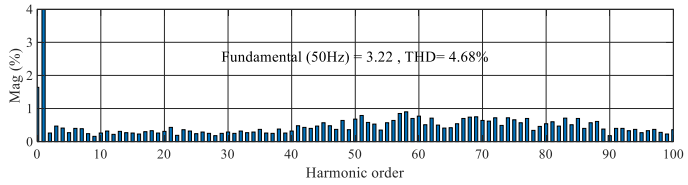
(a)



(b)



(c)



(d)

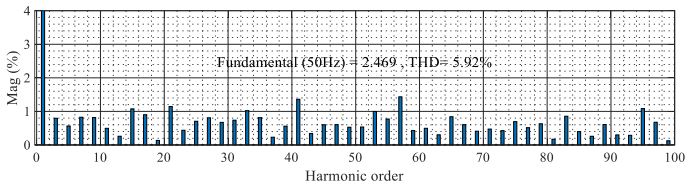
Fig. 3. 24. THD spectrum in the load current for reference amplitude 2.5 A through (a) simulation, (b) experiment; and for 4 A through the (c) simulation, (d) experiment using the FCS-MPC in *αβ*-frame.

The percentage THD graph has spread spectrum nature due to the variable switching frequency of the FCS-MPC. A higher percentage THD is observed for lower current

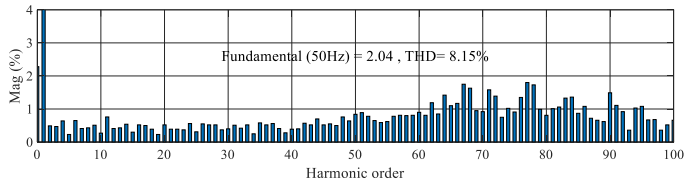
reference (2.5 A) for both frames due to lower current reference amplitudes, however, the percentage THD is more in the case of *dq*-frame as compared to *αβ*-frame. The higher percentage THD is observed during experimental validation as compared to simulations for both the cases. Further, the percentage THDs are more for the current reference 2.5 A than 4 A due to lower current reference amplitudes that validate with the simulation results.

3.5.2.2 Tracking performance

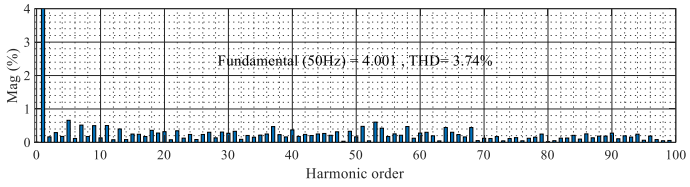
In order to investigate the performance of the three-phase VSI system with FCS-MPC, dynamic response of controller is analyzed where the tracking performance of the load



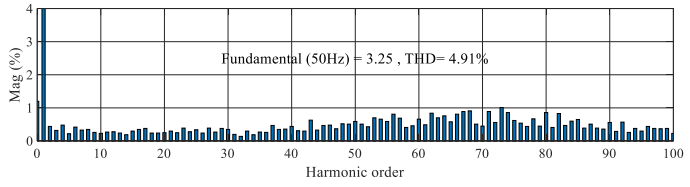
(a)



(b)



(c)

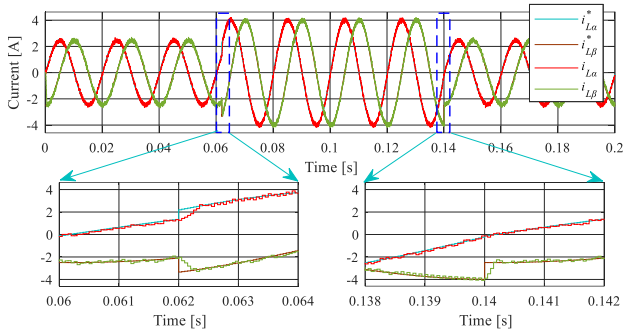


(d)

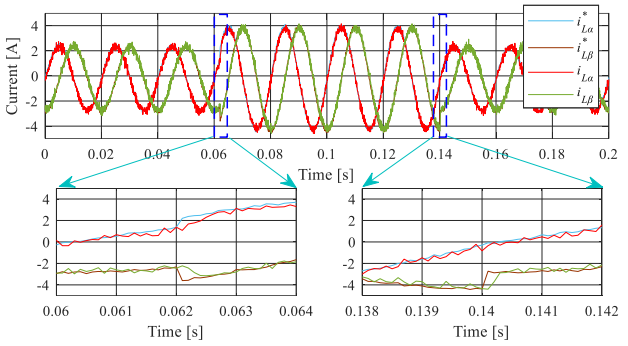
Fig. 3. 25. THD spectrum in the load current for reference amplitude 2.5 A through (a) simulation, (b) experiment; and for 4 A through the (c) experiment using simulation, (d) the FCS-MPC in *dq*-frame.

current is demonstrated for a step-change in reference current from 2.5 A to 4 A at instant 0.062 s and from 4 A to 2.5 A at instant 0.14 s. The load current tracking in Fig. 3.26 and

Fig. 3.27 are demonstrated to investigate the performance of the VSI system during the simulation as well as an experiment through the FCS-MPC implemented in $\alpha\beta$ and dq frames, respectively. The current tracking in $\alpha\beta$-frame is demonstrated considering real and imaginary components ($i_{L\alpha}$, $i_{L\beta}$), whereas, in dq-frame using direct and quadrature components (i_{Ld}, i_{Lq}). In the case of the dq-frame, the step changes are applied in the d-axis component of the reference current, keeping the q-axis reference current zero. The time axis is enlarged to demonstrate the current tracking during the transient caused by step

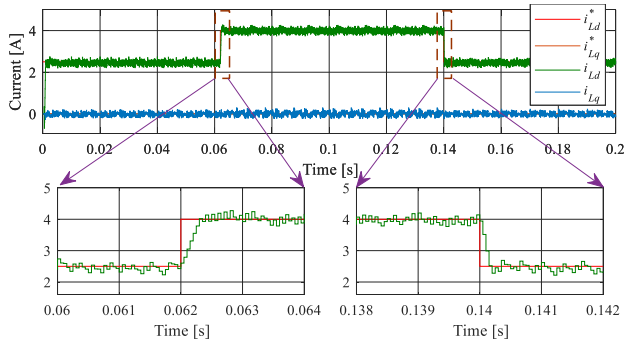


(a)

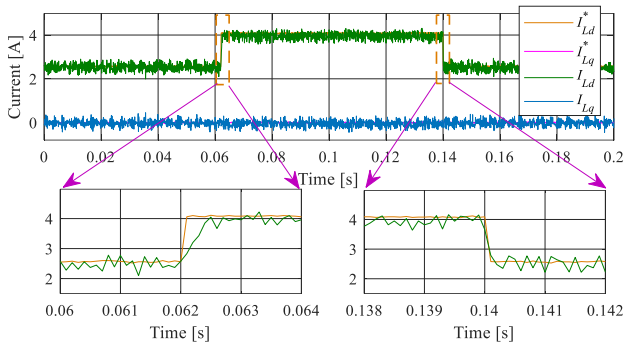


(b)

Fig. 3. 26. Tracking performance of load current $i_{L\alpha}$, $i_{L\beta}$ for the FCS-MPC in $\alpha\beta$-frame through the (a) simulation, (b) experiment.



(a)



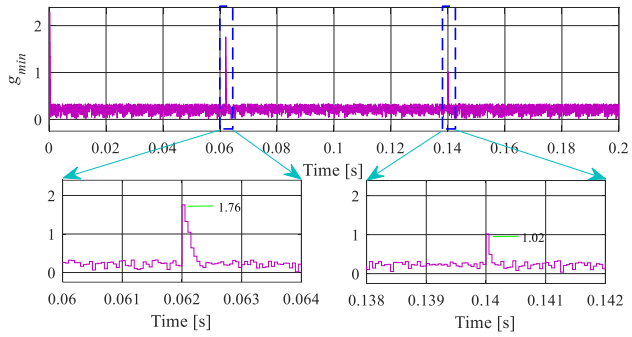
(b)

Fig. 3. 27. Tracking performance of load current $i_{L\alpha}$, $i_{L\beta}$ for the FCS-MPC in dq-frame through the (a) simulation, (b) experiment.

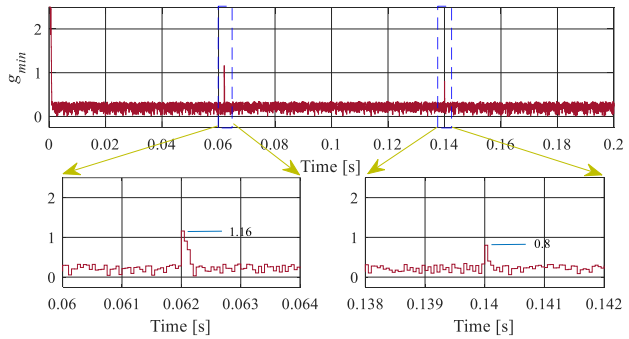
changes in reference current. From the enlarged view, it is investigated that the good dynamic response is maintained for both step changes for the FCS-MPC in both frames.

3.5.2.3 Intermediate responses

The value of minimum cost function g_{min} and the index number of the selected optimum switching state $\boldsymbol{S}_{opt}$ corresponding to the g_{min} for each sampling interval are depicted in Fig. 3.28 and Fig. 3.29, respectively with the FCS-MPC in $\alpha\beta$ as well as dq frames considering

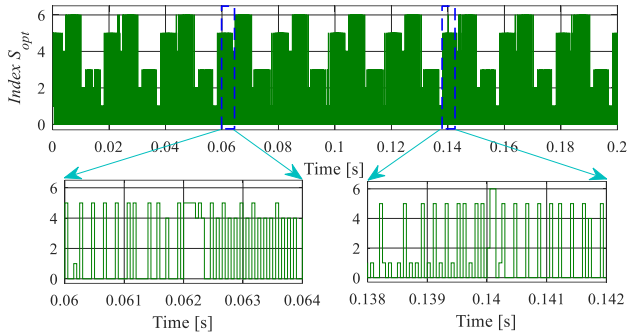


(a)

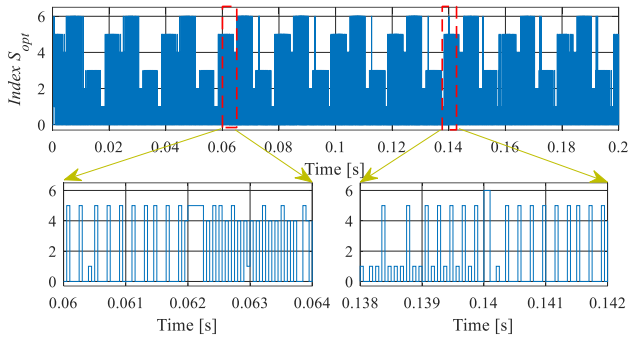


(b)

Fig. 3. 28. Simulation results: The values of minimum cost function g_{min} for the FCS-MPC in (a) $\alpha\beta$-frame and (b) dq-frame.



(a)

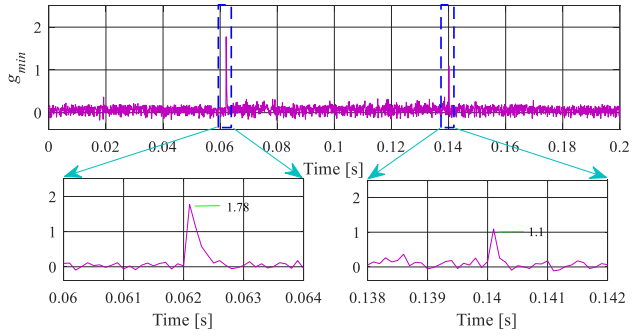


(b)

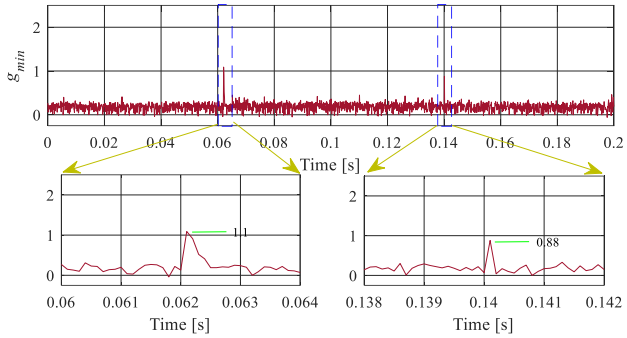
Fig. 3. 29. Simulation results: The index number of selected optimum switching state S_{opt} in each sampling interval for the FCS-MPC in (a) $\alpha\beta$-frame and (b) dq-frame.

the simulation results. Similarly, the value of g_{min} and the index number of the selected $\boldsymbol{S}_{opt}$ are depicted in Fig. 3.30 and Fig. 3.31, respectively with the FCS-MPC in both frames for the results obtained during the experiment.

The intermediate responses are intentionally demonstrated as an enlarged view during the instant of transients caused by the two step changes in reference current. The selection

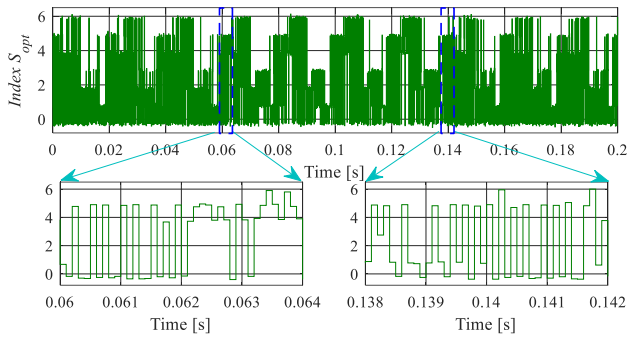


(a)

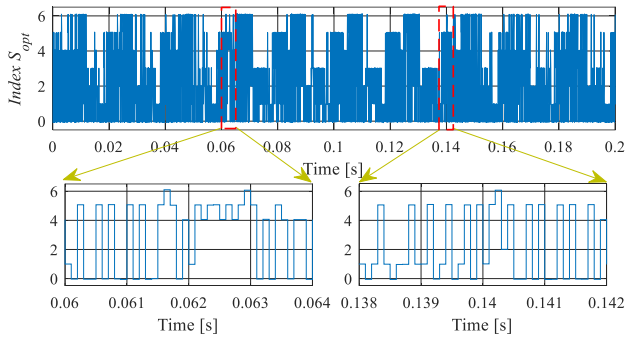


(b)

Fig. 3. 30. Experimental results: The values of minimum cost function g_{min} for the FCS-MPC in (a) $\alpha\beta$-frame and (b) dq-frame.



(a)



(b)

Fig. 3. 31. Experimental results: The index number of selected optimum switching state S_{opt} in each sampling interval for the FCS-MPC in (a) $\alpha\beta$-frame and (b) dq-frame.

of index numbers among 0 to 6 can be observed with a similar selection profile in each complete cycle. Regarding simulation results, the selected $\boldsymbol{S}_{opt}$ in each sampling intervals is not identical with respect to sampling interval for the FCS-MPC in $\alpha\beta$ and dq frames that signify the different selection of optimum voltage vectors, and consequently the selection of the minimum current error. Similar to the selection of $\boldsymbol{S}_{opt}$, the values of g_{min} are following the same profile for both frames and a sharp spike is observed at the instant of

step changes (0.062 s, 0.14 s) that signifies the step changes provided in reference current at that instants. There is a significant difference in the sharp spikes at instants 0.062 and 0.14 s, however, a slight change in spikes is observed for the case of simulation through the FCS-MPC in $\alpha\beta$ and dq frames at both instants. The significant difference in spike maybe because of the higher (4 A) to lower (2.5 A) step change in current reference at instant 0.14 s.

In the case of experiments, the selection profiles for the index numbers of the selected $\boldsymbol{S}_{opt}$ are similar to those analyzed during the simulations for each sampling interval. Further, the non-identical selected $\boldsymbol{S}_{opt}$ with respect to sampling interval for the FCS-MPC in $\alpha\beta$ and dq frames validate the different selection of optimum voltage vectors, and consequently the selection of minimum current error. As compared to the simulation results, the values of g_{min} are following the same profiles for both frames and a sharp spike observed at the instant of step changes (0.062 s, 0.14 s) validates the step changes provided in reference current at that instants. However, the slightly higher peak of the sharp spikes is observed during the experiments for both the cases.

3.6 Summary

This chapter presented the features of a model-based design (MBD) platform and step-by-step development of the FCS-MPC algorithm on a digital simulator of Xilinx (XSG) considering the controller implementation in two coordinates $\alpha\beta$ and dq. The XSG modelling of the FCS-MPC in $\alpha\beta$-frame was further tested through HIL co-simulation using FPGA for controlled power conversion through the three-phase VSI system considered with motor load condition. The FCS-MPC was initially implemented in MATLAB/Simulink and further in the XSG platform that used for digital system design. The controller performance is validated for the real-time environment through a HIL co-simulation considering the step-by-step analysis through intermediate outputs: minimum cost function and selection of an index number. Also, the performance is validated considering the effect of the sampling time and tracking performance under dynamic conditions. The modelling of the FCS-MPC in XSG is a viable choice due to the discrete nature of the controller. As well as, the real-time HIL co-simulation is a realistic approach for the implementation by validating the controller performance before applying it to the

real experimental system to reduce the risk of component damage/whole system failure. The integrated platform of MATLAB/Simulink-XSG can be further used to generate HDL codes for the implementation of FCS-MPC in the real-time experimental system using FPGA.

The FPGA-based real-time implementation was performed with the FCS-MPC developed in the $\alpha\beta$ and dq frames through the modelling in XSG for the load current control of the three-phase VSI system. The FCS-MPC readily suits for the real-time FPGA-based system implementation through the modelling in digital simulator due to its inherent discrete nature. Moreover, the model-based design platform is advantageous to the rapid development through easy debugging and refinement in controller design by observing intermediate responses.

The experimental results validate the results obtained through the digital simulation environment of XSG considering the system performance by the dynamic response and intermediate response analysis. The fast dynamic response of the FCS-MPC is verified during experiments through the load current tracking with two step changes in the reference current for both frames. The increased ripple content in the load current with a lower amplitude of reference is validated from the load current tracking.

The system implementation through the FCS-MPC in dq-frame is considered better for the in-depth system analysis, however, as compared to the FCS-MPC in $\alpha\beta$-frame, complexity level increases due to additional coordinate transformation ($\alpha\beta$ to dq), reference phase angle generation θ^*, and computation of feed-forward term in decoupling for the design. Therefore, the system implementation using $\alpha\beta$-frame is preferable with the well-established controller, however, further improvement in the controller can be performed through better analysis using dq-frame.

Some improvement in the FCS-MPC is presented in chapter 4 considering issues of performance dependency on the accurate model, high switching frequency and steady-state error.

Chapter 4

ADVANCED FCS–MPC: ADAPTIVE PREDICTIVE MODEL AND MODIFIED COST FUNCTION

4.1 Introduction

The FCS-MPC directly uses the discrete-time model (predictive model) of the system to predict the behavior of the controlled variables of the system and the discrete-time model is dependent on the system parameters. The control dependency on model parameters creates problems in a real-time environment, where the parameters may vary due to various reasons such as error during measurement or change during the operation of the system [96]. In addition, the power electronics components used in the system may change their values with temperature, operating conditions and interval of time (aging effect) [97]. Due to the above reasons, there may be a parameter mismatch between the model for prediction and the actual system. The model parameter mismatch causes inaccuracy in the prediction of the system behavior and affects the performance of the controller [98].

The FCS-MPC has been applied to a wide variety of power converters for a load current control objectives where the load normally consists of resistance and inductance. The load resistance variations result in a steady-state error (SSE) in the predicted current, whereas the load inductance mismatch is responsible for transient as well as steady-state errors in the predicted current [97]. Therefore, a deviation in the load inductance results in the increased ripple in the load current. This error is more significant when operated with lower switching frequency or lower amplitude of current reference [99]-[101]. In [99], the concepts of intermediate sampling, as well as integral error term, were proposed to face the problem of SSE and results were presented for the current control of the four-quadrant chopper converter. In [100], the problem of SSE during model parameter mismatch was

addressed and an approach to incorporate past current errors as a constraint inside a cost function with a variable weighting factor was proposed towards the elimination of SSE.

An adaptive predictive model is proposed in this work to compensate for the effect of change in load parameters by using simple mathematical relation of the three-phase inverter output voltage, dc voltage supply, and modulation index. The predictive model coefficient computed using load parameters is one of the significant factors that influence system performance. The performance is analyzed based on the implementation of the FCS-MPC in stationary $\alpha\beta$ and rotating dq frames for the adaptive predictive model. The dynamic behavior and steady-state error are considered for analysis of system performance.

Apart from the issue of model parameter mismatch, the FCS-MPC has to deal with some other drawbacks, such as variable switching frequency that causes switching losses and unwanted resonances. The average switching frequency increases when the system is operated with higher sampling for enhanced performance that results in even higher switching losses. In this way, a high switching frequency issue of the FCS-MPC is one of the major drawbacks of the controller that is a by-product of using high sampling frequency for the enhanced system performance. The functionality of controlling various control variables simultaneously by using only a single control function or cost function can be utilized to overcome the issue of the high switching frequency. The issue of switching frequency has been addressed by researchers and various approaches towards a reduction of switching frequency has been proposed [63]–[67]. One of the most intuitive ideas to minimize control effort with switching frequency reduction is to include an additional parameter inside the cost function such as the change in switching state to control the number of commutations of the power switches [32], [63].

In general, dedicated constraints for the reduction in average switching frequency and SSE are incorporated inside a cost function in conventional FCS-MPC. Nevertheless, that ultimately increases the computational burden. It is desirable to achieve improved SSE with a reduction in average switching frequency considering the computational burden for implementation of the FCS-MPC. A modified cost function based on a novel constraint is proposed in this work to facilitate the reduction in SSE together with the objective of switching frequency reduction using a modified FCS-MPC approach. In the novel

proposed constraint, the past value of computed reference voltage vector and present value of voltage vector (corresponding to the past and the present current error respectively) are used for the design of novel modified cost function.

4.2 Adaptive Predictive Model

The predictive models described in chapter 2 for the FCS-MPC in $\alpha\beta$-frame (2.17) as well as dq-frame (2.19) depend on the coefficients k_1, k_2, k_3, for current prediction and computed using the load parameters (R, L) as represented below:

$$k_1 = \left(1 - \frac{RT_S}{L}\right),\ k_2 = \frac{T_S}{L},\ k_3 = \omega^* L \tag{4.1}$$

Normally, the exact value of the coefficients k_1 is very close to 1 according to the nominal parameter values and sampling time T_S. Some previous works have been presented considering the FCS-MPC implementation with the approximated value of the coefficient k_1 (k_1 = 1) considering fewer computations in the system implementation [30], [32]. However, system implementation with the approximated coefficient may increase the ripple content in the load current.

An approach towards improved performance with the accurate predictive model is required because any change in load parameters disturbs the accuracy of the predictive model, which ultimately affects the performance of the FCS-MPC. The value of a coefficient can be updated to compensate for the effect of change in load parameters. In this work, an approach to update the coefficient k_1 (adaptive k_1) corresponding to the change in load resistance R is considered by assuming unchanged load inductance L.

According to the phase voltage and line current relationship, the load impedance Z can be calculated as given below

$$Z = \frac{v_{ph,rms}}{i_{L,rms}} \tag{4.2}$$

where $v_{ph,rms}$ is the rms values of voltage in any phase and $i_{l,rms}$ is the rms value of the load current. The $v_{ph,rms}$ can be simply obtained using the relation between the phase voltage and a dc supply to an inverter as

$$V_{dc} = \frac{2\sqrt{2}v_{ph,rms}}{m} \tag{4.3}$$

where m is a modulation index.

By substituting the value of $v_{ph,rms}$ from (4.3) into (4.2), the value of Z can be updated according to the relation given as follows

$$Z = \frac{mV_{dc}}{2\sqrt{2}i_{L,rms}} \tag{4.4}$$

Since the load impedance Z contains resistive (R) as well as inductive reactance (X_L) and represented as

$$Z = \sqrt{R^2 + \left(X_L\right)^2}, \text{ where } X_L = \omega L \tag{4.5}$$

R can be computed by putting the value of Z from (4.4) to (4.5) and formulated as

$$R = \sqrt{\left(\frac{mV_{dc}}{2\sqrt{2}i_{L,rms}}\right)^2 - \left(X_L\right)^2} \tag{4.6}$$

Then, the value of k_1 can be updated with the updated R from (4.6) as a fixed value of L is considered. Thus, an expression for the adaptive k_1 can be generated by putting R from (4.6) to (4.1) and written as follows

$$k_1 = \left(1 - \frac{T_S}{L}\sqrt{\left(\frac{mV_{dc}}{2\sqrt{2}i_{L,rms}}\right)^2 - \left(X_L\right)^2}\right) \tag{4.7}$$

Since $\left(\frac{mV_{dc}}{2\sqrt{2}i_{L,rms}}\right)^2 \gg X_L$ the value of k_1 can be approximated as

$$k_1 = \left(1 - \frac{mV_{dc}T_S}{2\sqrt{2}Li_{L,rms}}\right) \tag{4.8}$$

The values of V_{dc}, T_S, and L are known and $i_{L,rms}$ can be obtained from the reference load current. In this way, k_1 can be updated from (4.8) with an assumption of $m = 1$.

By putting the values of simulation as well as experimental system parameters (V_{dc} = 145 V, T_S = 50µs, L = 10 mH), the value of adaptive k_1 can be expressed as

$$k_1 = \left(1 - \frac{0.2564}{i_{L,rms}}\right) \tag{4.9}$$

4.2.1 Performance with adaptive predictive model

The performance of the FCS-MPC in $\alpha\beta$ and dq frames are evaluated through the simulation as well as experiments considering the approximated (k_1 = 1) and adaptive value of the coefficient used for the current prediction and a comparative analysis is presented. Initially, the FCS-MPC with only the current control objective is considered for performance analysis. Later on, a constraint of change in switching state is considered for the comparative analysis with the change in weighting factor.

The thee-phase load current waveform (i_{La}, i_{Lb}, i_{Lc}) in Fig. 4.1 and Fig. 4.2 is demonstrated to investigate the performance of the VSI system during the simulation as well as an experiment through the FCS-MPC implemented in $\alpha\beta$ and dq frames, respectively considering k_1 = 1 and without any constraint. Moreover, a step changes in the reference current is considered for the performance validation and analysis of the FCS-MPC implementation using the FPGA.

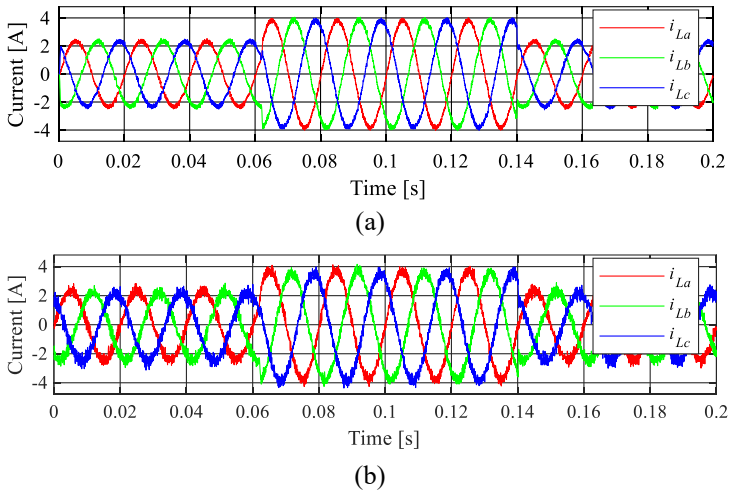
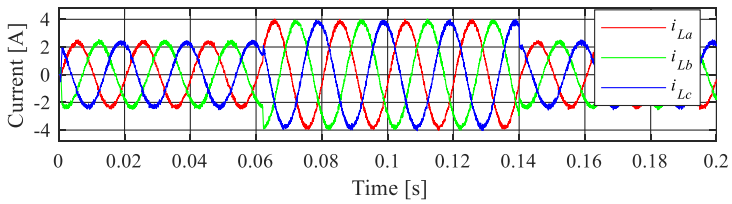
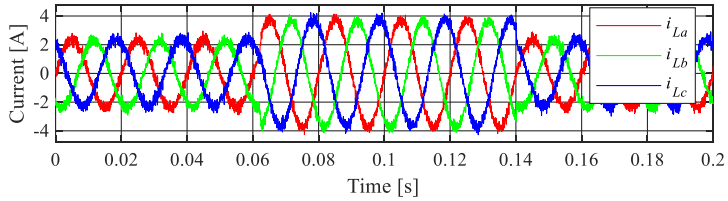


Fig. 4. 1. Three-phase load current for the FCS-MPC in $\alpha\beta$-frame with k_1 = 1 through (a) simulation and (b) experiment.



(a)



(b)

Fig. 4. 2. Three-phase load current for the FCS-MPC in *dq*-frame with $k_1 = 1$ through (a) simulation and (b) experiment.

4.2.1.1 Effect of change in coefficient k_1

The exact value of the coefficient k_1 ($k_1 = 0.95$) is also considered for the performance verification that is calculated by putting the values of the system parameters ($R = 10\ \Omega$, $L = 10$ mH, $T_S = 50\mu$s). The performance of the FCS-MPC in $\alpha\beta$ and *dq* frames is analyzed for the controller modelling with exact ($k_1 = 0.95$), approximate ($k_1 = 1$) as well as the adaptive values of the coefficient k_1. Moreover, the simulation and experiment were carried out considering the cost function without constraint for reference currents with low load ($\boldsymbol{i}_L = 2.5$ A) and high load ($\boldsymbol{i}_L = 4$ A) conditions. To investigate the quality of the load current and the switching stress on the power devices, the harmonic content in the load current corresponding to the average switching frequency (f_{sw}) is also analyzed considering both the frames. The results obtained during the simulation as well as an experiment are listed in Table 4.1 and 4.2 for the FCS-MPC in $\alpha\beta$ and *dq* frames, respectively. The harmonic content in the load current during the experiment was measured through HIOKI 3390 power analyzer and current clamp sensor.

During the simulation, a slight difference in percentage THD with the consequent change in average f_{sw} is observed for the FCS-MPC in $\alpha\beta$ and *dq* frames corresponding to the constants k_1, however, the performance is quite similar during the experiment. The percentage THD is less in the case of high load with the cost of slightly higher switching stress as compared to low load during the simulation. However, a significantly high current

Table 4. 1. Performance of the FCS-MPC in $\alpha\beta$-frame.

Indices		$\boldsymbol{i}_L = 4$ A			$\boldsymbol{i}_L = 2.5$ A		
		$k_1 = 0.95$	$k_1 = 1$	adaptive k_1	$k_1 = 0.95$	$k_1 = 1$	adaptive k_1
Simulation	THD (%)	3.54	3.69	3.57	5.28	5.60	5.0
	Average f_{sw} (Hz)	3733	3603	3700	3053	2983	3017
Experiment	THD (%)	4.9	5.2	4.6	8.5	9.1	7.5
	Average f_{sw} (Hz)	2556	2489	2445	2325	2150	2350

Table 4. 2. Performance of the FCS-MPC in dq-frame.

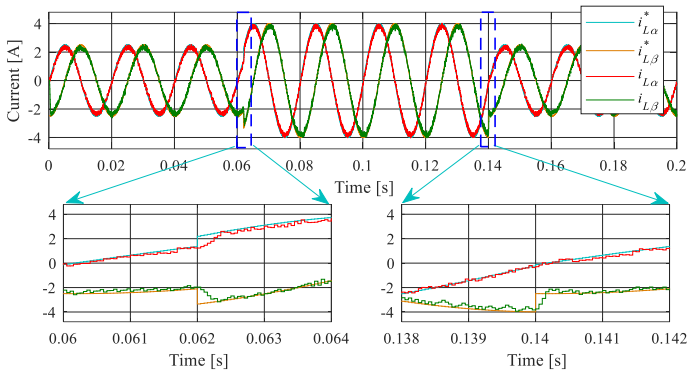
Indices		$\boldsymbol{i}_L = 4$ A			$\boldsymbol{i}_L = 2.5$ A		
		$k_1 = 0.95$	$k_1 = 1$	adaptive k_1	$k_1 = 0.95$	$k_1 = 1$	adaptive k_1
Simulation	THD (%)	3.74	3.92	3.55	5.61	5.86	5.50
	Average f_{sw} (Hz)	3911	3703	3630	3306	3023	3223
Experiment	THD (%)	4.8	5.3	4.7	8.4	9.2	7.9
	Average f_{sw} (Hz)	2586	2524	2465	2365	2120	2410

THDs are observed during the experiment for the low load as compared to high load conditions. The percentage THD in the load currents through the experiment is higher as compared to the simulation that is because of the simplified model of the VSI and the load used for the simulation study. Compared to the other cases of k_1, the controller performance is slightly better for current prediction with adaptive k_1 in both low load as well as high load conditions.

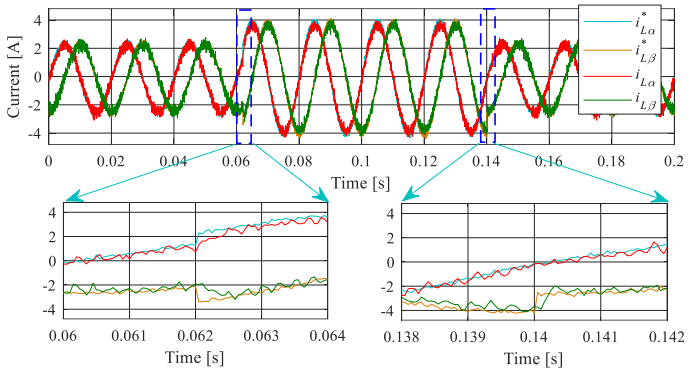
4.2.1.2 Dynamic performance

To investigate the dynamic performance of the FCS-MPC for the three-phase VSI system, the step change in the reference current is considered for current tracking during the transients. The comparative analysis for the system implementation using adaptive k_1 and

$k_1 = 1$ is performed considering simulation as well as experimental results. The tracking performance of the load current is demonstrated for the change in reference current from 2.5 A to 4 A at instant 0.062s and from 4 A to 2.5 A at instant 0.14s. The time axis is enlarged to demonstrate the current tracking during the transient caused by step changes in reference current.



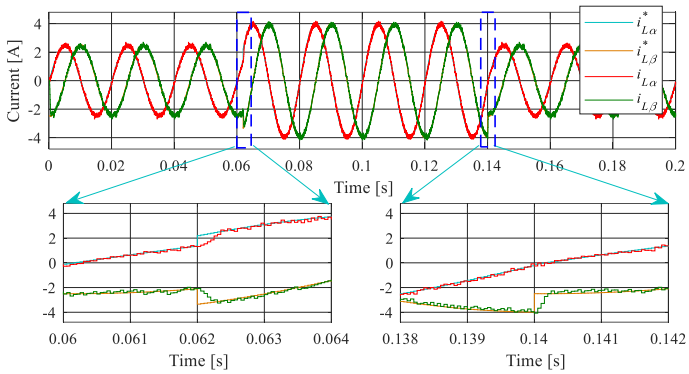
(a)



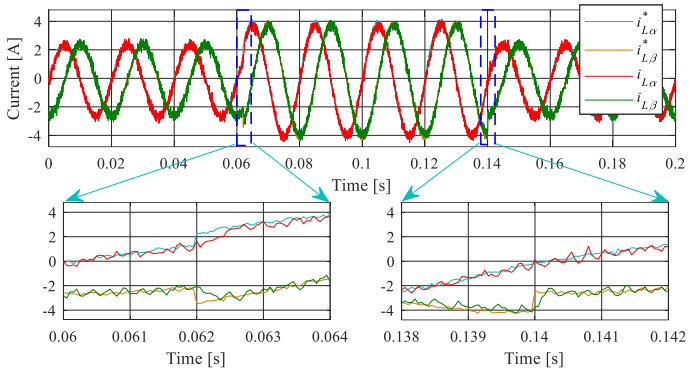
(b)

Fig. 4. 3. Load current tracking performance for the FCS-MPC in $\alpha\beta$-frame with $k_1 = 1$ through (a) simulation, (b) experiment.

The current tracking in Fig. 4.3 and Fig. 4.4 are depicted for the controller in $\alpha\beta$-frame with $k_1 = 1$ and adaptive k_1 respectively. Similarly, the current tracking in the dq-frame is demonstrated in Fig. 4.5 and Fig. 4.6 with $k_1 = 1$ and adaptive k_1, respectively. In the case of the dq-frame, the step changes are applied in the d-axis component of the reference current, keeping the q-axis reference current zero. The dynamic response is almost the same for the current prediction using $k_1 = 1$ as well as adaptive k_1. However, there is a noticeable SSE in current tracking for $k_1 = 1$ as compared to adaptive k_1.



(a)



(b)

Fig. 4. 4. Load current tracking performance for the FCS-MPC in $\alpha\beta$-frame with adaptive k_1 through (a) simulation, (b) experiment.

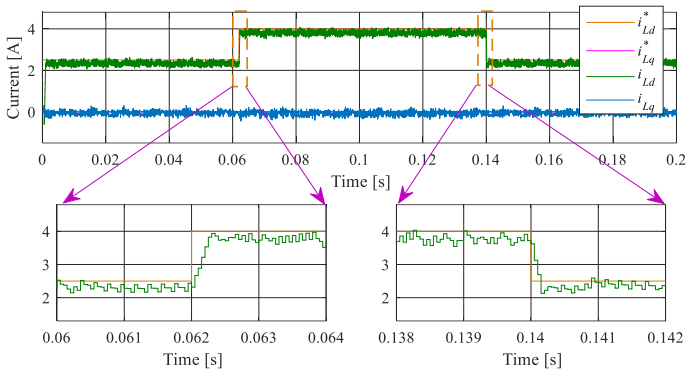
4.2.1.3 Performance with switching constraint

The cost function with a constraint of change in switching state of the inverter is considered to compare the system performance for the FCS-MPC. The inclusion of this constraint reduces the number of commutations of power switches that leads to a reduction in switching frequency. Present switching state $\boldsymbol{S}(k)$ is compared with previously applied switching state $\boldsymbol{S}(k\text{-}1)$ to ensure fewer switching commutations for each phase. The cost function with the constraint is formulated as

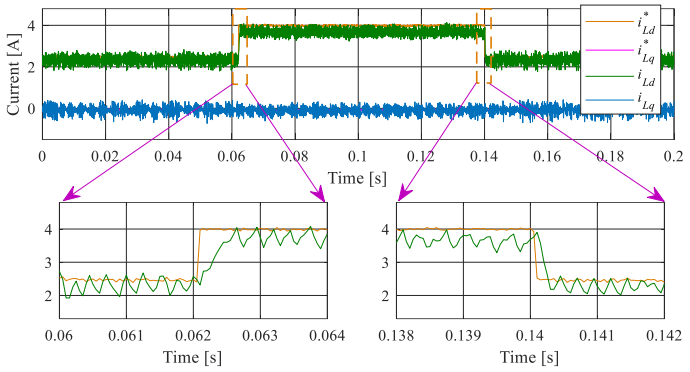
$$g = g_p + \lambda \cdot p \tag{4.10}$$

where g_p is the primary cost function with only current control objective defined in chapter 2 for the FCS-MPC in $\alpha\beta$-frame as $g_{\alpha\beta}$ (2.21) and dq-frame as g_{dq} (2.22), λ is the weighting factor and p is the number of switching commutations defined as

$$p = \sum_x \left| S_x(k) - S_x(k-1) \right|, \quad x = a,b,c \tag{4.11}$$



(a)



(b)

Fig. 4. 5. Load current tracking performance for the FCS-MPC in *dq*-frame with $k_1 = 1$ through (a) simulation, (b) experiment.

The system performance is investigated with the switching state constraint during the simulation and experiment. The system performance with varying λ is examined for average switching frequency f_{sw} as well as percentage THD in the load current where the average f_{sw} is evaluated using the following expression [59]:

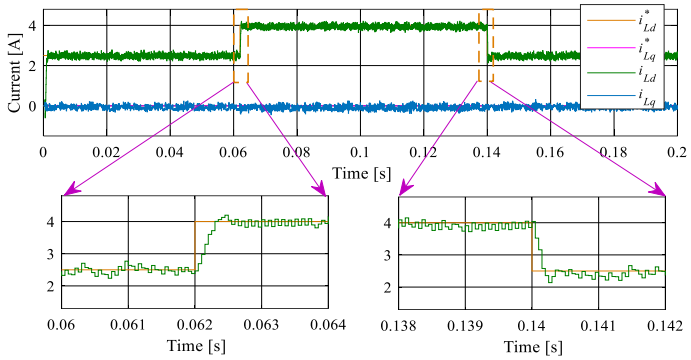
$$f_{sw} = \frac{1}{3}\frac{N_a + N_b + N_c}{T} \tag{4.12}$$

where N_a, N_b, and N_c are the number of switching periods in one switch of the phases *a*, *b*, and *c* of the VSI, respectively and T is the period considered for the calculation of the average f_{sw}.

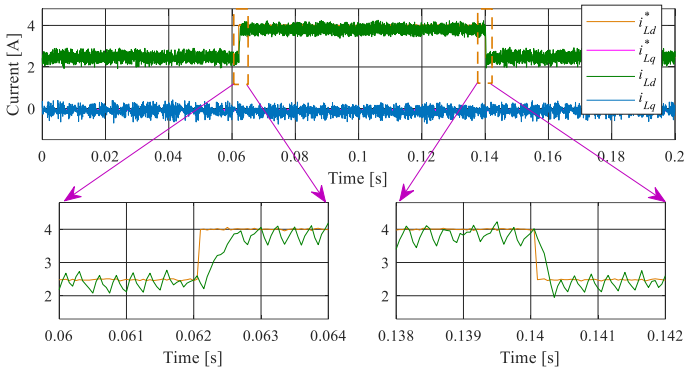
1. *For condition* $\boldsymbol{i}_L = 4$ A: *Adaptive* k_1 *and* $k_1 = 1$

The performance of the FCS-MPC in $\alpha\beta$, as well as *dq* frames for $\boldsymbol{i}_L = 4$ A, are depicted in Fig. 4.7 and Fig. 4.8 for the simulation and experiment results respectively. The average f_{sw} decreases corresponding to an increase in λ, consequently, the harmonic content in the

load current increases. A slightly higher percentage THD is observed corresponding to λ for

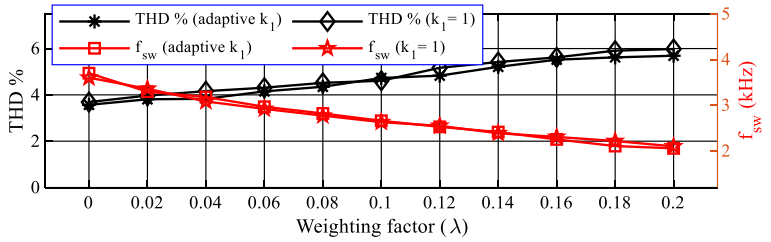


(a)

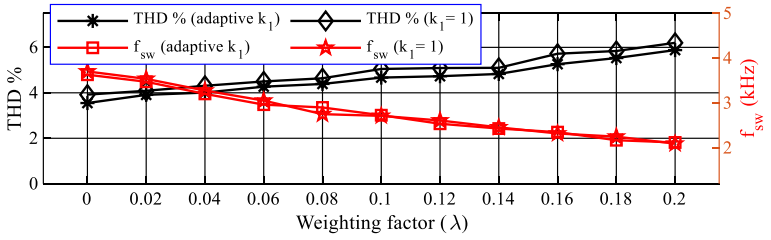


(b)

Fig. 4. 6. Load current tracking performance for the FCS-MPC in *dq*-frame with adaptive k_1 through (a) simulation, (b) experiment.



(a)



(b)

Fig. 4. 7. Average switching frequency (f_{sw}) and percentage THD in load current for $\boldsymbol{i}_L = 4$ A during simulation with the FCS-MPC in (a) $\alpha\beta$-frame, and (b) *dq*-frame.

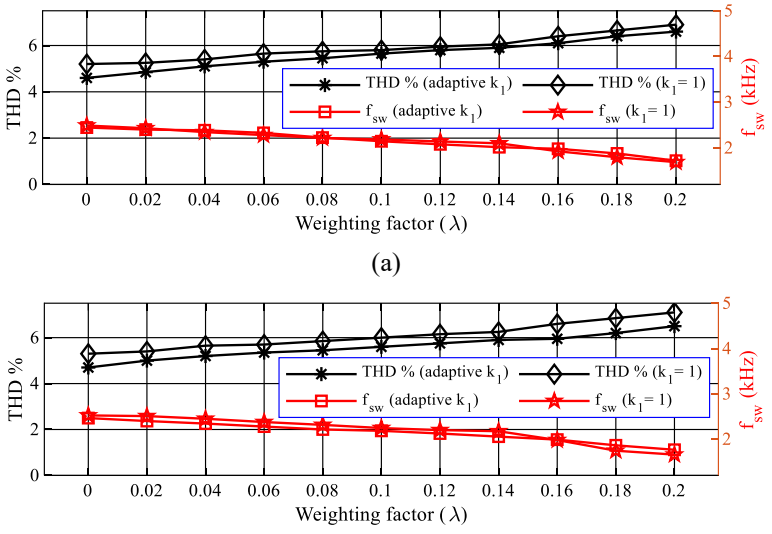


Fig. 4. 8. Average switching frequency (f_{sw}) and percentage THD in load current for $\boldsymbol{i}_L$ = 4 A during experiment with the FCS-MPC in (a) $\alpha\beta$-frame, and (b) dq-frame.

k_1 = 1 as compared to the adaptive k_1 during the simulation as well as the experiment. However, THD is almost the same especially for the value of λ = 0.1 to 0.14 in the simulation as well as the experiment for both the frames.

2. *For condition* $\boldsymbol{i}_L$ = 2.5 A: *Adaptive* k_1 *and* k_1 = 1

Similar to the previous case, the performance in both the frames for $\boldsymbol{i}_L$ = 2.5 A is presented in Fig. 4.9 and Fig. 4.10 for simulation and experiment respectively corresponding to the

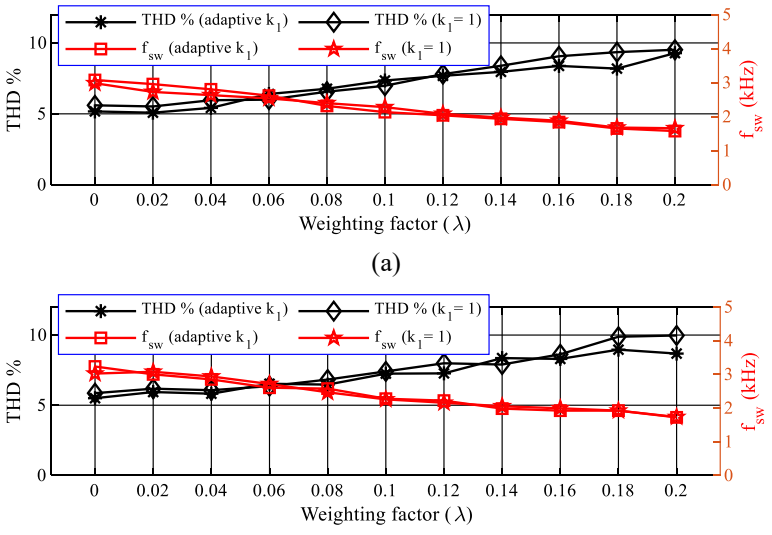
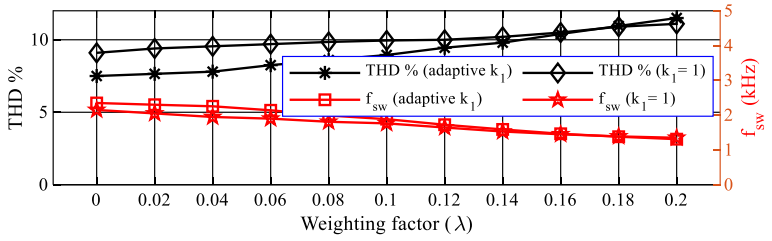
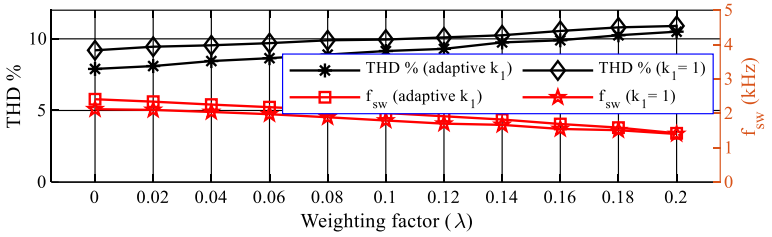


Fig. 4. 9. Average switching frequency (f_{sw}) and percentage THD in load current for $\boldsymbol{i}_L$ = 2.5 A during simulation with the FCS-MPC in (a) $\alpha\beta$-frame, and (b) dq-frame.



(a)



(b)

Fig. 4. 10. Average switching frequency (f_{sw}) and percentage THD in load current for $\boldsymbol{i}_L$ = 2.5 A during experiment with the FCS-MPC in (a) $\alpha\beta$-frame, and (b) dq-frame.

the same range of λ. In the case of the simulation, the gap between THD lines for adaptive k_1 and k_1 = 1 is negligible corresponding to variation in λ. However, the gap between THD lines decreases with the increase in λ for both the frames in the case of the experiment. And, similar to the case of $\boldsymbol{i}_L$ = 4 A, the THD is almost the same for value λ = 0.1 to 0.18. This trend of THD is authenticated through the average f_{sw} corresponding to change in λ and THD increases with the reduction in average f_{sw}.

The controller performance is significantly changed considering the percentage THD in load current for current prediction using fixed, adaptive and approximated value of coefficient k_1 as summarized in Table 4.1 and Table 4.2. In addition, the performance is dependent on constraint for switching frequency reduction that ultimately results in higher percentage THD. However, the switching constraint almost compensates for the effect of current prediction using the approximated value of coefficient k_1 for the higher value of λ.

4.3 Modified Cost Function

The control objectives of an inverter (with *RL* load) using the conventional FCS-MPC is addressed by predicting the load current corresponding to the possible voltage vectors. Nevertheless, this has a high computational burden and it is further increased with the incorporation of constraints. An idea to reformulate the conventional FCS-MPC with the elimination of eight current predictions required corresponding to the eight voltage vectors

in the three-phase two-level VSI was presented in [102] denoted by a simplified FCS-MPC. The reference voltage vector $\boldsymbol{v}_i^*(k)$ was evaluated in each sampling interval once as a single current prediction in the simplified FCS-MPC resulting reduction in the computational burden of the algorithm. The $\boldsymbol{v}_i^*(k)$ can be computed by replacing the predicted load current $\boldsymbol{i}_L(k+1)$ with the reference current $\boldsymbol{i}_L^*(k+1)$ in the expression of $\boldsymbol{i}_L(k+1)$ (2.15) as mentioned in chapter 2 and written below

$$\boldsymbol{i}_L(k+1)=\left(1-\frac{RT_S}{L}\right)\boldsymbol{i}_L(k)+\frac{T_S}{L}\boldsymbol{v}(k)$$

After rearrangement, the expression for $\boldsymbol{v}_i^*(k)$ can be written as:

$$\boldsymbol{v}_i^*(k)=\left(R-\frac{L}{T_S}\right)\boldsymbol{i}_L(k)+\frac{L}{T_S}\boldsymbol{i}_L^*(k+1) \tag{4.13}$$

The $\boldsymbol{v}_i^*(k)$ in dq-frame of the FCS-MPC with feed-forward decoupling of d and q components of the current can be formulated by rearranging (2.19) and represented in rotating d and q components as follows:

$$v_{id}^*(k)=\left(R-\frac{L}{T_S}\right)i_{Ld}(k)+\frac{L}{T_S}i_{Ld}^*(k+1)-\omega^* L i_{Lq}(k) \tag{4.14a}$$

$$v_{iq}^*(k)=\left(R-\frac{L}{T_S}\right)i_{Lq}(k)+\frac{L}{T_S}i_{Lq}^*(k+1)+\omega^* L i_{Ld}(k) \tag{4.14b}$$

The $v_{id}^*(k)$ and $v_{iq}^*(k)$ will be computed once in each sampling interval T_S. Then, a cost function is required to be designed to identify the one voltage vector nearest to the reference among eight voltage vectors ($\boldsymbol{v}_0$-$\boldsymbol{v}_7$).

4.3.1 Cost function with the constraint of change in switching state

The cost function with the switching constraint (g_{SSW}) in the simplified FCS-MPC can be formulated as

$$g_{SSW}=\lambda_{SP}\cdot g_{SP}+\lambda_{SSW}\cdot p \tag{4.15}$$

where λ_{SP} and λ_{SSW} are the weighting factors corresponding to the constraints of reference voltage vectors and switching state, respectively. The number of switching commutations

p is the same as represented in (4.11). The primary cost function (g_{SP}) in the simplified FCS-MPC can be expressed as

$$g_{SP} = \left\{v_{id}^{*}(k) - v_{id}(k)\right\}^{2} + \left\{v_{iq}^{*}(k) - v_{iq}(k)\right\}^{2} \tag{4.16}$$

The g_{SP} and corresponding g_{SSW} will be computed eight times according to the eight voltage vectors (v_{id}, v_{iq}) in each T_S.

4.3.2 Modified cost function with proposed constraint

The proposed constraint is incorporated considering a concept to retain an identical error profile for few control cycles (T_S) resulting in a reduced number of switching commutations. Moreover, the idea is to incorporate this constraint by using the simplified FCS-MPC to reduce the computational burden. The proposed constraint is designed using (4.13) to represent the current error in the form of computed reference voltage vector $\boldsymbol{v}_i^{*}(k)$. The change in error for instant 'k-1' in the form of computed reference voltage vector (4.17) is used to formulate the proposed novel constraint considering possible voltage vectors.

$$\boldsymbol{v}_i^{*}(k-1) = \frac{L}{T_s}\left[\boldsymbol{i}_L^{*}(k) - \left(1 - \frac{RT_S}{L}\right)\boldsymbol{i}_L(k-1)\right] \tag{4.17}$$

where $\boldsymbol{i}_L^{*}(k)$ is the reference load current at instant 'k' and $\boldsymbol{i}_L(k\text{-}1)$ is the measured current at instant 'k-1'. The error between the previously computed reference voltage vector and the possible voltage vectors is incorporated inside the modified cost function.

The cost function with the proposed constraint of change in reference voltage vector is defined as

$$g_{SE} = \lambda_{SP} \cdot g_{SP} + \lambda_{SE} \cdot \left\{\left|e_{Sd}\right| + \left|e_{Sq}\right|\right\} \tag{4.18}$$

where $e_S = v_i^{*}(k-1) - v_i(k)$.

The objective behind the inclusion of the proposed constraint is to reduce the average switching frequency as well as improve the SSE using a single constraint. A general schematic diagram of the MFCS-MPC algorithm for a three-phase VSI system is represented in Fig. 4.11 to summarize the load current control in the rotating dq frame.

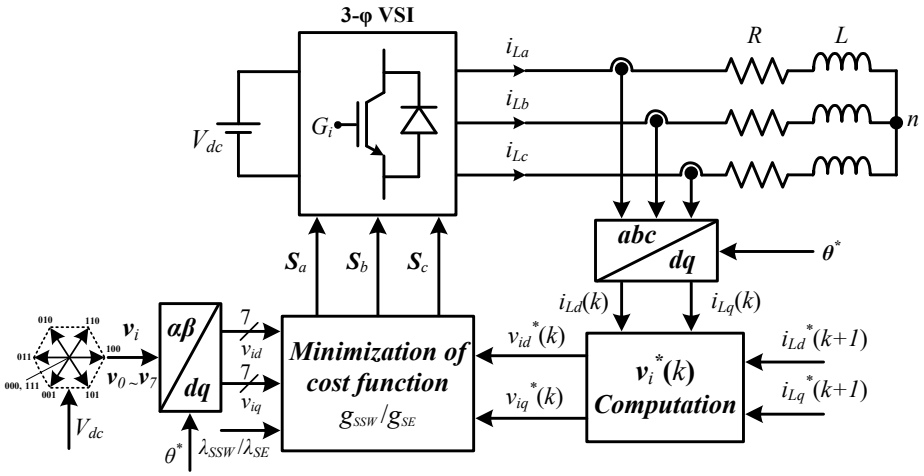


Fig. 4. 11. Schematic diagram of load current control using the simplified FCS-MPC in *dq*-frame using switching state constraint and the proposed constraint.

The controller formulation in only the *dq*-frame is considered that facilitates flexible controller performance analysis, especially in the SSE performance analysis due to the continuous load current references required for the system implementation. The SSE is one of the relevant indices for the performance evaluation of a control scheme. The SSE is calculated by using the following expression [59]

$$\text{SSE} = \frac{\sqrt{\overline{e_d}^2 + \overline{e_q}^2}}{\sqrt{i_{Ld}^{*\,2} + i_{Lq}^{*\,2}}} \times 100 \tag{4.19}$$

The $\overline{e_d}$ and $\overline{e_q}$ are the mean values of the control error for *d* and *q* axis, respectively and calculated according to the following relations

$$\overline{e_d} = \frac{1}{N}\sum_j \left\{ i_{Ld}^*(j) - i_{Ld}(j) \right\} \tag{4.20a}$$

$$\overline{e_q} = \frac{1}{N}\sum_j \left\{ i_{Lq}^*(j) - i_{Lq}(j) \right\} \tag{4.20b}$$

where *N* is the number of current samples considered for the calculation of the SSE.

4.3.3 System performance

The system performance is analyzed using the simulation through XSG-based modelling of the FCS-MPC considering both cost functions with the change in switching state constraint (4.15) as well as the proposed constraint (4.18). To evaluate the robustness of

the FCS-MPC algorithms, a step-change in reference current is considered for the demonstration of dynamic performance. A comparative analysis is presented between the change in switching state constraint and proposed novel constraint considering indices SSE as well as average switching frequency. The change in weighting factors for the aforementioned constraints are considered to demonstrate the effect on switching frequency and load current THDs. Moreover, the different load currents and sampling time are considered to evaluate SSE considering similar load current ripples.

4.3.3.1 Dynamic performance

In order to investigate the performance of the system, the experimental results are presented depicting reference current tracking in Fig. 4.12 for the simplified FCS-MPC

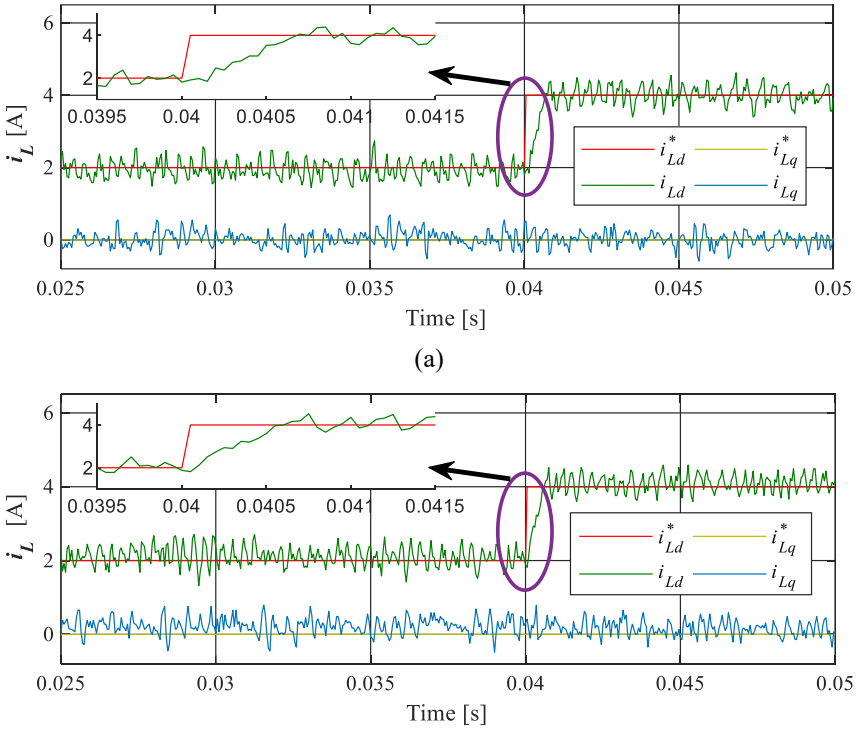


Fig. 4. 12. Experimental results of load current tracking for the simplified FCS-MPC (a) change in switching state constraint (λ_{SSW} = 0.175), (b) proposed constraint (λ_{SE} = 3.5).

considering the change in switching state constraint (g_{SSW}) as well as the proposed novel constraint (g_{SE}). The dynamic performance of the FCS-MPC is demonstrated through a step-change in the reference current from 2 A to 4 A at 0.04s. The reference current tracking, as well as transient response, is observed for the specific values of respective

weighting factors (λ_{SSW}, λ_{SE}) of the constraints considering similar current ripples. The two constraints present a similar tracking performance, however, better dynamic performance is observed in the case of the proposed novel constraint.

4.3.3.2 Average switching frequency analysis

The effect of varying weighting factors corresponding to the constraints in the simplified FCS-MPC is analyzed to investigate one of the objectives that is average switching frequency f_{sw} reduction. The system performance with varying weighting factors is examined during the simulation and experiment for average f_{sw} and corresponding percentage THD of the load current $\boldsymbol{i}_L$ ($\boldsymbol{i}_L$ = 4 A). The average f_{sw} and the percentage THD in $\boldsymbol{i}_L$ vs weighting factors (λ_{SSW}, λ_{SE}) are presented through line graphs in Fig. 4.13 for the simplified FCS-MPC.

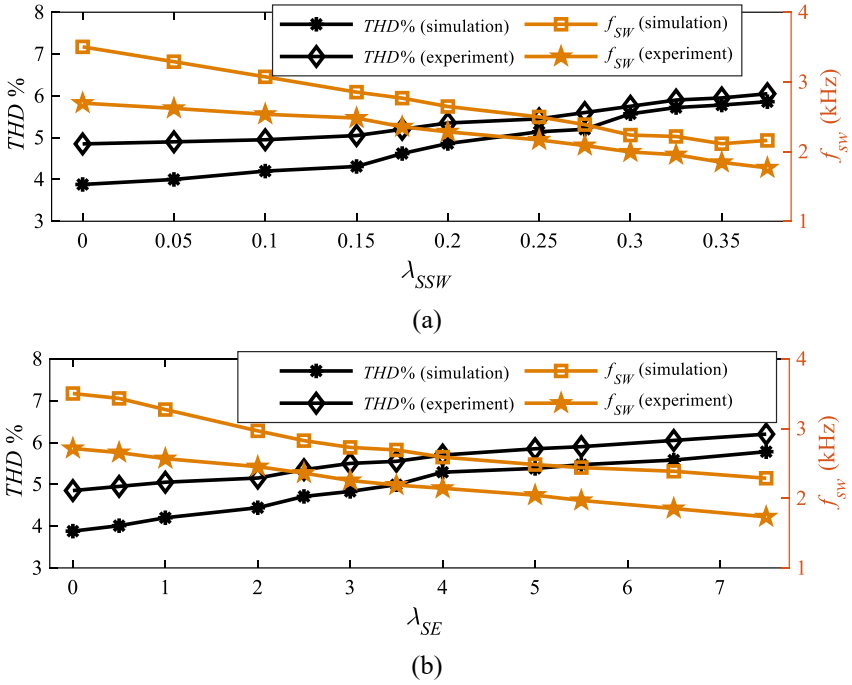


Fig. 4. 13. Average switching frequency and the percentage THD in the load current vs weighting factors (λ_{SSW}, λ_{SE}) for simplified FCS-MPC (a) change in switching state constraint, (b) proposed constraint.

A decreasing trend of average f_{sw} is observed with the increase in weighting factors, consequently, the harmonic content in the $\boldsymbol{i}_L$ increases with the weighting factors. Nevertheless, a significant difference between the simulation and experimental lines of average fsw as well as the percentage THD of $\boldsymbol{i}_L$ can be observed. The difference between simulation and experimental results maybe because of the ideal power switches and non-

realistic load properties in the simulation model of the VSI system with *RL* load. Furthermore, as the trend moves towards the lower average f_{sw} consequently higher THD, the simulation and experimental results become almost similar for both the cases.

4.3.3.3 Steady-state error analysis

The steady-state error (SSE) in the load current tracking is analyzed through the simulation as well as experiment for the simplified FCS-MPC with the change in switching state and the proposed constraints. The comparative SSE analysis is performed through bar graphs between the two constraints. The load current and the sampling time T_S having a significant impact on SSE. Therefore, for a clear demonstration of the SSE performance, different values of load current $\boldsymbol{i}_L$ (2, 2.5, 3, 3.5, 4A) are used for simulation as well as experiment. In addition, two cases of T_S (50, 100 µs) are considered. A similar load current THDs, obtained for varying weighting factors corresponding to respective constraints are considered for the comparative analysis.

1. *For* T_S = 50 µs: At first, the SSE performance in Fig. 4.14 is demonstrated considering simplified FCS-MPC without constraint ($\lambda_{SSW} = 0$, $\lambda_{SE} = 0$) for the simulation and experimental results. There is an increasing trend in the SSE as the load current decreases for both simulation and experiment, however, an increased SSE is observed during experiments.

Further, the SSE performance in Fig. 4.15 and Fig. 4.16 is demonstrated for simulation and experimental results respectively considering simplified FCS-MPC with the change in switching state (g_{SSW}) and proposed (g_{SE}) constraint. The proposed novel constraint has better SSE performance for the considered cases of similar percentage THDs corresponding to the weighting factor of respective constraints. In addition, this has

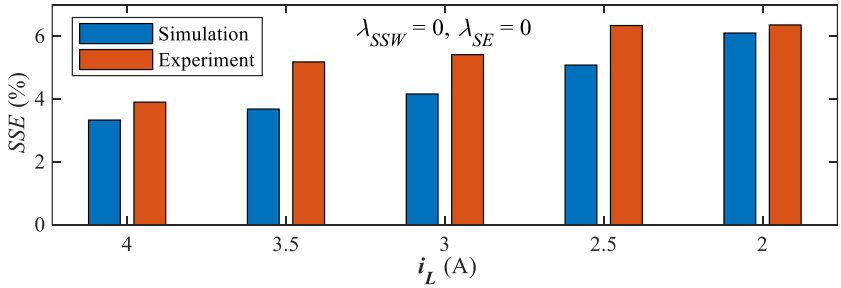


Fig. 4. 14. SSE performance of simplified FCS-MPC without constraint for T_S = 50 µs.

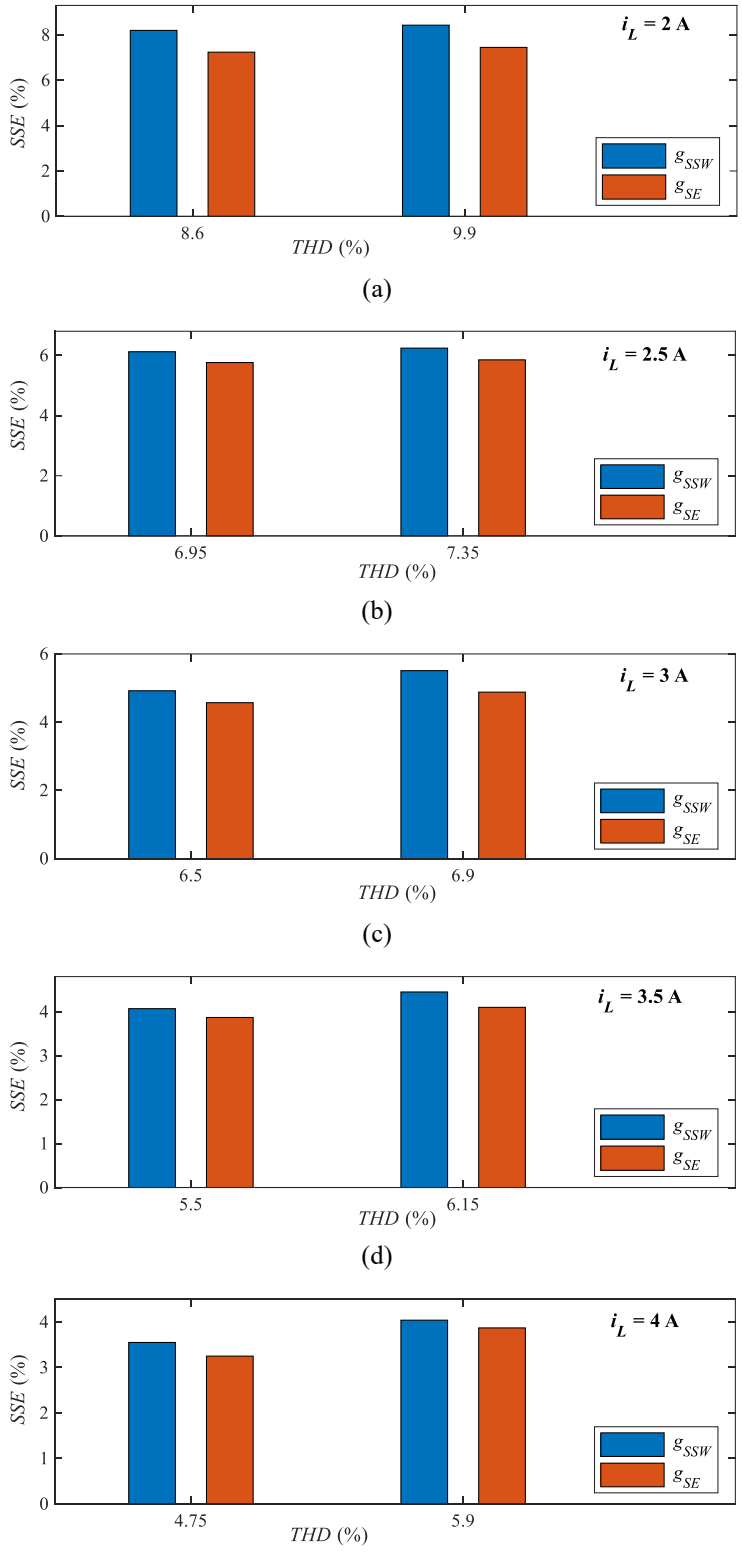


Fig. 4. 15. Simulation results (T_S = 50 µs) of SSE performance for simplified FCS-MPC with the change in switching state constraint (g_{SSW}) and the proposed constraint (g_{SE}): (a) $\boldsymbol{i}_L$ = 2 A, (b) $\boldsymbol{i}_L$ = 2.5 A, (c) $\boldsymbol{i}_L$ = 3 A, (d) $\boldsymbol{i}_L$ = 3.5 A, and (e) $\boldsymbol{i}_L$ = 4 A.

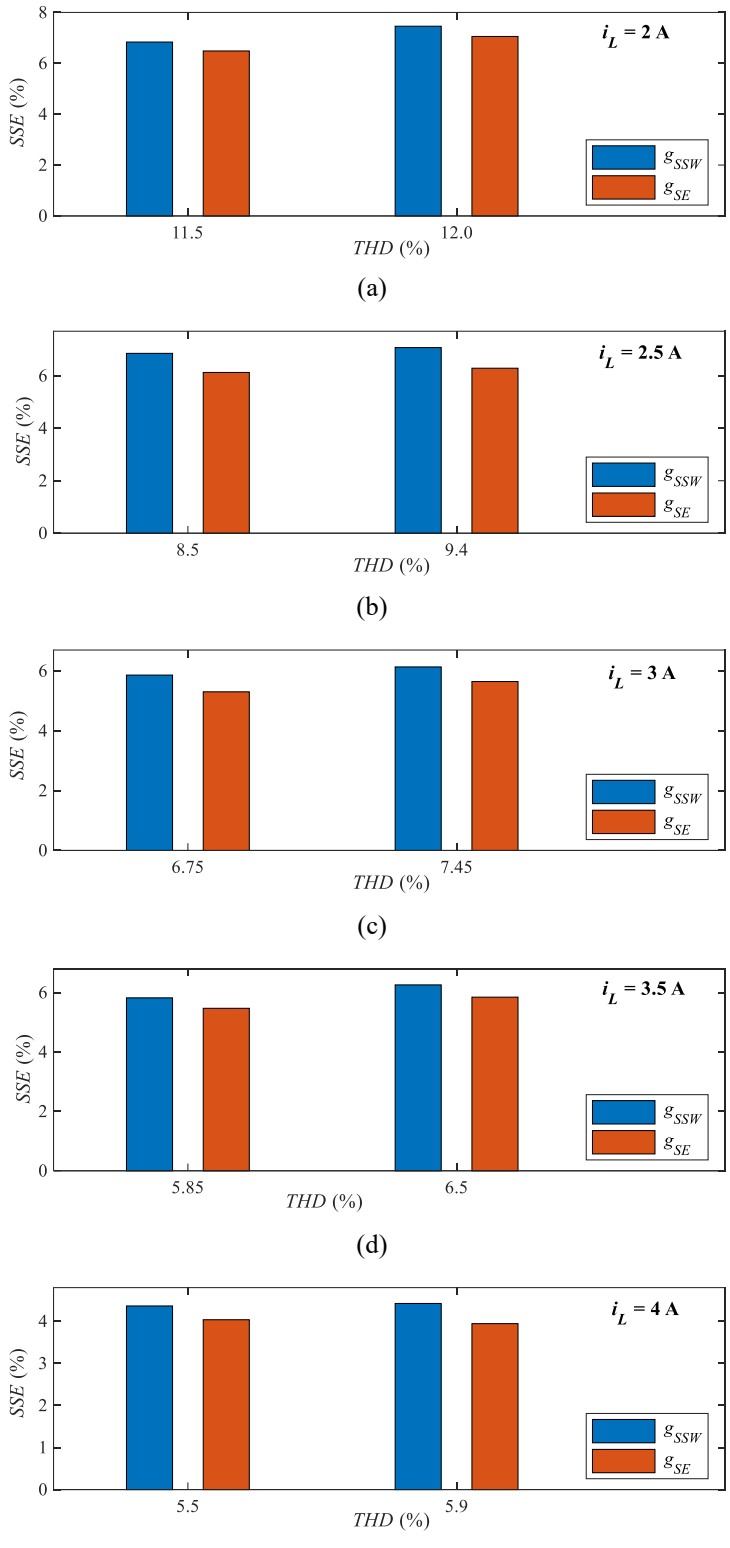


Fig. 4. 16. Experimental results (T_S = 50 µs) of SSE performance for simplified FCS-MPC with the change in switching state constraint (g_{SSW}) and the proposed constraint (g_{SE}): (a) i_L = 2 A, (b) i_L = 2.5 A, (c) i_L = 3 A, (d) i_L = 3.5 A, and (e) i_L = 4 A.

demonstrated better SSE performance for almost all the cases of considered load currents. The SSE performance of proposed novel constraint based on simplified FCS-MPC is authenticated for simulation as well as experimental results.

2. *For* T_S = 100 µs: Similarly, the SSE performance in Fig. 4.17 is demonstrated for T_S = 100 µs without constraint (λ_{SSW} = 0, λ_{SE} = 0). The similar trend of increasing SSE is observed as the load current decreases.

Furthermore, the SSE performance in Fig. 4.18 and Fig. 4.19 is demonstrated for simulation and experimental results respectively for the simplified FCS-MPC with two constraints. Similar to the T_S = 50 µs, the SSE performance for the proposed novel constraint is better for the considered cases of similar percentage THDs. This has demonstrated significantly better SSE performance for all the cases of considered load currents and authenticated by simulation as well as experimental results.

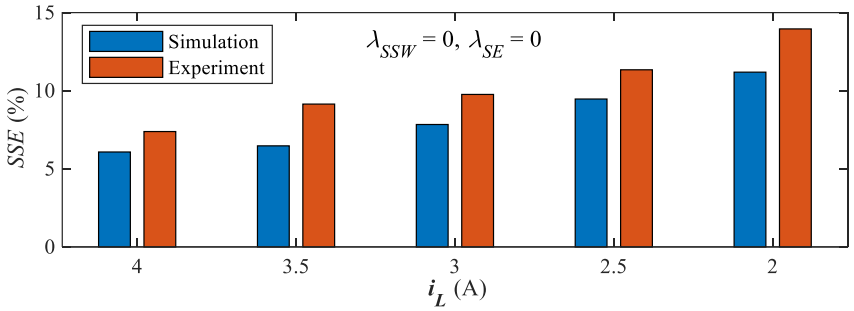
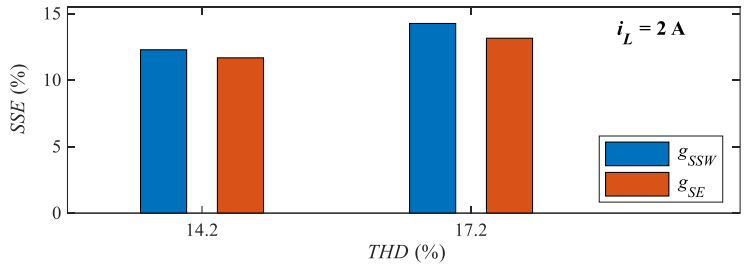
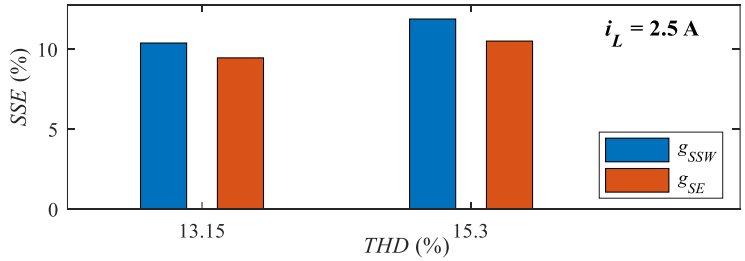


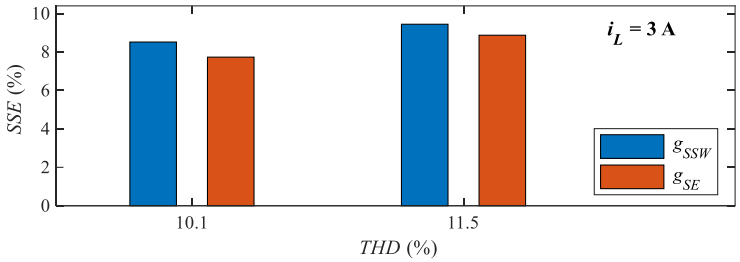
Fig. 4. 17. SSE performance of simplified FCS-MPC without constraint for T_S= 100 µs.



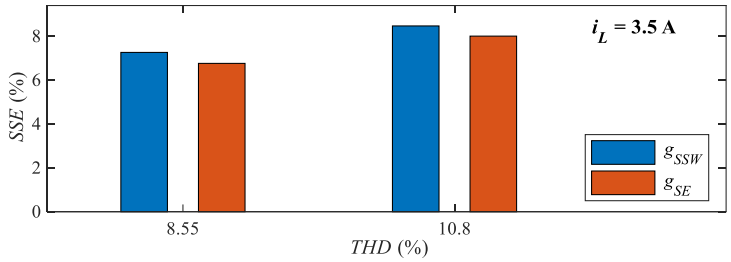
(a)



(b)



(c)



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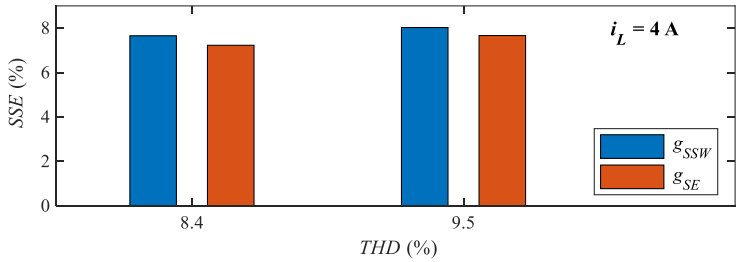
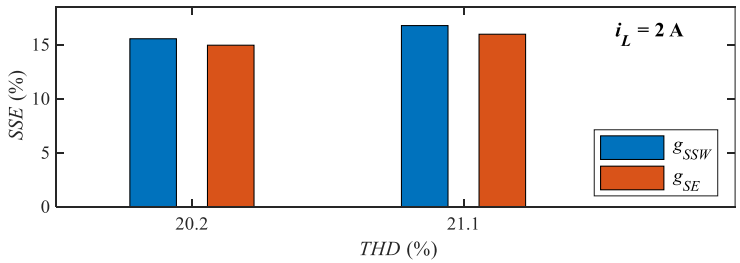
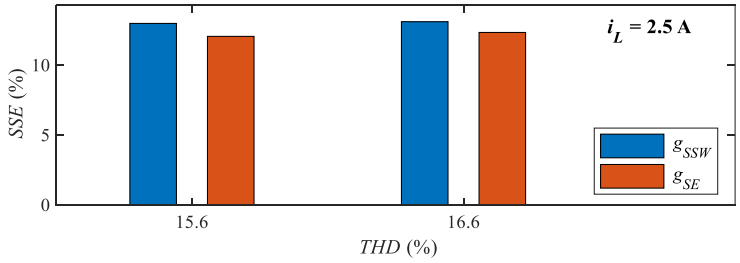


(e)

Fig. 4. 18. Simulation results (T_S = 100 µs) of SSE performance for simplified FCS-MPC with the change in switching state constraint (g_{SSW}) and the proposed constraint (g_{SE}): (a) $\boldsymbol{i}_L$ = 2 A, (b) $\boldsymbol{i}_L$ = 2.5 A, (c) $\boldsymbol{i}_L$ = 3 A, (d) $\boldsymbol{i}_L$ = 3.5 A, and (e) $\boldsymbol{i}_L$ = 4 A.



(a)



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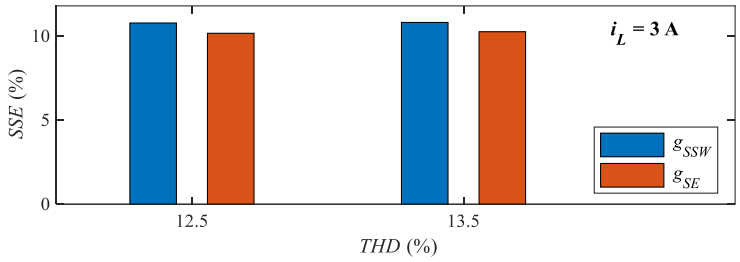

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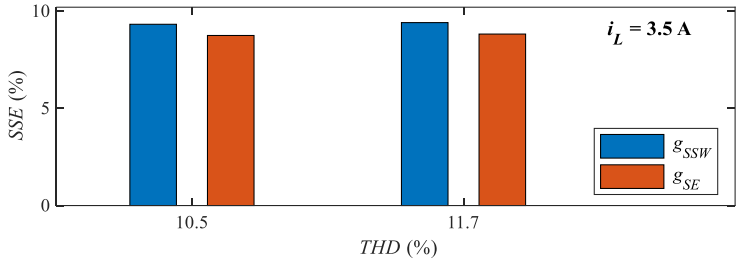

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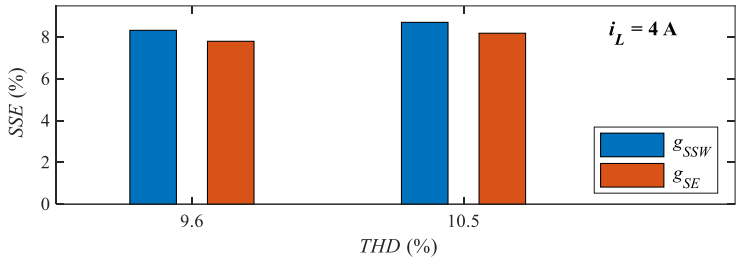


(e)

Fig. 4. 19. Experimental results (T_S = 100 µs) of SSE performance for simplified FCS-MPC with the change in switching state constraint (g_{SSW}) and the proposed constraint (g_{SE}): (a) $\boldsymbol{i}_L$ = 2 A, (b) $\boldsymbol{i}_L$ = 2.5 A, (c) $\boldsymbol{i}_L$ = 3 A, (d) $\boldsymbol{i}_L$ = 3.5 A, and (e) $\boldsymbol{i}_L$ = 4 A.

4.4 Summary

This chapter presented an approach to compensate for the effect of change in system parameters in the physical environment. The change in load resistance was considered to update the predictive model (called as, adaptive predictive model) according to the updated value of a coefficient k_1 used for the prediction (adaptive k_1) while keeping the exact value of the load inductance. To verify the performance of the proposed approach, the exact predictive model with k_1 = 0.95 and an approximated predictive model with k_1 = 1 were also considered for the system implementation and in-depth comparative analysis.

The controller performance is authenticated through simulation as well as experimental results for FPGA-based implementation of the FCS-MPC in $\alpha\beta$ and dq frames

considering the dynamic behavior during transients. Furthermore, the system performance with exact (k_1 = 0.95), approximate (k_1 = 1), and adaptive values of coefficient k_1 was verified during the simulation as well as experiment considering load current THD and average switching frequency. A constraint of a change in switching state is also considered for the in-depth analysis and understanding of the effect of current prediction using adaptive k_1 as well as k_1 = 1. The effect of switching constraint was analyzed considering the performance indices average switching frequency (f_{sw}) and current THD with varying weighting factor (λ). A reduction in average f_{sw} was observed with increasing λ, however, the THD in load current was increased with λ.

A modified cost function based on a novel constraint capable of improving steady-state error (SSE) together with a reduction in the average switching frequency was presented that is authenticated by the simulation as well as experimental results. The simplified FCS-MPC is used for the performance verification by incorporating constraints of change in switching state and proposed novel constraint. Considering the effect of low sampling on SSE, the proposed method demonstrate the better SSE for low sampling (T_S = 100 μs) as well for various load current conditions. The proposed novel constraint demonstrates better transient performance considering the system dynamics for a step-change in load current.

There is a decreasing trend of the average switching frequency consequently increasing trend of the percentage load current THD corresponding to weighting factors of the respective constraints for the simplified FCS-MPC. However, the computational burden of the simplified FCS-MPC scheme is less as compared to the conventional FCS-MPC because of the elimination of large calculations in current predictions.

Chapter 5

FPGA RESOURCE OPTIMIZATION

5.1 Introduction

Every FPGA has a set of programmable logic, I/O, and memory resources. The FPGA resources consist of configurable logic blocks (CLBs) which are the main constituent to implement code on the FPGA. A CLB element comprises a pair of slices and a slice contains LUTs and flip-flops [103], [104]. According to the family of the FPGA chip, the number of LUTs and flip-flops in a single slice are different. For instance, there are four LUTs and eight flip-flops in a slice considering 7 series FPGAs [30]. In addition, there is a major component of the FPGA resources, called DSP slices, that are mainly used to implement signal processing functions. The main constituents of a DSP slice are signed multipliers, adder/accumulator, arithmetic logic unit (ALU) logic functions and many more [105].

FPGA resource utilization is another key aspect of FPGA-based system control implementation. There is a possibility to adopt different implementation strategies for a specific FPGA implementation approach to enhance resource utilization. In this way, the MBD approach can be advantageous by allowing different implementation strategies under the same environment and to compare the FPGA resource utilization. In this work, the analytical implementation strategies using an MBD approach are proposed considering the reduction in the FPGA resource utilization for fully parallel implementation of the FCS-MPC algorithm. A comparative analysis of FPGA resource utilization is considered corresponding to the predictive model coefficient of the FCS-MPC for a three-phase VSI system with RL load. Moreover, resource utilization for controller implementation using stationary $\alpha\beta$ and rotating dq reference frames is used for in-depth analysis. The FPGA

resource utilization is compared considering fixed (k_1 = 0.95), approximated (k_1 = 1) as well as adaptive values of a coefficient k_1 used for current prediction in $\alpha\beta$ and dq frames.

The following strategies are considered for the modelling of the FCS-MPC algorithm in both $\alpha\beta$ and dq frame:

- Fundamental mathematical blocks for the current prediction and cost function computation
- MCode block for the current prediction and cost function computation
- Approximation for the coefficient k_1
- Adaptive k_1

5.2 Implementation Strategy

The implementation strategy is crucial for the time required for computation and resource utilization. There is a possibility to reduce the required FPGA resources significantly by using an appropriate implementation strategy that may create the possibility of system implementation using smaller FPGAs. The following are the objectives of analytical implementation strategies mentioned in the previous subsection:

- FPGA resource: minimization of resource utilization (LUTs, flip-flops, DSP slices) required for fully parallel implementation.
- Usability: the implementation strategy with minimum resource utilization can be used for semi-parallel/sequential implementation.
- Trade-off: maintaining appropriate control quality and computational speed with reduced resource utilization.

In addition, the optimum strategy can be beneficial to develop various controllers for the FPGA-based system implementation. The implementation strategies are described as follows:

5.2.1 Fundamental mathematical blocks

In this strategy, the future current predictions and cost function computations are performed using fundamental mathematical XSG blocks: AddSub, CMult, Mult, Absolute. AddSub block performs the addition and subtraction for two inputs, CMult block performs the function of gain multiplier for a single input, Mult block performs the function of

multiplication for two inputs and Absolute block performs the function of absolute value computation for real and imaginary quantities in (2.21) and (2.22) described in chapter 2. The coefficients (k_1, k_2, k_3) used for future current predictions are provided by Xilinx Constant blocks with an appropriate number of bits and binary point settings for fixed-point number representation.

5.2.2 MCode blocks

In this strategy, the future current predictions and cost function computations are performed together through a single MCode block corresponding to each voltage vector using MATLAB code. This strategy is further subdivided into two cases based on the coefficients (k_1, k_2, k_3):

Case-I: coefficients defined as inputs to MCode blocks

Case-II: coefficients defined inside MCode blocks

The MATLAB code for the prediction (Ipred_real and Ipred_img) and cost computation using current errors (x and y) in $\alpha\beta$-frame for case-I and case-II is mentioned in Table 5.1 and 5.2, respectively.

The values of k_1, k_2 are defined inside the MATLAB code in case-II using a command xfix that is used for the fixed-point number representation. Similarly, the MATLAB codes

Table 5. 1. MATLAB code for the prediction and cost computation in $\alpha\beta$-frame for case-I

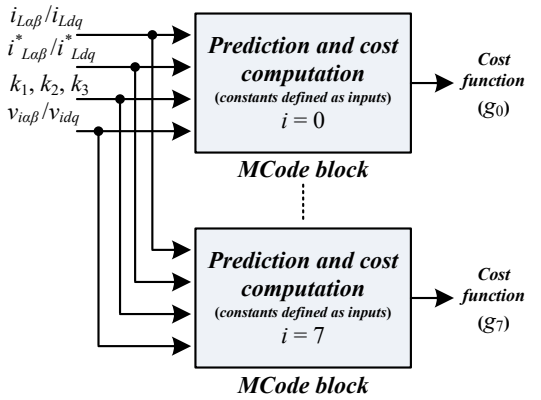
MATLAB code: **Case-I**

```
1:  function [cost] = mpc_case-I (Im_real, Im_img, Iref_real, Iref_img, k1, k2, v_real, v_img)
2:  Ipred_real = k1*Im_real + k2*v_real;
3:  Ipred_img = k1*Im_img + k2*v_img;
4:  x = Iref_real – Ipred_real;
5:  y = Iref_img – Ipred_img;
6:      if (x<0)
7:          mod_x = – x;
8:      else
9:          mod_x = x;
10:     end
11:     if (y<0)
12:         mod_y = – y;
13:     else
14:         mod_y = y;
15:     end
16: cost = mod_x + mod_y;
17: end
```

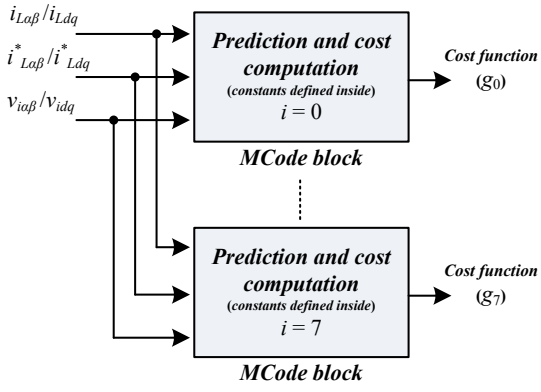
Table 5. 2. MATLAB code for the prediction and cost computation in $\alpha\beta$-frame for case-II

MATLAB code: **Case-II**

```
1:  function [cost] = mpc_case-II (Im_real, Im_img, Iref_real, Iref_img, v_real, v_img)
2:  k1 = xfix({xlSigned, 10, 8, xlRound, xlWrap}, 0.95);
3:  k2 = xfix({xlSigned, 13, 13, xlRound, xlWrap}, 0.005);
4:  Ipred_real = k1*Im_real + k2*v_real;
5:  Ipred_img = k1*Im_img + k2*v_img;
6:  x = Iref_real – Ipred_real;
7:  y = Iref_img – Ipred_img;
8:      if (x<0)
9:          mod_x = – x;
10:     else
11:         mod_x = x;
12:     end
13:     if (y<0)
14:         mod_y = – y;
15:     else
16:         mod_y = y;
17:     end
18: cost = mod_x + mod_y;
19: end
```



(a)



(b)

Fig. 5. 1. Development methodologies for the FCS-MPC in XSG using MCode block (a) case-I, (b) case-II.

for the case-I and case-II of the FCS-MPC in *dq*-frame are designed using the coefficients k_1, k_2, and k_3 according to the codes designed for the FCS-MPC in $\alpha\beta$-frame mentioned above. The development methodologies are presented in Fig. 5.1 for case-I (Fig. 5.1(a)) and case-II (Fig. 5.1(b)). An additional case (case-III) is considered for the resource utilization in the current prediction using adaptive k_1 where other coefficients defined inside the MCode block like case-II.

5.3 Resource Utilization

The FPGA resource utilization considering implementation strategies mentioned in the previous section are listed in Table 5.3 and 5.4 for the FCS-MPC in $\alpha\beta$ and *dq* coordinates, respectively. To select the optimum design strategy, only two logic indices LUTs and DSP slices need attention because the number of Flip-flops are the same considering $\alpha\beta$-frame as well as *dq*-frames.

Table 5. 3. FPGA resource utilization for the development of the FCS-MPC in $\alpha\beta$-frame.

Logic utilization indices	*Fundamental Mathematical Blocks*			*MCode Block*				
				Case-I		*Case-II*		*Case-III*
	$k_1 = 0.95$	$k_1 = 1$	*Adaptive* k_1	$k_1 = 0.95$	$k_1 = 1$	$k_1 = 0.95$	$k_1 = 1$	*Adaptive* k_1
LUTs (53200)	5732 (11%)	4799 (9%)	6546 (12%)	4364 (8%)	3804 (7%)	4896 (9%)	3794 (7%)	5488 (10%)
Flip-flops (106400)	549 (1%)	549 (1%)	1551 (2%)	549 (1%)	549 (1%)	549 (1%)	549 (1%)	1551 (2%)
DSP slices (220)	21 (10%)	19 (9%)	26 (12%)	25 (11%)	19 (9%)	19 (9%)	19 (9%)	27 (12%)

Table 5. 4. FPGA resource utilization for the development of the FCS-MPC in *dq*-frame.

Logic utilization indices	*Fundamental Mathematical Blocks*			*MCode Block*				
				Case-I		*Case-II*		*Case-III*
	$k_1 = 0.95$	$k_1 = 1$	*Adaptive* k_1	$k_1 = 0.95$	$k_1 = 1$	$k_1 = 0.95$	$k_1 = 1$	*Adaptive* k_1
LUTs (53200)	5017 (9%)	5004 (9%)	5489 (10%)	8534 (16%)	8304 (16%)	9967 (19%)	8072 (15%)	9133 (17%)
Flip-flops (106400)	804 (1%)	804 (1%)	1806 (2%)	804 (1%)	804 (1%)	804 (1%)	804 (1%)	1806 (2%)
DSP slices (220)	66 (30%)	62 (28%)	66 (30%)	86 (39%)	74 (34%)	24 (11%)	24 (11%)	32 (15%)

5.3.1 Coefficient k_1: fixed ($k_1 = 0.95$) and approximated ($k_1 = 1$)

The coefficient k_1 is used in future current prediction using (2.17) and (2.19) as mentioned in chapter 2 for $\alpha\beta$ and dq frames, respectively. The value of k_1 depends on the load parameters (R, L) and sampling time (T_S). The exact value of k_1 is 0.95 based on the parameters (R = 10 Ω, L = 10 mH and T_S = 50 µs) considered for simulation and experimental validations. In the case of $k_1 = 0.95$, the number of bits 10 and binary points 8 are specified and provides the coefficient value of 0.9492187 that utilizes significant FPGA resources. The approximation ($k_1 = 1$) can be opted considering the reduction in FPGA resource utilization due to the omission of the required bits and the multiplier used to multiply the exact value of k_1. Consequently, the required bits and the multipliers directly reduce the LUTs and DSP slices, respectively. However, the performance with $k_1 = 1$ is poor as demonstrated in chapter 4.

In case-II of MCode block, the equal number of DSP slices are required for both the subcases $k_1 = 0.95$ and 1, however, the required number of LUTs for $k_1 = 0.95$ is slightly higher as required for $k_1 = 1$. In the case of the FPGA implementation using controller development in $\alpha\beta$-frame, both cases (case-I and II) of MCode with $k_1 = 1$ are the optimum solutions, however, considering better controller performance based on current prediction using an exact value of k_1 with the cost of slightly increased LUTs, case-II of MCode block with $k_1 = 0.95$ can be the optimum choice.

On the other hand, for the controller development in the dq-frame, case-II of MCode block is an optimum strategy due to the least percentage utilization of DSP slices among all the individual resource indices. Although the LUTs requirement has reduced significantly in the case of the development using fundamental mathematical blocks, the required DSP slices have increased approximately 3 times. Furthermore, the FPGA resource utilization for the development of the FCS-MPC in dq-frame is even higher as compared to $\alpha\beta$-frame due to the additional coordinate transformation ($\alpha\beta$ to dq) for voltage vector including measured current, reference phase angle θ^* generation using CORDIC SINCOS and an extra effort for computation of feed-forward term used for decoupling.

5.3.2 Adaptive k_1

The adaptive k_1 is used in future current prediction using (2.17) and (2.19) as mentioned in chapter 2 for $\alpha\beta$ and dq frames, respectively as well as (4.8) as mentioned in chapter 4. In the case of the controller development using adaptive k_1, resource utilization is significantly higher than the optimum design cases (MCode block: case-II) in both $\alpha\beta$-frame as well as dq-frames. However, considering the updated predictive model corresponding to the load changes, the controller performance is better for the controller development using adaptive k_1 as demonstrated in chapter 4. Moreover, a trade-off between controller performance and the FPGA resource utilization can be a better choice to decide an appropriate implementation strategy corresponding to the system application.

5.4 Summary

The real-time system implementation using FPGA requires a set of FPGA resources to design the digital logic for the controller. This chapter presented an approach towards the optimum FPGA resource based on an analytical implementation strategy. The FCS-MPC was developed through an MBD approach of XSG considering both $\alpha\beta$ and dq coordinates. The two implementation strategies, fundamental mathematical blocks and MCode blocks were used for the current prediction and cost computation. For the system development using the MCode block, two possible cases were also considered where the coefficients used for the current prediction can be defined as inputs to the MCode block (Case-I) or can be defined inside the MCode block (Case-II). Moreover, three different values of the coefficient k_1: fixed ($k_1 = 0.95$) approximated ($k_1 = 1$) and adaptive k_1 has opted for the comprehensive analysis of FPGA resource utilization.

A significant reduction is achieved (around 65% in DSP Slices) in overall FPGA resource requirement in dq coordinate for system development through MCode block case-II (coefficients defined inside the MATLAB code) of Xilinx blockset. Especially, system development through an approximated value of a coefficient ($k_1 = 1$) provides a further reduction in FPGA resources. Furthermore, resources are optimized using case-II for adaptive current prediction (around 50% reduced DSP Slices). However, a trade-off between the controller performance (presented in chapter 4) and optimum resource utilization is vital for the cost-performance ratio.

Chapter 6

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

The primary objective of this work was to develop a system for the intuitive implementation of the FCS-MPC algorithm using an FPGA. The FCS-MPC is one of the categories of a wide family of the MPC that has been utilized for the power converters and drives due to its appealing characteristics especially the one to handle multiple control variables simultaneously. However, FCS-MPC has to deal with some issues such as computational delay during real-time implementation, a variable switching frequency, high switching frequency requirements for enhanced performance, an issue of model parameter mismatch and a non-zero steady-state error. In this work, different approaches were proposed to tackle some issues of the FCS-MPC.

In chapter 2, the fundamental principle of the FCS-MPC was discussed considering the controller implementation in two well-known coordinates: stationary $\alpha\beta$ and rotating dq. The two major computation steps of the FCS-MPC implementation: the predictive model and the cost function were formulated considering the load current control objective of the three-phase two-level VSI system.

To overcome the computational delay issue of the FCS-MPC, the controller was implemented using an FPGA through the controller development on an MBD platform of a Xilinx digital simulator (XSG) as discussed in chapter 3. The XSG platform facilitates an automatic HDL code generation for the straightforward implementation of the system using FPGA. The MBD platform is considered advantageous for rapid controller development and prototyping using easy debugging by analyzing intermediate responses. The XSG platform facilitates the HIL simulation environment that is an intermediate stage between the software simulation and the actual experimental system implementation. The

XSG modelling of the FCS-MPC in $\alpha\beta$-frame was further used for the HIL simulation using an FPGA considering load current control in a three-phase VSI system with motor load conditions. The controller was developed in MATLAB/Simulink as well as XSG and a comparative analysis was presented through the simulation results to validate the performance with HIL simulation. To demonstrate the features of the MBD platform of XSG, the intermediate responses: minimum cost function and selection of an index number were also presented. Moreover, the performance is validated considering the effect of the sampling time and tracking performance under dynamic conditions.

To validate the performance in a real-time environment, the XSG modelling of the FCS-MPC was utilized to generate the HDL code automatically for the FPGA-based system implementation. The load current control objective of the three-phase VSI system with RL load was considered for the physical system implementation. A comparative analysis between the FCS-MPC in $\alpha\beta$-frame and dq-frame was presented through the simulation as well as the experimental results considering the performance indices of dynamic response and intermediate response. Fast dynamic response of the FCS-MPC was validated during the simulation as well as experiment through load current tracking with step changes in the reference. The FCS-MPC implementation in dq-frame is considered better for the in-depth system analysis. However, system complexity increases as compared to $\alpha\beta$-frame.

An approach to update the predictive model (called as an adaptive predictive model) according to the load changes in the real environment was presented in chapter 4. A coefficient k_1 used in the predictive model was updated according to the proposed approach considering a change in the load resistance while keeping a fixed value of the load inductance. A comparative analysis was presented among the exact model with $k_1 = 0.95$, the approximated model with $k_1 = 1$ and the adaptive model with adaptive k_1 to authenticate the proposed approach. The performance was tested through the simulation as well as experimental results using FPGA-based implementation of the FCS-MPC in both $\alpha\beta$ and dq frames considering performance indices of load current THD and the average switching frequency. The performance was also verified with the constraint of a change in switching state for the effect of the adaptive predictive model (adaptive k_1) as well as an approximated predictive model ($k_1 = 1$). The average switching frequency f_{sw} and the load current THD

were observed with the change in weighting factor λ and demonstrated using line graphs. A reduction in the average f_{sw} was verified with increasing λ, whereas the THD in load current was increased consequently.

The problem of a non-zero steady-state error (SSE) in the FCS-MPC implementation was also considered in this work and a novel constraint-based modified cost function was presented. A simplified FCS-MPC with the elimination of prediction steps was used for the implementation of the FCS-MPC algorithm with the proposed constraint. To verify the performance related to the minimization of SSE, the FCS-MPC was implemented in *dq*-frame with the proposed constraint as well as the constraint of a change in switching state. An improvement in the SSE was observed with the proposed constraint according to the comparative bar graph for the similar current THD values. To validate the effectiveness of the proposed constraint, the SSE was calculated for the different range of current reference values with various current THDs corresponding to λ values. Moreover, the performance is verified using FCS-MPC implementation with a higher (T_S = 50 µs) and lower sampling (T_S = 100 µs).

An approach to optimize the FPGA resources utilized during the FPGA-based system implementation was resented in chapter 5 using analytical implementation strategies. The controller development was performed using fundamental mathematical blocks and MCode blocks individually in XSG as implementation strategies. The two cases were considered for the controller development using MCode blocks where the coefficients k_1, k_2, k_3 defined as inputs to the MCode block (Case-I) and defined inside the MCode block (Case-II). Moreover, the fixed, approximated as well as an adaptive predictive model were considered for the in-depth analysis of FPGA resource utilization in different cases.

A significant reduction is achieved (around 65% in DSP Slices) in overall FPGA resource requirement in *dq* coordinate for system development through MCode block case-II (coefficients defined inside the MATLAB code) of Xilinx blockset. Especially, system development through an approximated value of a coefficient (k_1 = 1) provides a further reduction in FPGA resources, however, large current ripples were observed as compared to the fixed and adaptive predictive model. Furthermore, resources are optimized using case-II for adaptive current prediction (around 50% reduced DSP Slices). The overall

system implementation strategies and performance analysis will be vital for achieving a trade-off between controller performance and FPGA resource utilization.

5.2 Future Scope of Work

The possible future scope of work using the control scheme FCS-MPC is mentioned here.

1. To compensate for the effect of model parameter mismatch in the physical system implementation, an approach was adopted to update the predictive model only according to the change in load resistance. The effect of inductive load parameter variation on controller performance could be a possible future work considering the FPGA-based FCS-MPC implementation using optimum resources.

2. An approach to minimize FPGA resource utilization was presented in this work. This resource optimization approach can be useful for the designing of complex systems that require large FPGA resources such as industrial drive applications.

3. The control scheme was implemented using an FPGA through the controller development in a digital MBD platform of XSG for the load current control of a three-phase two-level VSI system. This MBD approach can pave the path for designing realistic and efficient controllers in Power Electronic converter applications.

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