Bias voltage criteria of gate shielding effect for protecting IGBTs from shoot-through phenomena

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Abstract

In this paper, we propose the criteria of bias voltage from parasitic capacitance and demonstrate the criteria in an experiment with the present IGBT. The bias voltage criteria are theoretically predicted for the new generation IGBT based on the scaling principle. For safe switching, the required gate voltage bias is predicted to be -1.2 V or less for the present IGBTs and -6 V or less is required to completely cancel the gate noise voltage. From the IGBT design, the bias voltage of scaling IGBT requires -2 V to completely cancel the gate noise voltage.

1. New generation IGBT based on scaling principle

IGBTs are widely applied in various power electronics systems, such as electric vehicles, railways and for high-voltage direct current (HVDC) transition, and the market is rapidly expanding.

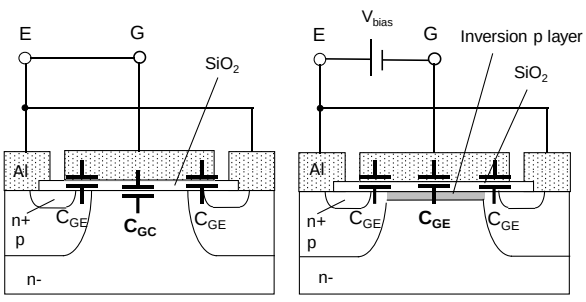
Since 2011, a new generation IGBT based on a scaling principle has been proposed and fabricated experimentally [1-4]. The IGBT features a low collector-emitter saturation voltage (V_{CE}(sat)) and low gate voltage driving. The on-state characteristics of the IGBT have been confirmed by a one-cell device experimentally [4]. The static and dynamic characteristics of larger IGBT chips have not been confirmed yet. From the viewpoint of gate structure, accurate control for the diffusion thickness of the p base layer and flouting p layer is required to lower the electric field stress of gate oxide for high reliability.

The low V_{CE}(sat) is realized by enhanced carrier accumulation because narrow mesa disturbs hole extraction. Several types of new generation IGBTs have the same feature of low V_{CE}(sat) [5, 6].

The low gate voltage driving for example 5V instead of 15V is realized by increased capacitance per unit area between the gate and emitter (C_{GE}) by forming of a thin gate oxide film. Only an IGBT based on a scaling principle can be driven by a low gate voltage, which saves power for gate driving in proportion to the square of the voltage swing. This means that low voltage gate driving can use the driver IC instead of the driver board. And the low voltage of the digital signal level and the driver size has the advantage of integration and/or intelligent driving [7].

However, low gate voltage driving with a low threshold voltage (V_{th}) has the disadvantage of false driving by gate noise. From this concern, the IGBT is not yet in the market. For example, the threshold voltage of the present IGBTs (scaling factor=1) and the new generation IGBT (scaling factor=3) is 6 V and 2 V, respectively. The V_{GE} margin from 0 V is decreased to one-third corresponding to the scaling factor. In this case, bias voltage (V_{bias}) is generally used to prevent false driving. Although V_{bias} is known by suppressing V_{GE} noise, the voltage enlarges the gate driver size because the voltage swing increases the power for gate driving and the negative voltage complicates circuit configuration. This means that the V_{bias} may lose one of the advantages of scaling IGBT.

In this paper, we propose the criteria of minimum required bias voltage from parasitic capacitance [8] and demonstrate the criteria in an experiment with the present IGBT. After that, we verify the bias voltage theoretically regarding application for the new generation IGBT based on the scaling principle.



(a) V_{GE}=0V (b) Sufficient bias voltage

Fig. 1. Schematic view of parasitic capacitance in the emitter side of IGBT. When the bias voltage is sufficient to form a p inversion layer, C_{GC} is decreased and C_{GE} is increased.

2. Criteria of the minimum bias voltage required for the gate shielding effect

The capacitance between the gate and collector (C_{GC}) and C_{GE} is determined by the following equations:

$$C_{GC}(V_{GC}) = \frac{dQ}{dV_{GC}} \quad (1)$$

$$C_{GE}(V_{GE}) = \frac{dQ}{dV_{GE}} \quad (2)$$

The C_{GC} and C_{GE} are changed by V_{CE} and V_{GE}, respectively (see Fig. 1). V_{GC}, V_{GE} and V_{CE} are related as follows:

$$V_{GC} + V_{GE} = V_{CE} \quad (3)$$

From these equations, V_{GE} under an open gate circuit is eventually expressed by the following analytical equation model as far as the C_{GC} change with the V_{CE}:

$$V_{GE}(R_G = \infty) = \frac{q\varepsilon N_B {A_{GC}}^2 \left(\sqrt{1 + \frac{2{C_{GE}}^2 V_{CE}}{q\varepsilon N_B {A_{GC}}^2}} - 1 \right)}{{C_{GE}}^2} \quad (4)$$

where, q, ε, N_B and A_{GC} are electron charge, dielectric constant, concentration of the n base layer and area of C_{GE}, respectively. It is predicted from Eq. 4 that when V_{bias} is 0 V, V_{GE} is roughly increased in proportion to the route of V_{CE}.

Next, we predict the V_{bias} effect from C_{GC} and C_{GE} in the experiment because the capacitance has complex V_{CE} dependence. When the bias voltage is 0 V, C_{GC} is decreased corresponding to the V_{CE} increase because the depression layer expands in the n- base region (see Fig. 2). When a sufficient bias voltage is applied for a gate shielding effect, C_{GC} is dramatically decreased because the inversion p layer covers the gate oxide film and connects the p bases. When the bias voltage is 0 V, C_{GE} is constant at a lower value because the initial diffusion layer only contributes to C_{GE} (see Fig. 3). When a sufficient bias voltage is applied, C_{GE} is constant at a higher value because the initial diffusion layer and inversion p layer contribute to C_{GE}.

The predicted V_{GE} under V_{bias} is calculated by a parasitic capacitance. These results are categorized as follows (see Fig. 4):

(a) $V_{bias} \geq -1V$: V_{GE} is affected without V_{CE}
(b) $-2V \geq V_{bias} \geq -5V$: V_{GE} is affected depending on V_{CE}
(c) $V_{bias} \leq -6V$: V_{GE} is not affected by V_{CE}

Increase of collector current (I_C) by false driving occurs when the V_{GE} exceeds the threshold voltage. Therefore, the criteria of the bias voltage are calculated by V_{GE} with the threshold voltage. As a result, the required bias voltage is predicted to be -1.2 V or less even if V_{CE} is assumed to be up to a DC

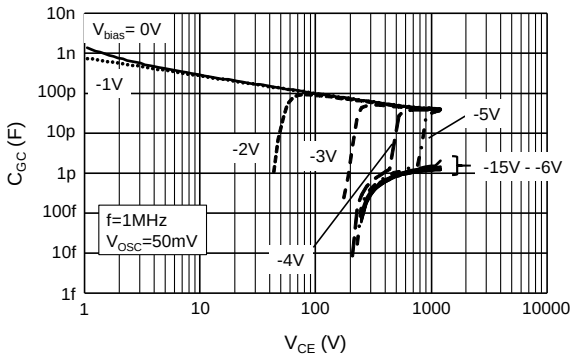


Fig. 2. Capacitance between gate and collector (C_{GC}) in our experiment. C_{GC} is decreased dramatically by the bias voltage and converged to a constant value under -6 V.

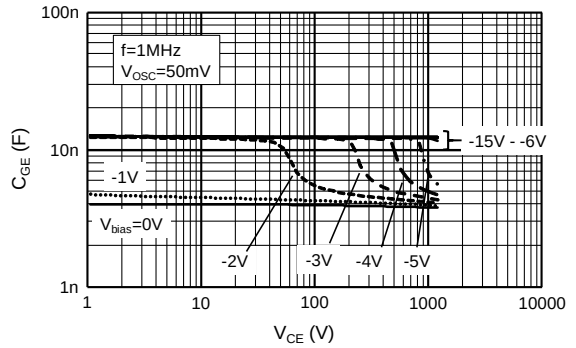


Fig. 3. Capacitance between gate and emitter (C_{GE}) in our experiment. C_{GE} is increased by the bias voltage and converged to a constant value under -6 V.

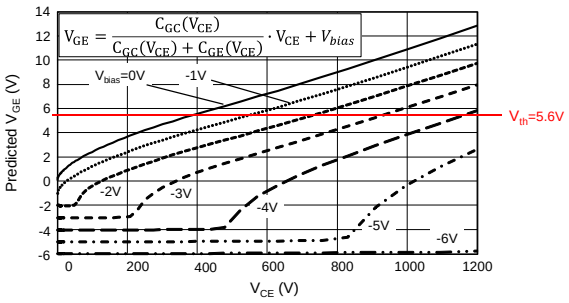


Fig. 4. Predicted V_{GE} calculated from C_{GC} and C_{GE}. The bias voltage effect is decreased by the increase of V_{CE}.

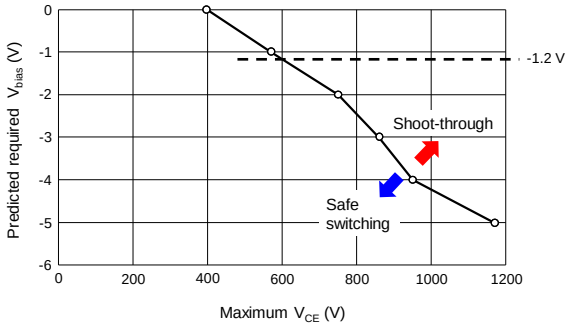


Fig. 5. Criteria of safe switching without shoot-through. -1.2 V or less is required even if V_{CE} is assumed to be the minimum DC voltage of 600 V.

voltage (V_{DC}) of 600 V (see Fig. 5). This time, we use planar gate IGBT in the experiment. However, the mechanism and V_{GE} prediction method of trench gate IGBTs are the same as that of planar gate IGBTs.

3. Demonstration of validity of bias voltage criteria in experiment

The criteria are demonstrated by an inductor load double pulse test with a 2 in 1 IGBT module (see Fig. 6). The rated voltage and current are 1200 V and 50 A, respectively. The low side gate resistance is up to 1000 Ω for a virtual open circuit between the gate and emitter. The minimum low side gate resistance is 0 Ω except the inner gate resistance of the IGBT chip. High side gate resistance is fixed to 0 Ω because the highest dV_{CE}/dt of 24kV/μs leads to the worst case of the highest V_{GE}. Stray inductance of the gate and main circuit is fixed in this experiment. It is assumed that the higher value of both inductances increases the V_{GE} because of the higher V_{CE} surge and impedance of the gate circuit.

When the V_{bias} is -4 V, normal waveforms of V_{GE}, V_{CE}, I_C and I_C through low side IGBT (I_{C_L}) are measured (see Fig. 7). When the V_{bias} is -3 V, V_{GE} has a smaller noise voltage (see Fig. 8). When the V_{bias} is -2 V, V_{GE} has a larger noise voltage (see Fig. 9). When the V_{bias} is -1 V, V_{CE} has the largest noise voltage and I_{C_L} is increased over 100 A (see Fig. 10). The current limit protects low side IGBT.

The charge by integration of I_{C_L} during the first gate pulse clearly indicates that the bias voltage to prevent false driving is from -2 V to -1 V (see Fig. 11). The calculated bias voltage criteria were confirmed. The charge from the current is used for the judgement of false driving because the voltage waveform is affected by stray inductance of the bonding wires and

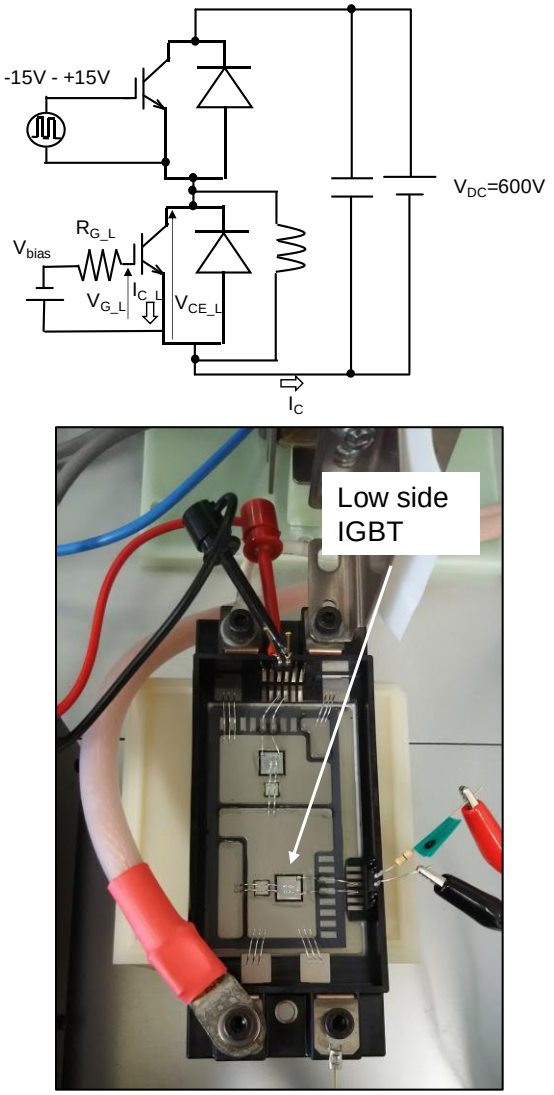


Fig. 6. L load double pulse switching circuit and 2 in 1 IGBT module for demonstration.

terminals.

4. Discussion of bias voltage for new generation IGBT based on the scaling principle

The bias voltage of scaling IGBT can be predicted with the assumptions described below. The doping concentration and thickness of the n- base region of scaling IGBT is the same as the present IGBT to maintain the same blocking voltage. The thickness of the gate oxide film is scaled down based on the scaling factor to obtain the same gate charge. As a result, the bias voltage is also scaled down to one-third if the scale factor is 3. Specifically, a bias voltage of -2 V is predicted for complete gate noise reduction.

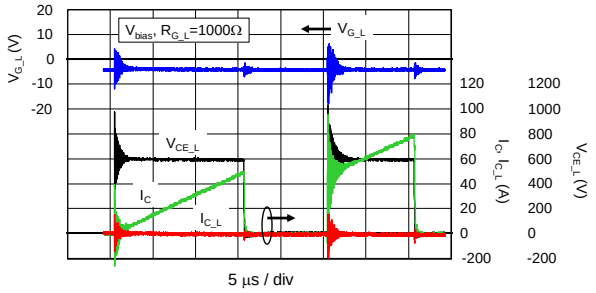


Fig. 7. Waveform example for a bias voltage of -4 V. The waveforms are normal.

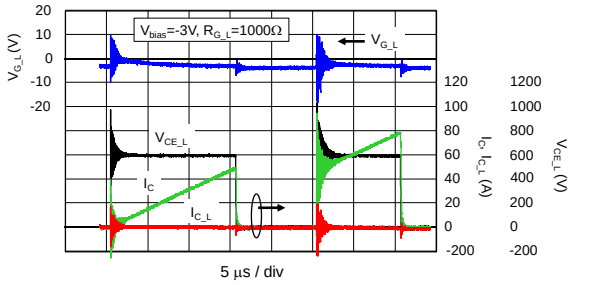


Fig. 8. Waveform example for a bias voltage of -3 V. V_{GE} has a smaller noise voltage.

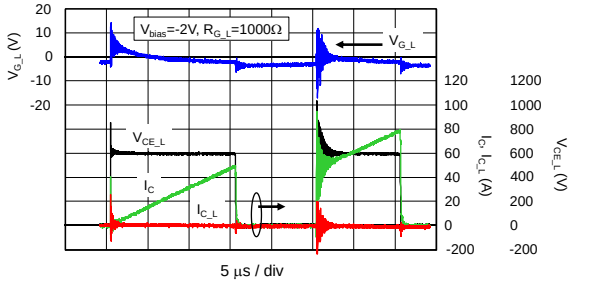


Fig. 9. Waveform example for a bias voltage of -2 V. V_{GE} has a larger noise voltage.

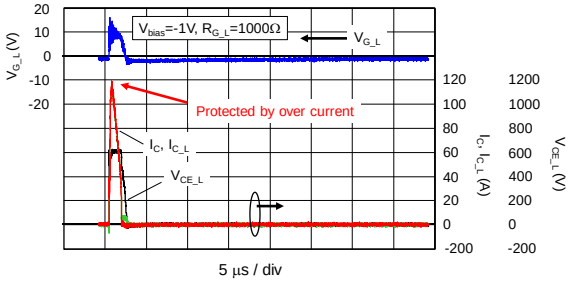


Fig. 10. Waveform example for a bias voltage of -1 V. V_{GE} has the largest noise voltage and I_{C_L} is increased over 100 A.

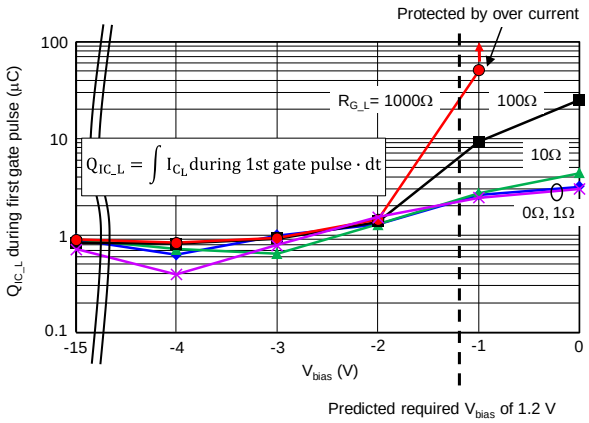


Fig. 11. Charge by integration of I_{C_L} during first pulse (Shoot-through current). The charge clearly indicates that the bias voltage border to prevent false driving is from -2 V to -1 V. The predicted bias voltage of 1.2 V and the criteria are confirmed in the experiment.

5. Conclusions

In this paper, we propose the criteria of bias voltage from parasitic capacitance and demonstrate the criteria in an experiment with the present IGBT. We verified the bias voltage theoretically regarding the application for new generation IGBT based on the scaling principle.

For safe switching, a bias voltage of -1.2 V or less is predicted to be required and -6 V or less is predicted to be required to cancel the gate noise voltage completely.

The predicted bias voltage is also scaled down to one-third if the scale factor is 3. Specifically, a minimum required bias voltage of about -2 V is predicted for complete gate noise cancellation by the gate shielding effect for a new generation IGBT based on the scaling principle.

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