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Paper

Mechanism Clarification of Switching Loss and Surge Voltage / Current Reduction with Active Gate Drive for System Reliability Improvement

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Abstract: The active gate drive (AGD) technique is payed attention as a switching technique which can reduced both of switching loss and surge voltage. So far, only switching loss and surge voltage of main switch have been discussed, and the reverse recovery characteristic of rectification diode has not been discussed. In addition, the mechanism of loss and surge reduction has not been clarified. In this paper, the influence of AGD on reverse recovery characteristics, and the mechanism of loss and surge reduction are discussed for system reliability improvement. As a result, the mechanism of loss and surge reduction is clarified.

Keywords: Active gate drive, Surge voltage, Switching loss, Reverse recovery loss,

1. Introduction

A switch mode power supply (SMPS) has been miniaturized with miniaturizing the electric equipment. The easiest technique for miniaturization of the SMPS is high frequency switching. Higher switching frequency leads to achieve the miniaturization of the passive components such as inductor, transformer, capacitor which occupying a large volume in SMPS. On the other hand, the switching loss and surge voltage of the MOSFETs as switching device are increases, and the reverse recovery loss of the rectification diodes are also increases.

The system reliability of SMPS has been decided by the life time of the electricity capacitor, so far. However, the ceramic capacitors are used instead of the electricity capacitor for miniaturization of the SMPS. In this electricity capacitor less SMPS, the system reliability is decided by the life time of the switching devices such as MOSFETs and rectification diodes. The switching loss and surge voltage of MOSFETs are increased, and the reverse recovery loss of rectification diodes are also increased by higher switching frequency, but heat sink is not able to be so larger for miniaturization of the SMPS. Therefore, the hot spot of switching devices due to the large loss and surge causes the peeling of solder layer and lifted off of bonding wire, and these phenomena are remarkably decreased system reliability[1] [2]. So far, these issues have been solved by snubber circuit and soft-switching technique with auxiliary circuit, though these techniques inhibits the miniaturization of the SMPS and the system reliability is decreased due to the large amount of circuit components.

The active gate drive (AGD) technique is payed attention as the switching technique which can reduced both problems of switching loss and surge voltage [3]~[6]. In references 3 to 6, the only effect of the active gate drive has been discussed and its mechanism of surge voltage and switching loss has never been discussed. In addition, only main switch has been discussed, and the reverse recovery characteristic of rectification diode has not been discussed.

In this paper, the influence of AGD on reverse recovery characteristics is confirmed, and the mechanism of loss and surge reduction are clarified.

Table 1: Circuit parameters and specifications.

Symbol	Descriptions	Value
VDD	Input Voltage	20 V
L	Smoothing Inductor	150 uH
MOSFET	Main switch	STP20NM60
Diode	Rectification diode	STTH5L06

2. Effect of Active Gate Drive

The switching characteristics are measured by using switching test circuit with double pulse as shown in Fig. 1. As shown in Fig. 1, the resistance is connected in series with the transistor, and the resistance is switched by giving the pulse single to the transistor. The switching loss and surge voltage of MOSFET during turn-off interval, and the reverse recovery current during turn-on interval are evaluated. At first, both of MOSFET and rectification diode characteristics are measured with constant gate resistance, respectively.

Next, the influence of AGD on both of MOSFET and rectification diode characteristics are examined, respectively. The circuit parameters and specifications are shown in Table 1.

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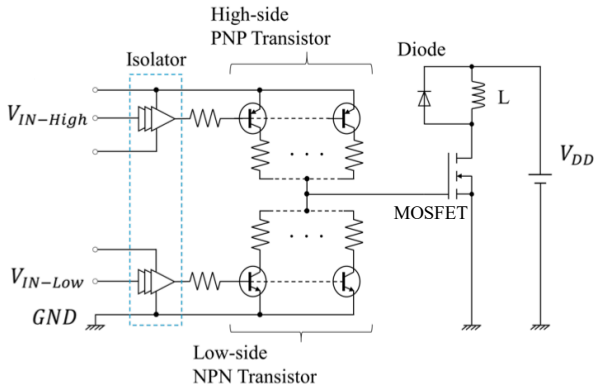


Figure 1: Switching test circuit with AGD.

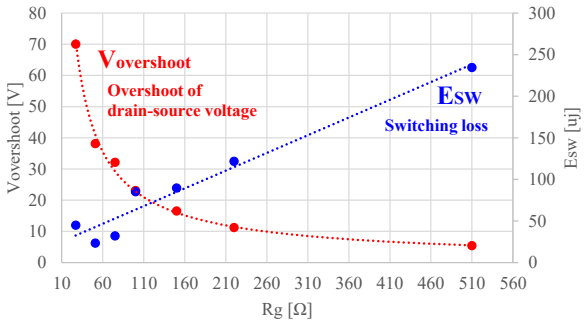


Figure 2: Switching loss and surge voltage of MOSFET.

2.1 Turn-off interval The switching loss and surge voltage characteristics against gate resistance are shown in Fig. 2. Although the surge voltage is decreased with increase of gate resistance, the switching loss is increased, as shown in Fig. 2.

There is the relation of the trade-off of the switching loss and surge voltage, and the optimal gate resistance is around 120 ohm. In this case, the switching loss is around 75 uJ and surge voltage is around 20 V. Next, the influences of AGD on switching loss and surge voltage reduction are confirmed.

The gate resistances connected in high-side PNP transistor showing in Fig. 1 are switched by 4 states. Based on device physics, there are 3 states between turn-off interval. However, drain-source voltage is gradually increasing in first-half of miller interval, and the drain-source voltage is rapidly increasing in second-half of miller interval, as shown in Fig. 3. Hence, turn-off interval is separated into 4 states. Both of switching loss and surge voltage are reduced as shown in Fig. 4. In this case, the switching loss is 80 uJ and surge voltage is around 5 V. These results are the same as previous reports [3]. Moreover, the sufficient effect has been confirmed although only 4 states AGD.

2.2 Turn-on interval The reverse recovery current of rectification diode and switching loss of MOSFET characteristics against gate resistance are shown in Fig. 5. The reverse recovery current of rectification diode is reduced easily with large gate resistance. However, the switching loss of MOSFET is increasing in proportion to the gate resistance as shown in Fig. 5. The optimal gate resistance is around 190 ohm. In this case, the reverse recovery current is around 1.3A and the switching loss is 30 uJ.

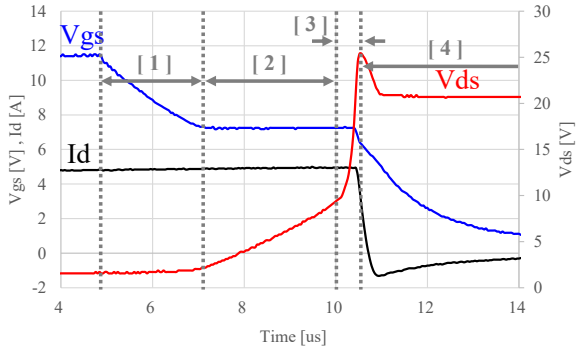


Figure 3: Switching waveform of turn-off interval.

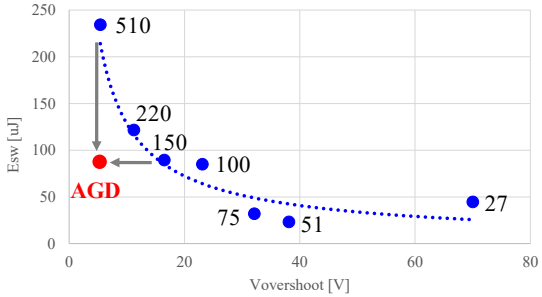


Figure 4: Effect of AGD in turn-off interval.

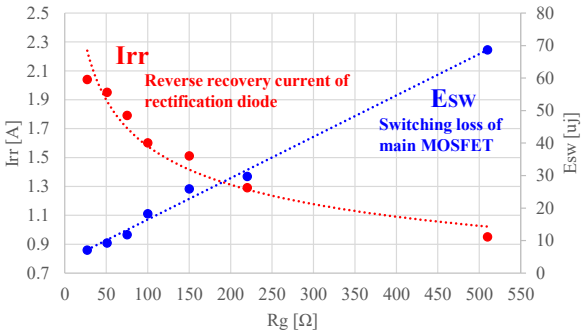


Figure 5: Reverse recovery current of rectification diode and switching loss of MOSFET.

Next, the influence of AGD on reverse recovery current of rectification diode and the switching loss of MOSFET are confirmed. The gate resistances connected in low-side NPN transistor showing in Fig. 1 are also switched by 4 states, and turn-on interval is also separated into 4 states as shown in Fig. 6. Both of reverse recovery current and switching loss are reduced as shown in Fig. 7. In this case, the reverse recovery current is around 1.4 A and the switching loss is 10 uJ. From these results, it has been confirmed that the AGD is effective on improvement of reverse recovery characteristic, and the sufficient effect has been also confirmed although only 4 states AGD.

These results are the same as previous reports [3]. Moreover, the sufficient effect has been confirmed although only

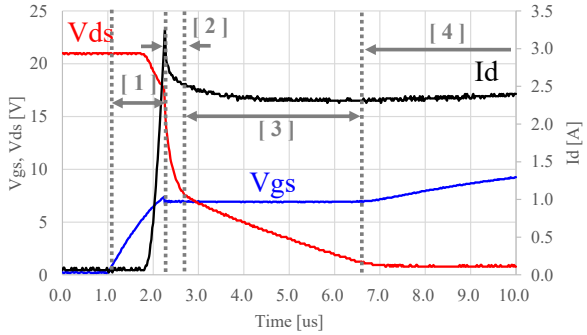


Figure 6: Switching waveform of turn-on interval.

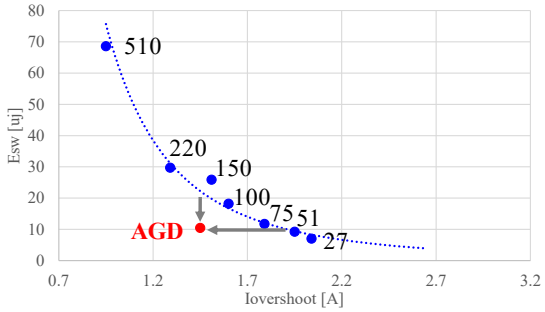


Figure 7: Effect of AGD in turn-on interval.

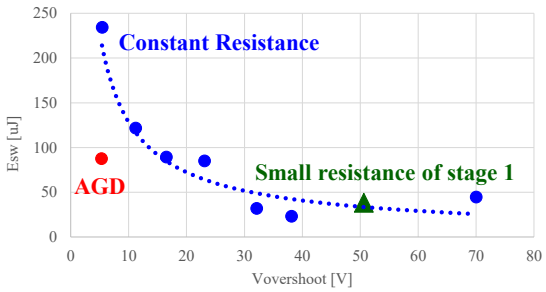


Figure 8: Effect of gate resistance of state 1 (turn-off).

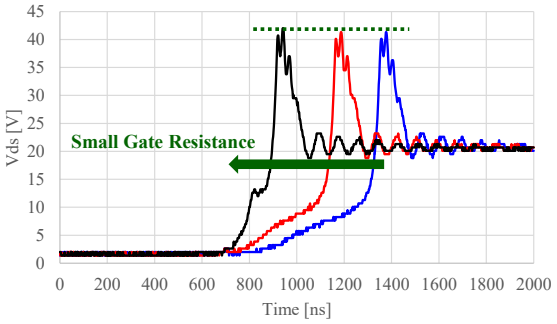
4 states AGD.

3. Loss and Surge Reduction Mechanism

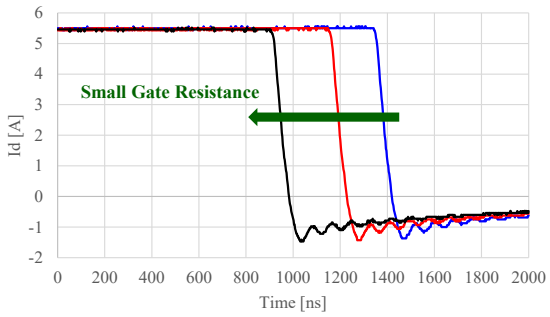
In this section, the influences of gate resistance (AGD) on switching characteristics on each state are investigate for the clarification of loss and surge reduction mechanism.

3.1 Turn-off interval Based on the setting showing in Fig. 4, which is sufficiently obtained the AGD effect, the gate resistance of each state is changed to examine the influence on the switching characteristics.

(a) State 1 (Vdc to Miller voltage)
This state is the most important state for the basis of AGD. When the resistance of this section is set to small, the effect of AGD is disappeared, and the switching characteristics is the same as constant resistance case as shown in Fig. 8. The gate resistance of this state should be set to moderately lager, and the gate voltage should be gently reduced to Miller voltage during interval of state 1.



(a) Drain-source voltage



(b) Drain current

Figure 9: Effect of gate resistance of state 2. (turn-off).

(b) State 2 (First-half of Miller interval)
The surge voltage across drain and source terminal does not depend on gate resistance as shown in Fig. 9(a). However, the rise time of drain-source voltage depends on gate resistance, and dv/dt of drain-source voltage is larger with small resistance. On the other hand, the di/dt of drain current is not changed as shown in Fig. 9(b). In addition, the Miller interval becomes shorter due to the large dv/dt of drain-source voltage. Because of this, the drain-source voltage is reduced faster with large dv/dt. In this state, the switching loss is reduced. The gate resistance of this state is influence on dv/dt, but is never influence on di/dt. Hence, this state can reduce only switching loss.

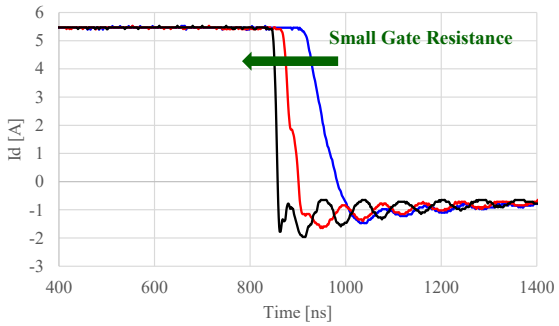
(c) State 3 (Second-half of Miller interval)
The di/dt of drain current depends on gate resistance as shown in Fig. 10(a)), and di/dt is larger with smaller gate resistance.

As a result, the surge voltage across drain and source terminal becomes smaller with larger gate resistance.

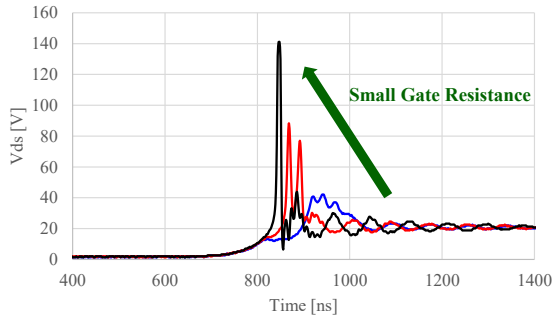
The gate resistance of this state is influence on di/dt, and the surge voltage across drain and source terminal can be reduced.

(d) State 4 (Miller voltage to 0V)
In this state, the switching action is almost finished, so it is not influence on switching loss and surge voltage occurrence.

However, gate voltage does not reach to zero, so the gate resistance of this state should be set smaller than



(a) Drain current



(b) Drain-source voltage

Figure 10: Effect of gate resistance of state 3. (turn-off).

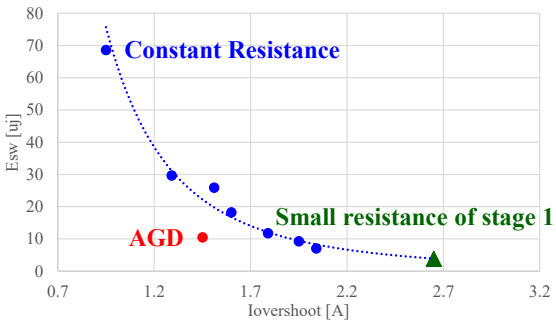


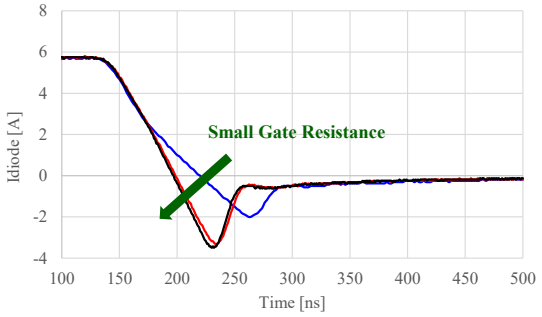
Figure 11: Effect of gate resistance of state 1.(turn-on).

state 3. This leads to reduction of the drive power of MOSFET.

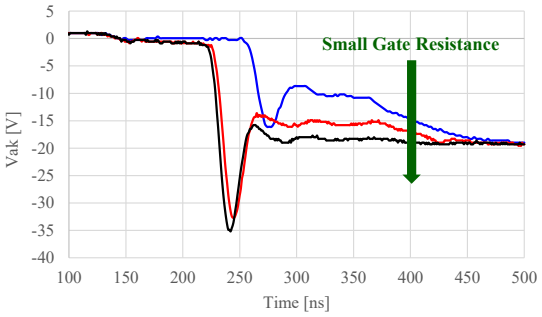
3.2 Turn-on interval Based on the setting showing in Fig. 6, which is sufficiently obtained the AGD effect, the gate resistance of each state is changed to examine the influence on the switching characteristics.

(a) State 1 (0 V to Miller voltage)
This state is also the most important state for the basis of AGD. When the resistance of this section is set to small, the effect of AGD is disappeared. Moreover, the switching characteristics are the same as constant resistance case as shown in Fig. 11. These characteristics are the same as turn-on interval case. The gate resistance of this state should be set to moderately lager, and the gate voltage should be gently increased to miller voltage during interval of state 1.

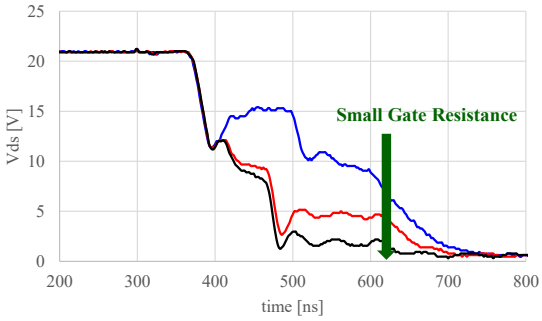
(b) State 2 (First-half of Miller interval)



(a) Reverse recovery current



(b) Anode-Cathode voltage

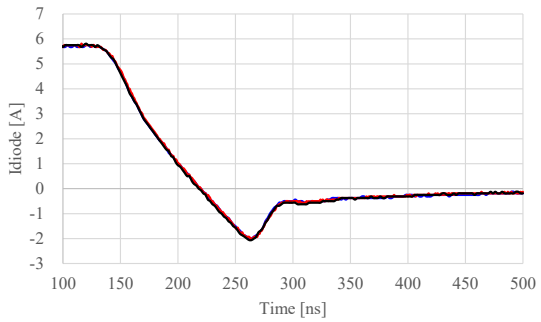


(c) Drain-source voltage

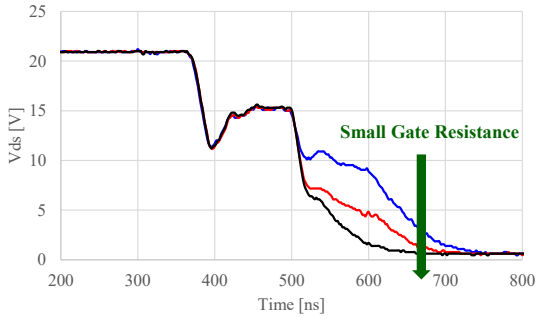
Figure 12: Effect of gate resistance of state 2. (turn-on).

The reverse recovery current depends on gate resistance as shown in Fig. 12(a), and di/dt is smaller with lager gate resistance. As a result, the voltage variation of anode-cathode voltage is reduced with larger gate resistance as shown in Fig. 12(b). Therefore, the reverse recovery loss can be reduced in this state. However, the drain-source voltage variation becomes larger, and the switching loss becomes increased as shown in Fig. 12(c). The gate resistance of this state is influence on di/dt of reverse recovery current, and the reverse recovery loss can be reduced.

(c) State 3 (Second-half of Miller interval)
The reverse recovery current does not depend on gate resistance as shown in Fig. 13(a), and di/dt is never changed by gate resistance. On the other hand, the voltage variation of drain-source voltage depends on gate resistance as shown in Fig. 13(b). The voltage variation of drain-source voltage is reduced with larger gate resistance. The gate resistance of this state is in-



(a) Reverse recovery current



(b) Drain-source voltage

Figure 13: Effect of gate resistance of state 3.(turn-on).

fluence on the voltage variation of drain-source voltage, but is never influence on di/dt of reverse recovery current. Hence, this state can reduce only switching loss.

(d) State 4 (Miller voltage to V_{dc})
In this state, the switching action is almost finished, so it is not influence on switching loss and surge voltage occurrence. Therefore, the gate resistance of this state is set the same as state 3.

4. Conclusions

In order to improve the system reliability of SMPS, the influence of AGD on loss and surge reduction has been investigated in this paper. As a result, the effects of AGD have been confirmed in both of MOSFET and rectification diode. Moreover, the mechanism of loss and surge reduction has been clarified. The optimization of the gate resistance of each state will be discussed in the next report.

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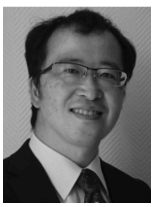

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