On Evaluation for Aging-Tolerant Ring Oscillators with Accelerated Life Test And Its Application to A Digital Sensor

Masayuki Gondo[1], Yousuke Miyake[2], Takaaki Kato[2], Seiji Kajihara[2]
Kyushu Institute of Technology, 680-4 Kawazu, Iizuka, Fukuoka, 820-8502 Japan
[1]q232042m@mail.kyutech.jp, [2]{miyake, katou, kajihara}@aries30.cse.kyutech.ac.jp

***Abstract*—An aging-tolerant ring oscillator (RO) has been proposed for a digital temperature and voltage sensor. This paper discusses on the effectiveness of aging-tolerance of the ROs through accelerated life test for a test chip with 65nm CMOS technology. The progress of delay degradation of the ROs is examined, and influence of delay degradation on measurement accuracy of the sensor is investigated. Experimental results show that the aging-tolerant ROs can mitigate delay degradation, and that the measurement errors of the sensor can be reduced. Compared with a sensor consisting of an aging-intolerant RO, temperature and voltage errors are reduced 2.5°C and 32mV, respectively.**

Keywords—Temperature and voltage sensor, Ring Oscillator, Aging-tolerance, Accelerated life test

I. Introduction

VLSIs have been widely used in various devices, and high reliability is often required especially for safety critical applications [1, 2]. It is effective to ensure the reliability or performance of the VLSIs by embedding sensors on a chip to monitor a chip temperature or voltage, because system errors and performance loss are often caused by abnormal heating or voltage drop [3]. Many kinds of on-chip sensor to monitor a chip temperature or voltage have been proposed [4-10]. Temperature sensors using an analog circuit like a thermal diode are well-known. Although the analog sensors provide high measurement accuracy, an AD converter is needed and the sensor size becomes large. So the number of sensors mounted on a chip is generally at most one. Sensors composed of digital circuits have been proposed [7-10]. In general, the size of digital sensors is small, more than one sensors can be mounted on the chip. The digital sensor proposed in [9] consists of ring oscillators (ROs). The sensor can measure temperature and voltage simultaneously from RO frequency, but it is necessary to newly design a special cell not included in a standard cell library. The digital sensor proposed in [10] that is also RO-based, is composed of three ROs with different circuit structure each other, and can be configured with only standard logic cells. It is reported that the sensor manufactured in 65nm CMOS technology achieved measurement accuracy of ±2.74°C under the temperature range of 0 to 120°C and the voltage range of 1.06 to 1.34V [11].

If a logic circuit deteriorates with time, circuit delay increases. NBTI (Negative Bias Temperature Instability) is a representative aging phenomenon which causes fluctuations in the threshold voltage of PMOS transistors. In [12], delay degradation of ROs due to BTI is discussed. In [13]-[16] several techniques regarding an NBTI-tolerance have been proposed. In terms of circuit structure, a technique in [13] adjusts gate size to suppress NBTI, and a technique in [14] inserts transistors to control gates condition during sleep state. In terms of power, a technique in [15] uses power gating to prevent NBTI during sleep state and a technique in [16] schedules voltage to compensate delay by NBTI. Because these techniques [13]-[16] need to design a special cell or to redesign not only the RO but also an entire chip, design cost becomes high. The BTI-insensitive ROs proposed in [12] consider RO topology to suppress potential difference for NBTI-induced degradation. The NBTI-tolerant RO in [10] can prevent the deterioration of PMOS transistors associated with oscillation by setting the transistors to off-state during non-oscillation mode. The circuit structure is effective to avoid aging by not only NBTI but also HCI and electro migration. If the aging-tolerant ROs are used for the digital sensor, it would expect to maintain measurement accuracy for a long time [17]. However, the actual progress of delay degradation of the aging-tolerant ROs and the influence on accuracy of the sensor have not been quantitatively evaluated yet.

In this paper, the ability to suppress delay degradation of the aging-tolerant ROs and the digital temperature and voltage sensor [10] are investigated by accelerated life test for a test chip manufactured with 65nm CMOS technology. Three ROs with different architecture are implemented on the chip where two ROs are aging-tolerant and one is aging-intolerant. Fluctuations of the RO frequencies are measured and quantitatively evaluated by degradation of the ROs. From the accelerated life test, it is found that the frequency degradation of the two aging-tolerant ROs is 0.14% and 0.13% while that of the aging-intolerant RO is 0.97%. When the ROs make up a temperature and voltage sensor, a range of estimation error is reduced from 7.8°C to 5.3°C in temperature and 43mV to 11mV in voltage by enabling aging-tolerance of the ROs.

This paper is organized as follows. Section 2 describes the RO-based sensor and aging-tolerant ROs proposed in [10]. Section 3 describes a structure of the test chip. Section 4 shows experimental results for the ROs with accelerated life test. Section 5 shows evaluation results as the RO-based sensor. Section 6 concludes the paper.

II. Temperature and Voltage Sensor

A. RO-based Temperature and Voltage Sensor [10]

An on-chip digital temperature and voltage sensor (TVS) that employs three pairs of a ring oscillator and a counter is proposed for field testing [10]. The three ROs have different frequency characteristics each other for temperature and voltage, and the TVS can measure both temperature and voltage simultaneously. The TVS is small size and hence it can be placed at more than one places on the chip. Because the TVS is designed without analog circuits such as ADC, the process to calculate the temperature and voltage from RO frequencies is fully digital. As a result, a short measurement time under 100 μsec can be achieved.

The TVS consist of three ROs which have different frequency characteristics for both temperature and voltage each other, and the temperature and voltage are calculated from three RO frequencies. The estimation equations (1) and (2) are derived by multiple regression analysis on the

relationships between frequency and temperature, and between frequency and voltage.

$$\Delta T = a_{\Delta T} * \Delta F_1 + b_{\Delta T} * \Delta F_2 + c_{\Delta T} * \Delta F_3 + d_{\Delta T} \quad (1)$$

$$\Delta V = a_{\Delta V} * \Delta F_1 + b_{\Delta V} * \Delta F_2 + c_{\Delta V} * \Delta F_3 + d_{\Delta V} \quad (2)$$

where $\Delta F_i (i = 1,2,3), \Delta T,$ and ΔV indicate the amount of change of RO frequency of three ROs, a difference of temperature and voltage from the first measurement, respectively. $a_{\Delta T}, a_{\Delta V}, b_{\Delta T}, b_{\Delta V}, c_{\Delta T}, c_{\Delta V}, d_{\Delta T}, \ d_{\Delta V}$ indicate coefficients of estimation equations that are created by multiple regression analysis on the simulation data or measurement data of a representative chip. Note that the first measurement in field testing is supposed to be done under the well-controlled condition such as manufacturing test, i.e., the temperature and voltage are known values. In the second measurement and later, the calculation at the TVS is based on the amount of fluctuation of the temperature and voltage from the difference between the frequency at pre-shipment test and the frequency during system operation.

B. *Calibration for Process Variation*

The precise threshold voltage of each transistors is unknown in simulation because of process variation. The variation affects gate delay of actual circuits. If the RO frequency has large fluctuation in an RO-based sensor, accuracy of the sensor goes down. Process variation is classified into two categories, that are global variation and local variation [18]. By global variation, characteristics of transistors may change smoothly across the entire wafer. Then, the RO frequencies differ depending on chip location of the wafer. On the other hand, by local variation, characteristics of transistors vary independently. Therefore, frequency fluctuation caused by local variation will be reduced to $1/\sqrt{N}$ times according to the law of large numbers, where N is the number of RO stages. As a result, the TVS can reduce the influence of local variation by increasing the number of RO stages at the expense of circuit size. The influence of global variation can be reduced by applying the calibration process at the initial measurement which is assumed to be done under well-controlled condition [10]. The calibration process corrects the initial equations (1) and (2) by multiplying the ratio that is obtained by comparing frequency of the initial measurement F and circuit simulation or measurement of a representative chip F^{typ}. The corrected estimation equations (3) and (4) are given below.

$$\Delta T = a_{\Delta T} \frac{F_1^{typ}}{F_1} \Delta F_1 + b_{\Delta T} \frac{F_2^{typ}}{F_2} \Delta F_2 + c_{\Delta T} \frac{F_3^{typ}}{F_3} \Delta F_3 + d_{\Delta T} \quad (3)$$

$$\Delta V = a_{\Delta V} \frac{F_1^{typ}}{F_1} \Delta F_1 + b_{\Delta V} \frac{F_2^{typ}}{F_2} \Delta F_2 + c_{\Delta V} \frac{F_3^{typ}}{F_3} \Delta F_3 + d_{\Delta V} \quad (4)$$

C. *Aging-tolerant RO*

It is difficult to avoid aging of ROs while they are operating, i.e. oscillating. When ROs are used for a TVS, however, by stopping oscillation of the ROs except during measuring temperature and voltage, deterioration of the ROs can be suppressed and even recovered from NBTI aging.

Generally, while the input of PMOS transistor is set to 1(high), NBTI does not progress. In [10], aging-tolerant RO structure is proposed such that NBTI deterioration is suppressed during the non-oscillation mode, that is, control signals set PMOS input to 1 during the non-oscillation mode. Fig. 1 shows an example of an aging-tolerant RO composed of NAND gates. The RO has two control signals, Enable signal (*En*) and Start signal (*Start*). When *En* and *Start* are set to 0, outputs(*output_YB*) set to 1 and the RO does not oscillate. Since inputs (*input_A*) of the PMOS transistors associated with oscillation are set to 1, the RO is prevented from NBTI deterioration. When *En* and *Start* set to 1, the RO oscillate. *En* is set to 1 to reset each logic gates, and then *Start* is set to 1 to start oscillation.

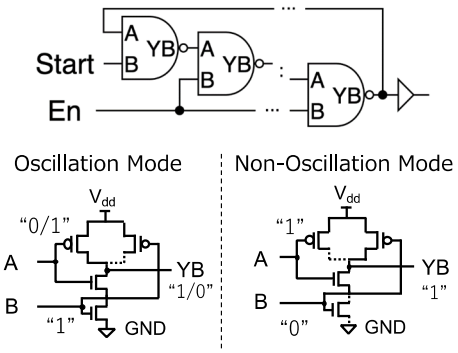


Fig. 1. NBTI-tolerant structure

III. Circuit Structure of Test Chip

A. *Test Chip Architecture*

A test chip with 65nm CMOS technology is designed to evaluate performance of the aging-tolerant ROs and the TVS. Chip size is 2.0mm×1.5mm. The core voltage is 1.20V and the operating clock frequency is 50 MHz. The TVS consists of three ROs, where RO1 is 51 stages of 3-inputs NAND gate, RO2 is 51 stages of 3-inputs ORNAND gate, and RO3 is 51 stages of 2-inputs XOR gate. RO1 and RO2 have aging-tolerant structure but RO3 is aging-intolerant. Details are given in the next section. Although there are various types of ROs available, these three ROs were selected based on an RO selection method [11] that can estimate temperature and voltage with high accuracy. Each RO is connected a counter that counts the number of oscillations during a preset oscillation time 81.92 μsec (20ns×4096clock). RO frequency is derived from the measured RO count value and the oscillation time, and temperature and voltage values are estimated by applying the estimation equations as shown in the equations (3) and (4). Fig. 2 shows the test chip layout. Four TVSs are placed around a CUT to observe the influences of the test chip layout or process variation.

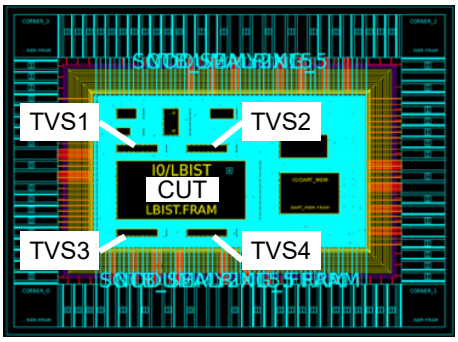


Fig. 2. Test chip layout with 65nm CMOS technology (2.0mm×1.5mm)

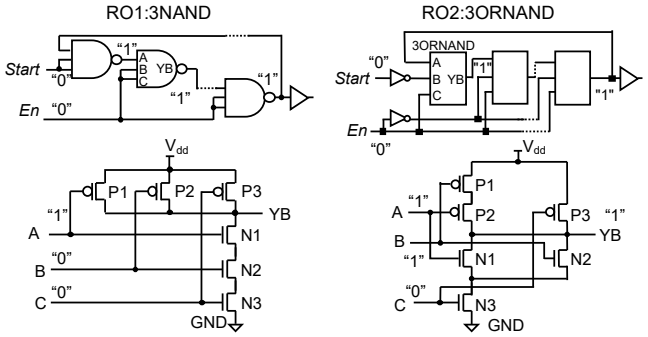
B. *Aging-tolerant Structure*

NBTI (Negative BTI) and PBTI (Positive BTI) are aging phenomena that cause increase of a circuit delay. Since NBTI

is a critical issue of VLSIs, this paper discusses an aging-tolerant RO structure focusing on NBTI. Although PBTI is an important issue in the state-of-the-art CMOS technology, PBTI is not a serious issue in the 65nm CMOS technology yet. Thus, PBTI is out of consideration in this paper.

a) Aging-tolerant RO1 and RO2

Fig. 3 shows logic level and transistor level structure of RO1 and RO2. Logic gates of the ROs connects *output_YB* of each logic element to *input_A* of the gate in the next stage. In order to control its oscillation, Start signal (*Start*) or Enable signal (*En*) is connected to each logic element. *Start* is only connected to the first stage of 51 stages. *En* is connected to the other stages. The ROs are oscillating during (*Start*, *En*) = (1,1), though they are not oscillating during (*Start*, *En*) = (0,0). While stopping oscillation, PMOS transistor P1 of RO1 and P1, P2 of RO2 are off-state and recovered from NBTI aging because these PMOS transistors are set to 1.



(a) 3NAND (b) 3ORNAND

Fig. 3. RO1 and RO2 with aging-tolerant structure

b) Aging-intolerant RO

Fig. 4 shows circuit structure of RO3. RO3 is oscillating during (*Start*, *En*) = (1,1) and do not oscillate during (*Start*, *En*) = (0,0) as well as RO1 and RO2. However, PMOS transistor P3 on oscillation path that is always set to 0 degrades due to NBTI. As a result, threshold voltage of P3 goes up and frequency drops, PMOS P4 through oscillating path is expected to recover deterioration.

Note that, the TVS should consist of the three types of aging-tolerant RO such as [10] and [17], but the implemented RO3 is not aging-tolerant structure. The design error was caused by misreading the transistor structure of the XOR gate at the time of chip design, which resulted in the aging-intolerant RO structure. However, by using the RO3, we can evaluate the impact on a TVS of the difference between aging-tolerant ROs and aging-intolerant ROs.

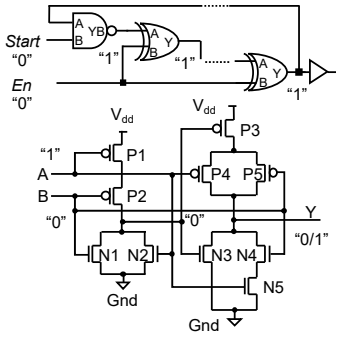


Fig. 4. RO3 without aging-tolerant structure

IV. Evaluation with Accelerated Life Test

A. Experiment contents

In order to perform accelerated life test, this experiment uses a thermostatic bath ESPEC SU-241 to heat the chip and a tester ADVANTEST CX1000D to control chip operation and power supply. In the experiment, RO frequency fluctuations in the chip that operates continuously for half a day under high stress conditions are measured. Then, the influence of degradation for estimation accuracy is evaluated when the aging-tolerant ROs used to the TVS.

Fig. 5 and Fig. 6 show a relation between chip operation and stress conditions during the accelerated life test. The chip that mounted four TVS with aging-tolerant ROs is accelerated by exposing it under high stress condition during 174.85 hours on 14 days (12.5 hours per a day) as shown in Fig. 5. After 12.5 hours of accelerating deterioration, turn-off the measurement device (power-off) and left the chip under the room temperature for 10.5 hours. When the chip is power-off state, its deterioration will be recovered. A measured RO frequency is that including recovery effect for non-operating. The experiment days are consecutive, but the experiment does not be performed on weekends and national holidays. Thus, the amount of recovery for degraded RO frequency may be different before and after these days. As high stress conditions for accelerating deterioration, temperature and voltage are 85°C and 2.0V (standard core voltage is 1.2V), respectively. The temperature is a limit of heat resistance temperature of DUT board, the voltage is a value close to the upper limit of the chip's correct operation. Accelerating time is the time excluding nighttime for safety reasons.

Fig. 6 shows a detail of the chip operation and the stress conditions. The RO frequency is measured under 30°C and 1.20V at the first of each experiment days. Then, to heat the chip from 30 to 85°C, and to wait for 1 hour until the temperature have stabilized. After the temperature stabilizes, the RO frequency is measured under 85°C and 1.20V. Next, the voltage sets to 2.00V for accelerated deterioration. While degradation is accelerated under 2.00V, the RO frequency is measured under 1.20V every 3 minutes. the measurement time is about 100 μsec. Therefore, the measurement under 85°C and 2.00V, and acceleration of deterioration under 85°C and 1.20V during 3 minutes are repeated for 125 hours. The RO frequency measurement means that to obtain three RO frequencies each from four TVSs on the chip. Also, in order to evaluate the difference in the effect of degradation of chip operation, the ROs of TVS1 are constantly oscillating and the ROs of TVS2~4 are oscillating every 3 minutes.

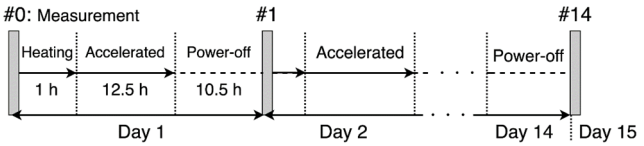


Fig. 5. Chip operations during 14 days

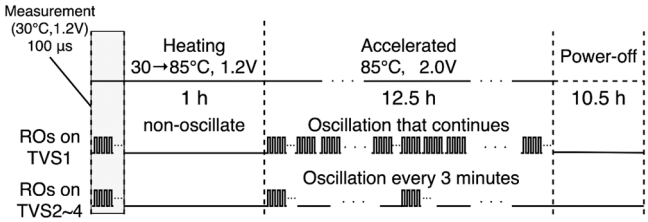


Fig. 6. Chip operations during 12.5 hours in each day

B. *Measured RO Frequencies due to Aging*

This section describes the effectiveness of aging-tolerant using the difference between RO frequencies of aging-tolerant and aging-intolerant ROs. In evaluating the frequency, all RO frequencies are converted to the value of frequency fluctuation due to deterioration in order to reduce the influence of process variation. Table I shows measured RO frequency of each TVS. The amount of fluctuation means that RO frequency measured on each day minus RO frequency measured on the first day. The fluctuation ratio means that the amount of fluctuation divided by RO frequency measured on the first day. In the TVS1, measured frequency of RO1, RO2, and RO3 are 204 MHz, 248 MHz, and 143 MHz. The amounts of fluctuation of RO1, RO2, and RO3 are -2.2 MHz, -4.1 MHz, and -1.4 MHz, respectively.

C. *Evaluation of aging-tolerant ROs*

This section shows RO frequency of TVS1 that constantly oscillates during deterioration accelerate and TVS2~4 that oscillates only during measuring, and quantitatively evaluations the frequency fluctuation reduction by aging-tolerant RO. The fluctuation ratio is used the first measured RO frequency is used in order to evaluate independent of process variation. Fig. 7 shows the relations between total experiment days and RO frequency. The graph uses the first measured RO frequency of each day as shown in Fig.6.

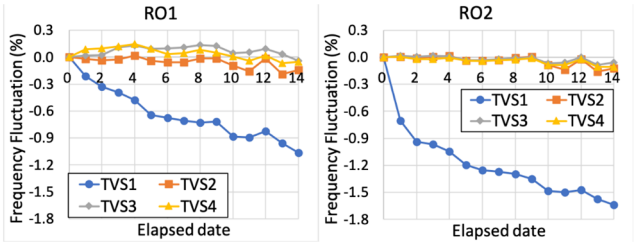
In order to evaluate the reduction of RO frequency of RO1 and RO2 with aging-tolerant, to compare the TVS1 that oscillates during deterioration acceleration and TVS2 that oscillates during measurement only. The RO ratio of RO1~3 of TVS1 are on the decline as shown in Fig 7. In the case of TVS2, the ratio of RO3 is only on the decline. In the measurement at the last day shows that deteriorated RO frequencies of RO1~3 in TVS1 are -1.1%, -1.6%, and -0.95%, respectively. Since RO1 and RO2 have aging-tolerant when not oscillating, it is confirmed that the effectiveness of the aging-tolerant ROs. However, since TVS1 was oscillating during accelerated deterioration, RO1 and RO2 deteriorate. On the other hand, RO1~3 of TVS2 are -0.14%, -0.13%, and -0.97%, respectively. TVS2 was oscillating only during measurement then, RO1, RO2 of TVS2 is reduced compared to that of TVS1. The TVS2's amount of fluctuation is RO frequency was reduced such as RO1 can be reduced 13% and RO2 is 7.6%. In the same way, RO1~3 of TVS3 are -0.039%, -0.059%, and -0.98%. RO1~3 of TVS4 are -0.050%, -0.11%, -1.1 %, respectively. When the condition that one of each RO of TVS1 is 100%, RO1 of the other TVS was reduced from 3.7% to 13% and RO2 from 3.6% to 7.6% under. aging-tolerant structure used in this experiment can reduce the logarithmically large fluctuation for accelerated deterioration on the first day.

V. Evaluation of Aging-tolerant RO for Sensor Applications

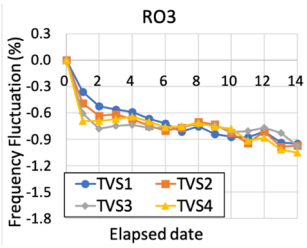
A. *Pre-experiment for Temperature and Voltage Estimation*

In order to evaluate an accuracy of the TVS estimation, temperature and voltage estimation equations are derived from the relationship among three RO frequencies, temperature, and voltage. In this paper, instead of SPICE simulation, measured values of a representative chip of the same manufacture chip are used.

The RO frequency is measured by using the constant temperature bath to set the temperature every 10°C from 30 to 80 and the portable tester to set the voltage every 0.01V from 1.00V to 1.40V. Temperature and voltage estimation equation based on measured RO frequency is generated. Each coefficient is defined such as $\alpha_{\Delta T}$, $b_{\Delta T}$, $c_{\Delta T}$, and $d_{\Delta T}$ are 13.86, -1.31, and -18.83, 30. $\alpha_{\Delta V}$, $b_{\Delta V}$, $c_{\Delta V}$, and $d_{\Delta V}$ are 0.003, -0.028, 0.048, and 1.2, respectively. Table II shows the estimation error of this estimation equation on temperature each 10 °C from 30°C to 80°C and voltage each 0.01V from 1.00V to 1.40V. The range of temperature estimation error is from -4.9°C to +4.9°C and voltage error is from -14mV to +9.3mV. In order to reduce the influence of process variation between the representative chip and test chip, the estimation equation is calibrated using RO frequency in 30°C and 1.2V. Calibrated coefficients $\alpha_{\Delta T}$, $b_{\Delta T}$, $c_{\Delta T}$, and $d_{\Delta T}$ are 13.93, -1.31, -18.66, and -68.54. $\alpha_{\Delta V}$, $b_{\Delta V}$, $c_{\Delta V}$, $d_{\Delta V}$, and are 0.004, -0.028, 0.047, and -1.18, respectively.



(a) RO1 (b) RO2



(c) RO3

Fig. 7. RO frequency fluctuation variations during 14 days

B. *Evaluation of Influence for Temperatire Measurement*

This section compares TVS1 and TVS2~4 to evaluate whether it can maintain estimation accuracy before deterioration by using aging-tolerant RO. In evaluating, RO3 mounted on TVS2~4 is assumed that has aging-tolerant then, it is set to fixed value is frequency that is value of first measurement on the first day.

TVS1 with deterioration RO and TVS2~4 or TVS2~4 with deterioration RO3 and TVS2~4 with no deteriorating RO3 were compared the amount of influence of RO frequency fluctuation on estimation error. As comparing of evaluation, the RO3 mounted on TVS2~4 is assumed that has aging-tolerant structure and it is defined as a fixed value measured RO3 frequency at first measurement on the first day of the experiment. RO3 with deterioration value is defined as *deteriorated RO3*. RO3 with fixed value is defined as *non-deteriorated RO3*. *deteriorated RO3* is used the frequency measured each experiment day and *non-deteriorated RO3* is used the frequency measured the first experiment day. Table III describes the temperature estimation error by RO3 deterioration and Fig. 8 shows the relationship total experiment days and estimation error of each TVS. Fig. 8(a) show the estimation result which use RO1 and RO2, deteriorated RO3 frequency to estimate temperature and Fig. 8(b) show the result which use RO1 and RO2, RO3 that is frequency before deterioration as fixed value.

TABLE I. PERFORMANCE OF THE TEMPERATURE AND VOLTAGE SENSOR BEFORE ACCELERATED LIFE TEST

		TVS1 (MHz)			TVS2 (MHz)			TVS3 (MHz)			TVS4 (MHz)		
Total days	Accelerlate Time(h)	RO1	RO2	RO3	RO1	RO2	RO3	RO1	RO2	RO3	RO1	RO2	RO3
1	0	203.680	248.392	143.041	205.739	249.685	142.863	202.527	246.837	141.427	203.544	247.604	142.032
2	12.4	203.246	246.643	142.529	205.701	249.697	142.162	202.565	246.870	140.569	203.716	247.616	141.046
3	24.9	203.014	246.057	142.289	205.670	249.655	141.963	202.571	246.842	140.322	203.743	247.550	141.052
4	37.4	202.882	245.991	142.236	205.686	249.691	141.982	202.745	246.879	140.370	203.784	247.554	141.082
5	49.9	202.704	245.796	142.198	205.775	249.727	141.907	202.786	246.865	140.386	203.839	247.587	141.119
6	62.4	202.365	245.427	142.094	205.657	249.591	141.799	202.715	246.757	140.339	203.732	247.506	141.044
7	74.9	202.305	245.271	142.009	205.620	249.589	141.718	202.720	246.763	140.344	203.615	247.500	140.951
8	87.4	202.235	245.242	141.881	205.625	249.609	141.765	202.744	246.781	140.359	203.635	247.523	140.967
9	99.9	202.195	245.165	141.965	205.708	249.666	141.858	202.795	246.805	140.397	203.705	247.539	141.022
10	112.4	202.218	245.039	141.842	205.713	249.700	141.819	202.782	246.835	140.385	203.643	247.571	140.955
11	124.9	201.884	244.713	141.793	205.547	249.475	141.678	202.620	246.661	140.275	203.560	247.386	140.924
12	137.4	201.859	244.673	141.786	205.408	249.331	141.512	202.634	246.692	140.286	203.461	247.390	140.730
13	149.9	201.998	244.739	141.877	205.707	249.625	141.704	202.715	246.836	140.339	203.580	247.549	140.780
14	162.4	201.727	244.487	141.699	205.347	249.279	141.458	202.593	246.630	140.255	203.409	247.338	140.582
15	174.9	201.510	244.327	141.686	205.444	249.373	141.475	202.448	246.691	140.045	203.441	247.336	140.540

TABLE II. PERFORMANCE OF THE TEMPERATURE AND VOLTAGE SENSOR BEFORE ACCELERATED LIFE TEST

Model TVS Estimation Error		
	Temperature(°C)	Voltage (mV)
+MAX	4.903	14.135
-MAX	-4.932	-9.332
Average	0.000	0.000
Std.Dev	1.855	4.243

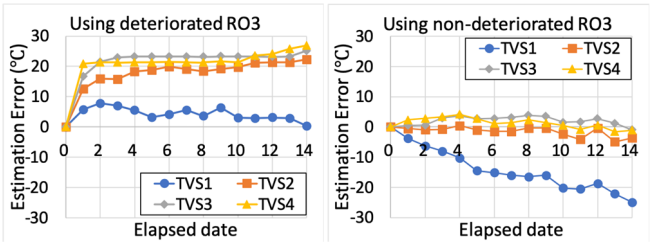
First, comparing the estimation result of TVS1 with *deteriorated RO3* and TVS2 with *non-deteriorated RO3*, estimation accuracy of TVS1 with aging-intolerant RO worse such as its range is from 0°C to 7.8°C. On the other hand, the range of TVS2 with aging-tolerant RO is from -4.9°C to 0.45°C then the range was reduced 2.5°C by using aging-tolerant, as well in TVS3 and TVS4. The reason is why aging-tolerant can reduce the logarithmically large fluctuation for accelerated deterioration on the first day. In addition, it is thought that the balance the coefficient and RO frequency fluctuation reduced estimation error. In the case of TVS1, RO2 frequency fluctuation is the largest from Table I but $b_{\Delta V}$ is smaller than $a_{\Delta V}$ and $c_{\Delta V}$. Since RO1 which coefficient value is high is smaller than that of RO2, the estimation accuracy did not deteriorate.

Second, evaluate the effect of an RO frequency fluctuation on estimation accuracy by comparing temperature estimation of TVS2 using *deteriorated RO3* and *non-deteriorated RO3*. Temperature estimation error range of TVS2 by using aging-tolerant RO3 changes from 22°C to 5.3°C (range of -4.9°C~+0.45°C). The estimation accuracy can be improved 17°C using the aging-tolerant RO3. This measurement result suggests that aging-tolerant structure is effective in reducing estimation accuracy deterioration.

Note that, in the case of focusing on the influence of alone RO, the accuracy deteriorated. The temperature estimation error range of TVS1 increased from 7.9°C to 25°C (range of -25°C~0.0°C). However, a measurement condition of TVS1 does not aim an evaluation of NBTI aging phenomena. Thus, it cannot be decided that the estimation error deteriorate due to aging-tolerant structure.

TABLE III. TEMPERATURE MEASUREMENT ACCURACY

Temperature Estimate Error (°C)								
	RO1, RO2, deteriorate_RO3				*RO1, RO2, non-deteriorate_RO3*			
	TVS1	TVS2	TVS3	TVS4	TVS1	TVS2	TVS3	TVS4
+MAX	7.804	22.287	25.167	26.984	0.000	0.451	3.803	4.140
-MAX	0.000	0.000	0.000	0.000	-24.915	-4.874	-0.919	-1.522



(a) The case for *deteriorated RO3* (b)The case for non-deteriorated RO3

Fig. 8. Temperature measurement accuracy

C. *Evaluation of Influence for Voltage Measurement*

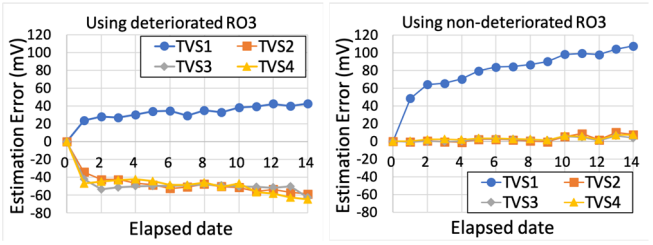
This section describes effectiveness of AGING-tolerant in voltage measurement accuracy of TVS as well as temperature. Table IV describes the voltage estimation error by RO3 deterioration and Fig. 9 shows the relationship total experiment days and estimation error of each TVS. Fig. 9(a) show the estimation error which use RO1 and RO2, deteriorated RO3 frequency to estimate temperature and Fig. 8(b) show the result which use RO1 and RO2, RO3 that is frequency before deterioration as fixed value.

First, comparing the estimation result of TVS1 with *deteriorated RO3* and TVS2 with *non-deteriorated RO3*, estimation accuracy of TVS1 with non-NBTI tolerant RO worse such as its range is from 0mV to 43mV. On the other hand, the estimation error range of TVS2 is from -10mV to 0mV then the range was reduced 32mV by using aging-tolerant, as well in TVS3 and TVS4. The voltage estimation accuracy of TVS1 worse because the coefficient of RO2 $b_{\Delta V}$ is higher than the other coefficients $a_{\Delta V}, c_{\Delta V}$ and RO2 frequency fluctuation is higher than the others so influence of RO2 on voltage estimation accuracy is strong.

Second, comparing temperature estimation of TVS2 using *deteriorated RO3* and *non-deteriorated RO3* to evaluate the effect of an RO frequency fluctuation on estimation accuracy, Estimation error of TVS2 with *deteriorated RO3* is -58mV that is the largest, then it increases 47mV than its TVS2 with *non-deteriorated RO3*. In other words, RO3 frequency fluctuation means the 4 times more estimation error. Even if it estimates voltage, aging-tolerant RO decreases the amount of estimation accuracy deterioration.

TABLE IV. VOLTAGE MEASUREMENT ACCURACY

Voltage Estimate Error (mV)								
	RO1, RO2, deteriorate_RO3				*RO1, 2, non-deteriorate_RO3*			
	TVS1	TVS2	TVS3	TVS4	TVS1	TVS2	TVS3	TVS4
+MAX	43.010	0.000	0.000	0.000	107.587	10.022	6.231	7.259
-MAX	0.000	-58.498	-62.711	-64.397	0.000	-1.037	-0.797	0.000



(a) The case for *deteriorated RO3* (b)The case for *non-deteriorated RO3*

Fig. 9. Voltage measurement accuracy

VI. CONCLUSION

This paper discussed about the effectiveness of aging-tolerant ROs using a test chip with 65nm CMOS technology and accelerated life test. Its application to an RO-based digital temperature and voltage sensor (TVS) was also evaluated. In order to evaluate the influence of aging-tolerant on the reduction of the amount of RO frequency fluctuation and the estimation accuracy of the TVS, accelerated life test was performed under different operating conditions for each of the four TVSs on the chip. Some experiments focus on RO frequency and results show the effect of aging-tolerant ROs, e.g. reduction of the RO frequency fluctuation by maximum 93% comparing RO frequency on the first day and last day. Then, they evaluated the estimation accuracy of the TVS with aging-tolerant RO in term of temperature and voltage. The estimation accuracy of the TVS with aging-tolerant RO is higher than that with deteriorated RO. In particular, estimation error ranges of TVS2 were reduced 2.5°C and 33mV compared to TVS1, respectively. In addition, comparing the errors of using aging-tolerant RO and aging-intolerant RO, the influence of RO3 with aging-tolerant were reduced 17°C and voltage 47mV than aging-intolerant. Therefore, aging-tolerant ROs can maintain the measurement accuracy of the TVS. As future works, a combination method that maintains TVS estimation error even if RO deteriorates, or a correction method that reduce TVS estimation accuracy deterioration by correcting the coefficient according to the amount of degradation RO will be investigated.

ACKNOWLEDGMENT

The VLSI chip in this study has been fabricated in the chip fabrication program of through the activities of VDEC, the University of Tokyo in collaboration with Renesas Electronics Corp. and Nippon Systemware Co., Ltd.

This work was supported by JSPS KAKENHI Grant Numbers JP19K20236 and JP18KT0014.

REFERENCES

[1] N. Kanekawa, E. Ibe, T. Suga, and Y. Uematsu, *Dependability in Electronic Systems: Mitigation of Hardware Failures, Soft Errors, and Electro-Magnetic Disturbances*, Springer, 2010

[2] H. Yi, T. Yoneda, I. Inoue, Y. Sato, S. Kajihara, and H. Fujiwara, "A failure prediction strategy for transistor aging," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 11, pp. 1951-1959, Nov. 2012.

[3] S. Reda, R. J. Cochran, A. N. Nowroz, "Improved thermal tracking for processors using hard and soft sensor allocation techniques," *IEEE Trans. on Computers*, vol. 60, no. 6, pp. 814-851, 2011.

[4] A. Bakker and J. H. Huijsing, "Micropower CMOS temperature sensor with digital output," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 933-937, Jul. 1996.

[5] M. A. P. Pertijs, K. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.1 C from -55 C to 125 C," *IEEE J. Solid-State Circuits*, vol.40, no.12, pp.2805-2815, Dec. 2005.

[6] P. Chen, C.C. Chen, C.C. Tsai, and W. F. Lu, "A time-to-digital-converter-based CMOS smart temperature sensor," *IEEE J. Solid-State Circuits*, vol.40, no.8, pp.1642-1648, Aug. 2005.

[7] C.-C. Chung and C.-R. Yang, "An Autocalibrated All-Digital Temperature Sensor for On-Chip Thermal Monitoring," *IEEE Trans. on Circuits Syst. II, Exp. Briefs*, vol. 58, no2, pp.105-107, Feb. 2011.

[8] S. Xie and W. T. Ng, "Digital integrated temperature sensors for VLSI thermal management," *Proc. IEEE Int'l Conf. on Solid-State and Integrated Circuit Technology*, pp.1-4, Oct. 2014.

[9] G. M. Quenot, N. Paris, and B. Zavidovique, "A Temperature and Voltage Measurement Cell for VLSI Circuits," *Proc. IEEE Euro ASIC,* pp. 334-338, May. 1991.

[10] Y. Miyake, Y. Sato, S. Kajihara, and Y. Miura, "Temperature and Voltage Measurement for Field Test Using an Aging-Tolerant Monitor," *IEEE Trans. on Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 11, pp. 3282-3295, Nov. 2016.

[11] Y. Miyake, Y. Sato, and S. Kajihara, "A Selection Method of Ring Oscillators for An On-chip Digital Temperature and Voltage Sensor," *Proc. IEEE International Test Conference in Asia*, pp. 13-18, Sep. 2019.

[12] R. Kishida, T. Asuke, J. Furuta, and K. Kobayashi, "Extracting Voltage Dependence of BTI-induced Degradation without Temporal Factors by Using BTI-Sensitive and BTI-Insensitive Ring Oscillators," *IEEE Trans. on Semiconductor Manufacturing*, vol. 33, no. 2, pp. 174-179, May 2020.

[13] S. Khan and S. Hamdioui, "Modeling and mitigating NBTI in nanoscale circuits," *Proc. IEEE On-Line Testing Symposium*, pp. 1-6, July 2011.

[14] I.-C. Lin, C.-H. Lin, and K.-H. Li, "Leakage and Aging Optimization Using Transmission Gate-Based Technique," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 1, pp. 87–99, Jan. 2013.

[15] A. Calimera, E. Macii, and M. Poncino, "NBTI-aware power gating for concurrent leakage and aging optimization," *Proc. ACM/IEEE Int. Symp. Low Power Electron. Design*, pp. 127–132, Aug. 2009.

[16] L. Zhang and R. P. Dick, "Scheduled voltage scaling for increasing lifetime in the presence of NBTI," *Proc. IEEE Asia and South Pacific Design Automation Conference*, pp. 492-497, Jan. 2009.

[17] Y. Miyake, T. Kato, S. Kajihara, M. Aso, H. Futami, S. Matsunaga, Y. Miura, "On-Chip Delay Measurement for Degradation Detection And Its Evaluation under Accelerated Life Test," *Proc. IEEE International Symposium on On-Line Testing and Robust System Design*, July 2020.

[18] I.A.K.M Mahfuzul and H. Onodera, "On-Chip Detection of Process Shift and Process Spread for Silicon Debugging and Model-Hardware Correlation," *Proc. IEEE Asian Test Symp*., pp. 350~354, Nov. 2012.